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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	26
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8013mfae

Document Revision History (Continued)

Version History	Description of Change
Rev. 8	• In **Table 10-4**, added an entry for flash data retention with less than 100 program/erase cycles (minimum 20 years). • In **Table 10-6**, changed the device clock speed in STOP mode from 8MHz to 4MHz. • In **Table 10-12**, changed the typical relaxation oscillator output frequency in Standby mode from 400kHz to 200kHz.
Rev. 9	In **Table 10-19**, changed the maximum ADC internal clock frequency from 8MHz to 5.33MHz.
Rev. 10	Added the following note to the description of the TMS signal in **Table 2-3**: **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
Rev. 11	Removed “Preliminary” and made changes throughout the book, including changes in the following sections: • Feature additions to **Section 1.1.4** • Deleted Section 1.4.1 • **Table 2-3** • Added diagram in **Section 3.5.1** • Added paragraph to **Section 5.3** • Deleted Section 5.5, “Operating Modes” • Added features to **Section 6.2** • **Section 6.3.8.1** and **Section 6.3.8.2** • Deleted note from **Section 6.3.8.3** • Clarifications to **Section 6.3** register descriptions • Removed paragraph from **Section 6.4**
Rev. 12	• Revised **Section 7, Security Features**. • Updated temperature information in **Table 10-1** and **Table 10-4**. • Fixed miscellaneous errors.

Please see http://www.freescale.com for the most current data sheet revision.

56F8013/56F8011 Data Sheet Table of Contents

1.7 Product Documentation

The documents listed in **Table 1-2** are required for a complete description and proper design with the 56F8013 or 56F8011. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at:
http://www.freescale.com

Table 1-2 56F8013/56F8011 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit Digital Signal Controller core processor, and the instruction set	DSP56800ERM
56F801X Peripheral Reference Manual	Detailed description of peripherals of the 56F801X family of devices	MC56F8000RM
56F801X Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F801x family of devices	56F801XBLUG
56F8013/56F8011 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8013
Errata	Details any chip issues that might be present	MC56F8013E MC56F8011E

1.8 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
“asserted”	A high true (active high) signal is high or a low true (active low) signal is low.
“deasserted”	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56F8013/56F8011 are organized into functional groups, as detailed in **Table 2-1**. **Table 2-2** summarizes all device pins. In **Table 2-2**, each table row describes the signal or signals present on a pin, sorted by pin number.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins
Power (V_{DD} or V_{DDA})	2
Ground (V_{SS} or V_{SSA})	3
Supply Capacitors	1
Reset	1
Pulse Width Modulator (PWM) Ports[1]	7
Serial Peripheral Interface (SPI) Ports[2]	4
Analog-to-Digital Converter (ADC) Ports	6
Timer Module Ports[3]	2
Serial Communications Interface (SCI) Ports[4]	2
JTAG/Enhanced On-Chip Emulation (EOnCE)	4

1. Pins in this section can function as Timer and GPIO.
2. Pins in this section can function as Timer, I^2C, and GPIO.
3. Pins can function as PWM and GPIO.
4. Pins in this section can function as I^2C and GPIO.

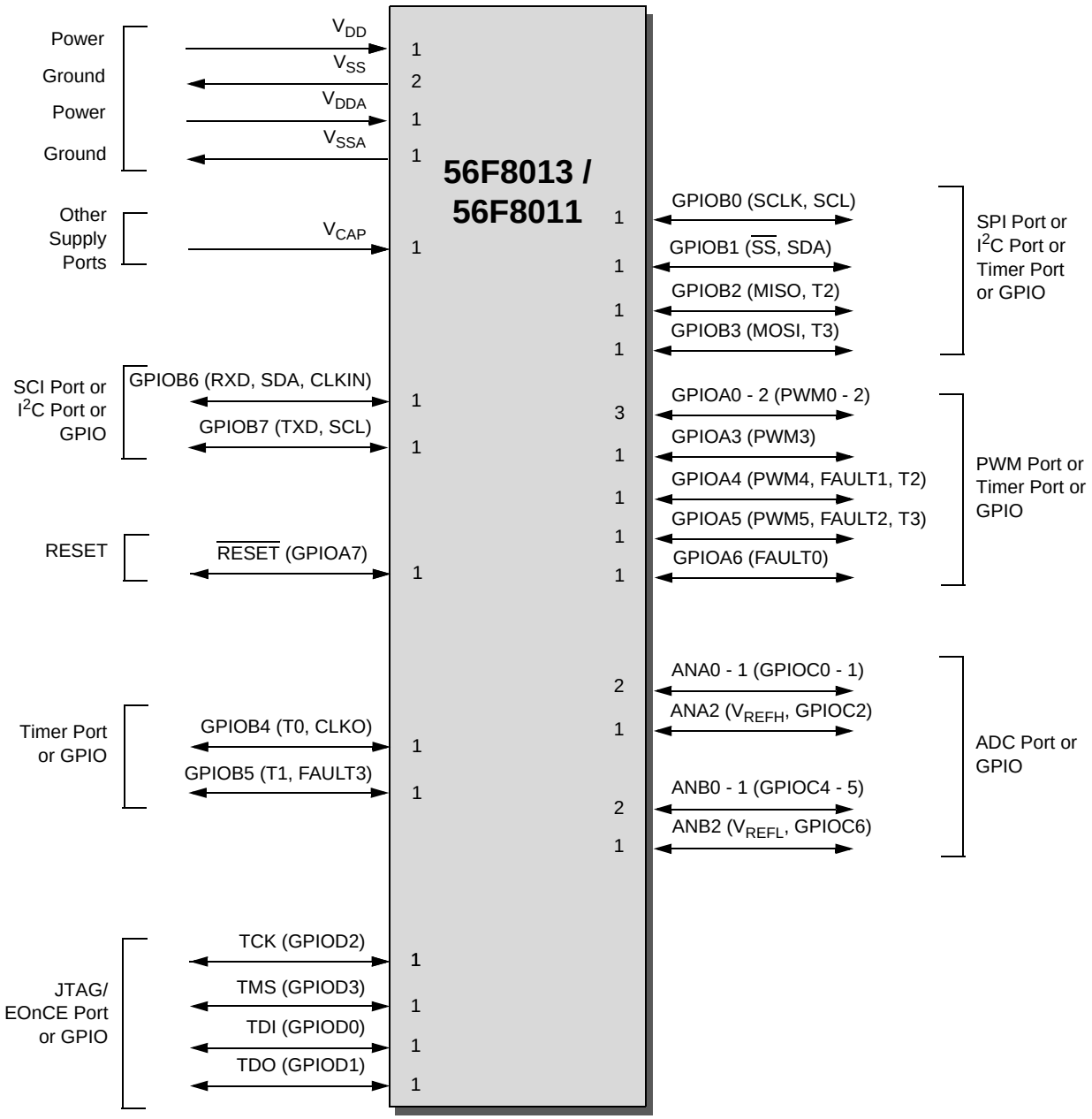


Figure 2-1 56F8013/56F8011 Signals Identified by Functional Group

Table 2-3 56F8013/56F8011 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOB2	17	Input/ Output	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(MISO)		Input/ Output		**SPI Master In/Slave Out** — This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The slave device places data on the MISO line a half-cycle before the clock edge the master device uses to latch the data.
(T2[5])		Input/ Output		**T2** — Timer, Channel 2 After reset, the default state is GPIOB2. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.
5. This signal is also brought out on the GPIOA4 pin.				
GPIOB3	16	Input/ Output	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(MOSI)		Input/ Output		**SPI Master Out/Slave In**— This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data.
(T3[6])		Input/ Output		**T3** — Timer, Channel 3 After reset, the default state is GPIOB3. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.
6. This signal is also brought out on the GPIOA5 pin.				
GPIOA0	29	Input/ Output	Input with internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(PWM0)		Output		**PWM0** — This is one of the six PWM output pins. After reset, the default state is GPIOA0.

Return to Table 2-2

Table 4-9 Quad Timer Registers Address Map (Continued) (TMR_BASE = $00 F000)

Register Acronym	Address Offset	Register Description
TMR0_CMPLD2	$9	Comparator Load Register 2
TMR0_CSCTRL	$A	Comparator Status and Control Register
		Reserved
TMR1_COMP1	$10	Compare Register 1
TMR1_COMP2	$11	Compare Register 2
TMR1_CAPT	$12	Capture Register
TMR1_LOAD	$13	Load Register
TMR1_HOLD	$14	Hold Register
TMR1_CNTR	$15	Counter Register
TMR1_CTRL	$16	Control Register
TMR1_SCTRL	$17	Status and Control Register
TMR1_CMPLD1	$18	Comparator Load Register 1
TMR1_CMPLD2	$19	Comparator Load Register 2
TMR1_CSCTRL	$1A	Comparator Status and Control Register
		Reserved
TMR2_COMP1	$20	Compare Register 1
TMR2_COMP2	$21	Compare Register 2
TMR2_CAPT	$22	Capture Register
TMR2_LOAD	$23	Load Register
TMR2_HOLD	$24	Hold Register
TMR2_CNTR	$25	Counter Register
TMR2_CTRL	$26	Control Register
TMR2_SCTRL	$27	Status and Control Register
TMR2_CMPLD1	$28	Comparator Load Register 1
TMR2_CMPLD2	$29	Comparator Load Register 2
TMR2_CSCTRL	$2A	Comparator Status and Control Register
		Reserved
TMR3_COMP1	$30	Compare Register 1
TMR3_COMP2	$31	Compare Register 2
TMR3_CAPT	$32	Capture Register
TMR3_LOAD	$33	Load Register
TMR3_HOLD	$34	Hold Register
TMR3_CNTR	$35	Counter Register
TMR3_CTRL	$36	Control Register
TMR3_SCTRL	$37	Status and Control Register
TMR3_CMPLD1	$38	Comparator Load Register 1
TMR3_CMPLD2	$39	Comparator Load Register 2
TMR3_CSCTRL	$3A	Comparator Status and Control Register

Table 4-15 I²C Registers Address Map (I2C_BASE = $00 F0D0)

Register Acronym	Address Offset	Register Description
I2C_ADDR	$0	Address Register
I2C_FDIV	$1	Frequency Divider Register
I2C_CTRL	$2	Control Register
I2C_STAT	$3	Status Register
I2C_DATA	$4	Data I/O Register
I2C_NFILT	$5	Noise Filter Register

Table 4-16 Computer Operating Properly Registers Address Map (COP_BASE = $00 F0E0)

Register Acronym	Address Offset	Register Description
COP_CTRL	$0	Control Register
COP_TOUT	$1	Time-Out Register
COP_CNTR	$2	Counter Register

Table 4-17 Clock Generation Module Registers Address Map (OCCS_BASE = $00 F0F0)

Register Acronym	Address Offset	Register Description
OCCS_CTRL	$0	Control Register
OCCS_DIVBY	$1	Divide-By Register
OCCS_STAT	$2	Status Register
		Reserved
OCCS_SHUTDN	$4	Shutdown Register
OCCS_OCTRL	$5	Oscillator Control Register

entering the Wait or Stop mode.

6.3 Register Descriptions

Table 6-1 SIM Registers (SIM_BASE = $00 F140)

Address Offset	Address Acronym	Register Name	Section Location
Base + $0	SIM_CTRL	Control Register	6.3.1
Base + $1	SIM_RSTAT	Reset Status Register	6.3.2
Base + $2	SIM_SWC0	Software Control Register 0	6.3.3
Base + $3	SIM_SWC1	Software Control Register 1	6.3.3
Base + $4	SIM_SWC2	Software Control Register 2	6.3.3
Base + $5	SIM_SWC3	Software Control Register 3	6.3.3
Base + $6	SIM_MSHID	Most Significant Half of JTAG ID	6.3.4
Base + $7	SIM_LSHID	Least Significant Half of JTAG ID	6.3.5
Base + $8	SIM_PWR	Power Control Register	6.3.6
		Reserved	
Base + $A	SIM_CLKOUT	CLKO Select Register	6.3.7
Base + $B	SIM_GPS	GPIO Peripheral Select Register	6.3.8
Base + $C	SIM_PCE	Peripheral Clock Enable Register	6.3.9
Base + $D	SIM_IOSAHI	I/O Short Address Location High Register	6.3.10
Base + $E	SIM_IOSALO	I/O Short Address Location Low Register	6.3.10

Add. Offset	Address Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	SIM_ CTRL	R	TC3_ SD	TC2_ SD	TC1_ SD	TC0_ SD	SCI_ SD	0	TC3_ INP	0	0	0	ONCE EBL	SW RST	STOP_ DISABLE		WAIT_ DISABLE	
		W																
$1	SIM_ RSTAT	R	0	0	0	0	0	0	0	0	0	0	SWR	COPR	EXTR	POR	0	0
		W																
$2	SIM_SWC0	R	Software Control Data 0															
		W																
$3	SIM_SWC1	R	Software Control Data 1															
		W																
$4	SIM_SWC2	R	Software Control Data 2															
		W																
$5	SIM_SWC3	R	Software Control Data 3															
		W																
$6	SIM_MSHID	R	0	0	0	0	0	0	0	1	1	1	1	1	0	0	1	0
		W																
$7	SIM_LSHID	R	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1
		W																
$8	SIM_PWR	R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LRSTDBY	
		W																
	Reserved																	
$A	SIM_ CLKOUT	R	0	0	0	0	0	0	$\overline{\text{PWM3}}$	$\overline{\text{PWM2}}$	$\overline{\text{PWM1}}$	$\overline{\text{PWM0}}$	CLK DIS	CLKOSEL				
		W																
$B	SIM_GPS	R	TCR	PCR	0	0	CFG_ B7	CFG_ B6	CFG_ B5	CFG_ B4	CFG_ B3	CFG_ B2	CFG_ B1	CFG_ B0	CFG_A5		CFG_A4	
		W																
$C	SIM_PCE	R	I2C	0	ADC	0	0	0	0	0	0	TMR	0	SCI	0	SPI	0	PWM
		W																
$D	SIM_IOSAHI	R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ISAL[23:22]	
		W																
$E	SIM_IOSALO	R	ISAL[21:6]															
		W																

0 = Read as 0
= Reserved

1 = Read as 1
= Reserved

Figure 6-1 SIM Register Map Summary

6.3.1 SIM Control Register (SIM_CTRL)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	TC3_ SD	TC2_ SD	TC1_ SD	TC0_ SD	SCI_ SD	0	TC3_ INP	0	0	0	ONCE EBL	SW RST	STOP_ DISABLE		WAIT_ DISABLE	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-2 SIM Control Register (SIM_CTRL)

6.3.1.1 Timer Channel 3 Stop Disable (TC3_SD)—Bit 15

This bit enables the operation of the Timer Channel 3 peripheral clock in Stop mode.

- 0 = Timer Channel 3 disabled in Stop mode

6.3.5 Least Significant Half of JTAG ID (SIM_LSHID)

This read-only register displays the least significant half of the JTAG ID for the chip. This register reads $401D.

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1
Write																
RESET	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1

Figure 6-6 Least Significant Half of JTAG ID (SIM_LSHID)

6.3.6 SIM Power Control Register (SIM_PWR)

This register controls the Standby mode of the large regulator. The large regulator derives the core digital logic power supply from the IO power supply. In some circumstances, the large regulator may be put in a reduced-power Standby mode without interfering with part operation. Refer to the overview of power-down modes and the overview of clock generation for more information on the use of large regulator standby.

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LRSTDBY	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-7 SIM Power Control Register (SIM_PWR)

6.3.6.1 Reserved—Bits 15–2

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.3.6.2 Large Regulator Standby Mode[1:0] (LRSTDBY)—Bits 1–0

This bit controls the pull-up resistors on the IRQA pin.

- 00 = Large regulator is in Normal mode
- 01 = Large regulator is in Standby (reduced-power) mode
- 10 = Large regulator is in Normal mode and the LRSTDBY field is write-protected until the next reset
- 11 = Large regulator is in Standby mode and the LRSTDBY field is write-protected until the next reset

NOTE:

Standby mode can be used when device operates below 200KHz with PLL shut down.

6.3.7 CLKO Select Register (SIM_CLKOUT)

The CLKO select register can be used to multiplex out selected clocks generated inside the clock

generation and SIM modules. All functionality is for test purposes only and is subject to unspecified latencies. Glitches may be produced when the clock is enabled or switched.

The lower four bits of the GPIO A register can function as GPIO, PWM, or as additional clock output signals. GPIO has priority and is enabled/disabled via the GPIOA_PEREN. If GPIOA[3:0] are programmed to operate as peripheral outputs, then the choice between PWM and additional clock outputs is done here in the CLKOUT. The default state is for the peripheral function of GPIOA[3:0] to be programmed as PWM. This can be changed by altering $\overline{\text{PWM3}}$ through $\overline{\text{PWM0}}$.

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	$\overline{\text{PWM3}}$	$\overline{\text{PWM2}}$	$\overline{\text{PWM1}}$	$\overline{\text{PWM0}}$	CLK DIS	CLKOSEL				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Figure 6-8 CLKO Select Register (SIM_CLKOUT)

6.3.7.1 Reserved—Bits 15–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.3.7.2 $\overline{\text{PWM3}}$—Bit 9

- 0 = Peripheral output function of GPIOA[3] is defined to be $\overline{\text{PWM3}}$
- 1 = Peripheral output function of GPIOA[3] is defined to be the Relaxation Oscillator Clock

6.3.7.3 $\overline{\text{PWM2}}$—Bit 8

- 0 = Peripheral output function of GPIOA[2] is defined to be $\overline{\text{PWM2}}$
- 1 = Peripheral output function of GPIOA[2] is defined to be the system clock

6.3.7.4 $\overline{\text{PWM1}}$—Bit 7

- 0 = Peripheral output function of GPIOA[1] is defined to be $\overline{\text{PWM1}}$
- 1 = Peripheral output function of GPIOA[1] is defined to be two times the rate of the system clock

6.3.7.5 $\overline{\text{PWM0}}$—Bit 6

- 0 = Peripheral output function of GPIOA[0] is defined to be $\overline{\text{PWM0}}$
- 1 = Peripheral output function of GPIOA[0] is defined to be three times the rate of the system clock

6.3.7.6 Clockout Disable (CLKDIS)—Bit 5

- 0 = CLKOUT output is enabled and will output the signal indicated by CLKOSEL
- 1 = CLKOUT is 0

6.3.7.7 Clockout Select (CLKOSEL)—Bits 4–0

Selects clock to be muxed out on the CLKO pin.

- 00000 = Reserved for factory test—Continuous system clock

Table 8-2 GPIO External Signals Map (Continued)
Pins in shaded rows are not available in 56F8013/56F8011

GPIO Function	Peripheral Function	LQFP Package Pin	Notes
GPIOB3	MOSI / T3	16	SIM register SIM_GPS is used to select between MOSI and T3 Defaults to B3
GPIOB4	T0 / CLKO	19	SIM register SIM_GPS is used to select between T0 and CLKO Defaults to B4
GPIOB5	T1 / FAULT3	4	SIM register SIM_GPS is used to select between T1 and FAULT3 Defaults to B5
GPIOB6	RXD / SDA / CLKIN	1	SIM register SIM_GPS is used to select between RXD and SDA. CLKIN functionality is enabled using the PLL Control Register within the OCCS block. Defaults to B6
GPIOB7	TXD / SCL	3	SIM register SIM_GPS is used to select between TXD and SCL Defaults to B7
GPIOC0	ANA0	12	Defaults to ANA0
GPIOC1	ANA1	11	Defaults to ANA1
GPIOC2	ANA2 / V_{REFH}	10	Defaults to ANA2
GPIOC3	ANA3		Not bonded out in 56F8013/56F8011 Defaults to ANA3
GPIOC4	ANB0	5	Defaults to ANB0
GPIOC5	ANB1	6	Defaults to ANB1
GPIOC6	ANB2 / V_{REFL}	7	Defaults to ANB2
GPIOC7	ANB3		Not bonded out in 56F8013/56F8011 Defaults to ANB3
GPIOD0	TDI	30	Defaults to TDI
GPIOD1	TDO	32	Defaults to TDO
GPIOD2	TCK	14	Defaults to TCK
GPIOD3	TMS	31	Defaults to TMS

8.3 Reset Values

Tables **4-18** through **4-21** detail registers for the 56F8013/56F8011; Figures **8-1** through **8-4** summarize register maps and reset values.

10.9 Serial Peripheral Interface (SPI) Timing

Table 10-14 SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 125 62.5	 — —	 ns ns	10-7, 10-8, 10-9, 10-10
Enable lead time Master Slave	t_{ELD}	 — 31	 — —	 ns ns	10-10
Enable lag time Master Slave	t_{ELG}	 — 125	 — —	 ns ns	10-10
Clock (SCK) high time Master Slave	t_{CH}	 50 31	 — —	 ns ns	10-7, 10-8, 10-9, 10-10
Clock (SCK) low time Master Slave	t_{CL}	 50 31	 — —	 ns ns	10-10
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	10-7, 10-8, 10-9, 10-10
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	10-7, 10-8, 10-9, 10-10
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	10-10
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	10-10
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	10-7, 10-8, 10-9, 10-10
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	10-7, 10-8, 10-9, 10-10
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	10-7, 10-8, 10-9, 10-10
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	10-7, 10-8, 10-9, 10-10

10.11 Serial Communication Interface (SCI) Timing

Table 10-16 SCI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud Rate[2]	BR	—	(f_{MAX}/16)	Mbps	—
RXD[3] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns	10-12
TXD[4] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns	10-13
LIN Slave Mode					
Deviation of slave node clock from nominal clock rate before synchronization	$F_{TOL\_UNSYNCH}$	-14	14	%	
Deviation of slave node clock relative to the master node clock after synchronization	F_{TOL_SYNCH}	-2	2	%	
Minimum break character length	T_{BREAK}	13		Master node bit periods	
		11		Slave node bit periods	

1. Parameters listed are guaranteed by design.
2. f_{MAX} is the frequency of operation of the system clock in MHz, which is 32MHz for the 56F8013/56F8011 devices.
3. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
4. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.

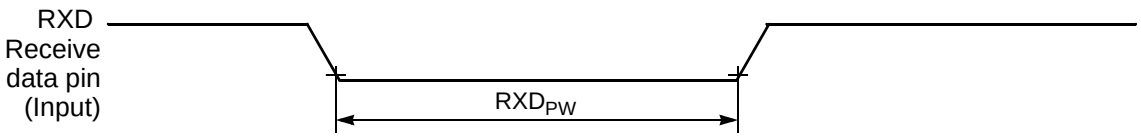


Figure 10-12 RXD Pulse Width

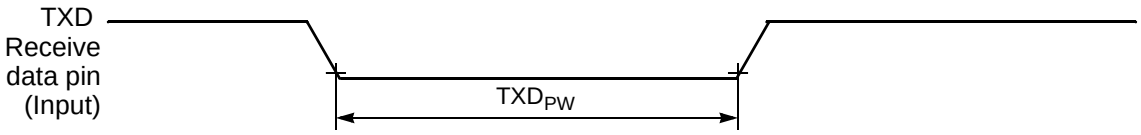


Figure 10-13 TXD Pulse Width

10.12 Inter-Integrated Circuit Interface (I^2C) Timing

Table 10-17 I^2C Timing

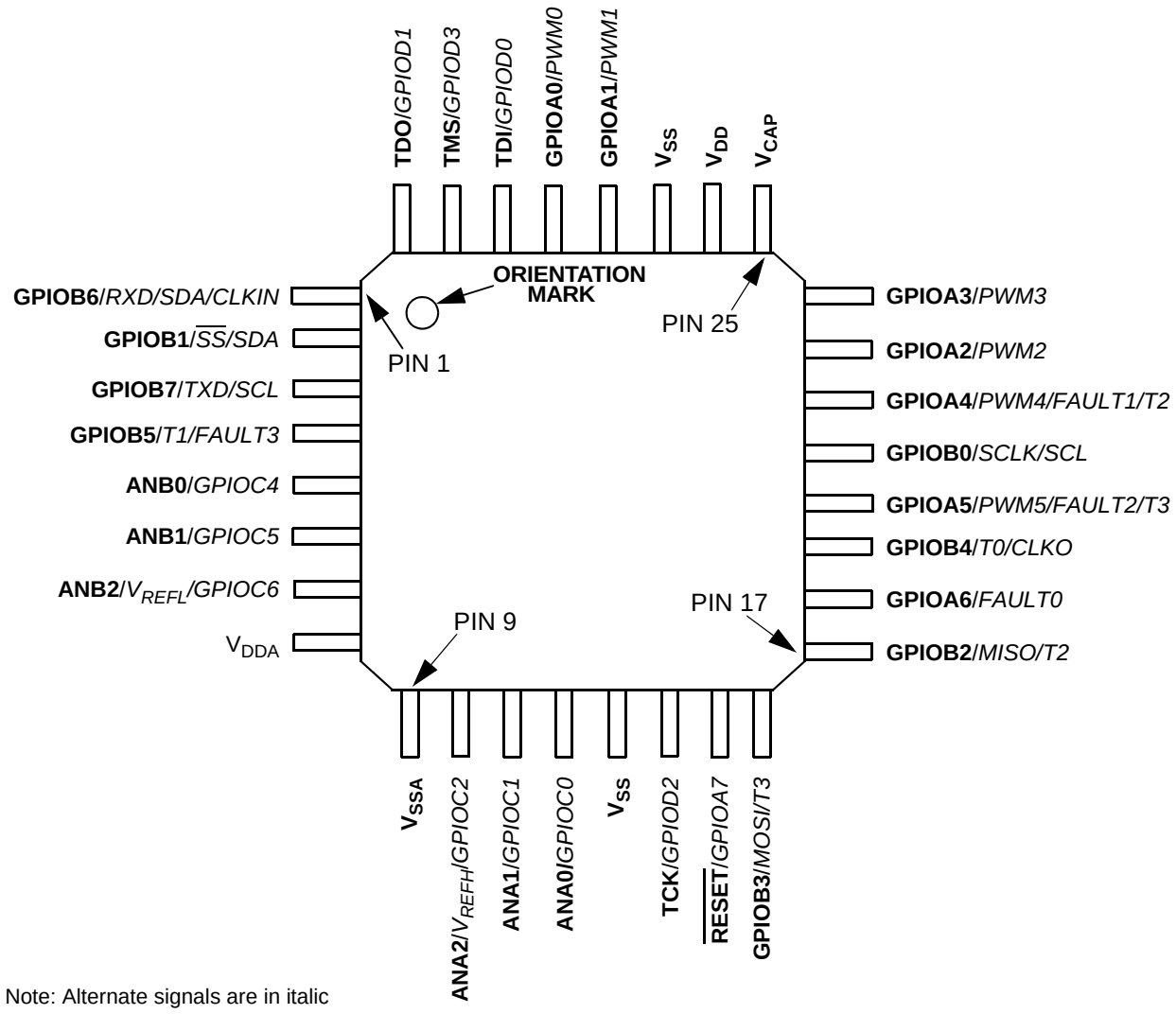
Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;\ STA}$	4.0		0.6		µs
LOW period of the SCL clock	t_{LOW}	4.7		1.25		µs
HIGH period of the SCL clock	t_{HIGH}	4.0		0.6		µs
Set-up time for a repeated START condition	$t_{SU;\ STA}$	4.7		0.6		µs
Data hold time for I^2C bus devices	$t_{HD;\ DAT}$	0[1]	3.45[2]	0[1]	0.9[2]	µs
Data set-up time	$t_{SU;\ DAT}$	250		100[3]		ns
Rise time of both SDA and SCL signals	t_r		1000	2 +0.1C_b[4]	300	ns
Fall time of both SDA and SCL signals	t_f		300	2 +0.1C_b[4]	300	ns
Set-up time for STOP condition	$t_{SU;\ STO}$	4.0		0.6		µs
Bus free time between STOP and START condition	t_{BUF}	4.7		1.3		µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0.0	50	ns

1. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
2. The maximum $t_{HD;\ DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. A Fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement $t_{SU;\ DAT}$ > = 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + $t_{SU;\ DAT}$ = 1000 + 250 = 1250ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
4. C_b = total capacitance of the one bus line in pF.

Part 11 Packaging

11.1 56F8013/56F8011 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8013/56F8011. These devices come in a 32-pin Low-profile Quad Flat Pack (LQFP). **Figure 11-1** shows the package outline for the 32-pin LQFP, **Figure 11-2** shows the mechanical parameters for this package, and **Table 11-1** lists the pin-out for the 32-pin LQFP.



Note: Alternate signals are in italic

Figure 11-1 Top View, 56F8013/56F8011 32-Pin LQFP Package

Part 12 Design Considerations

12.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

T_A = Ambient temperature for the package (^oC)
$R_{\theta JA}$ = Junction-to-ambient thermal resistance ($^oC/W$)
P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = Package junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = Thermocouple temperature on top of package (^oC)
Ψ_{JT} = Thermal characterization parameter ($^oC/W$)
P_D = Power dissipation in package (W)

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