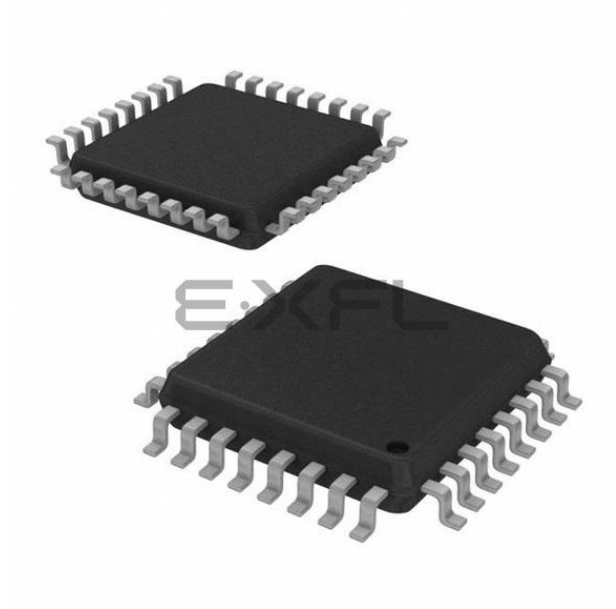

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	26
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8013vfae

Document Revision History

Version History	Description of Change
Rev. 0	Initial release.
Rev. 1	Updates to **Part 10, Specifications,** **Table 10-1**, added maximum clamp current, per pin **Table 10-12**, clarified variation over temperature table and graph **Table 10-16**, added LIN slave timing
Rev. 2	Added alternate pins to **Figure 11-1** and **Table 11-1**.
Rev. 3	Corrected ADC offering on page 3, clarified **Section 1.4.1**, corrected bit selects in Timer Channel 3 Input (TC3_INP) bit 9, **Section 6.3.1.7**, and simplified notes in **Table 10-9**.
Rev. 4	Added clarification on sync inputs in **Section 1.4.1**, added voltage difference specification to **Table 10-1** and **Table 10-4**, deleted formula for Ambient Operating Temperature in **Table 10-4**, also a note for pin group 3 to **Table 10-1**, corrected **Table 8-1**, error in Port C peripheral function configuration, removed text from notes in **Table 10-9** that referred to multiple flash blocks - this family has one flash block. Added RoHs and “pb-free” language to back cover.
Rev. 5	Updates to **Section 10** **Table 10-5**, corrected max values for ADC Input Current High and Low; corrected typ value for pull-up disabled Digital Input Current Low (a) **Table 10-6**, corrected typ and added max values for Standby > Stop and Powerdown modes **Table 10-7**, corrected min value for Low-Voltage Interrupt for 3.3V **Table 10-11**, corrected typ and max values and units for PLL lock time **Table 10-12**, corrected typ values for Relaxation Oscillator output frequency and variation over temperature (also increased temp range to 150 degreesC) and added variation over temperature from 0—105 degreesC Updated **Figure 10-5** **Table 10-19**, updated max values for Integral Non-Linearity full input signal range, Negative Differential Non-Linearity, ADC internal clock, Offset Voltage Internal Ref, Gain Error and Offset Voltage External Ref; updated typ values for Negative Differential Non-Linearity, Offset Voltage Internal Ref, Gain Error and Offset Voltage External Ref; added new min values and corrected typ values for Signal-to-noise ratio, Total Harmonic Distortion, Spurious Free Dynamic Range, Signal-to-noise plus distortion, Effective Number of Bits
Rev. 6	Added details to Section 1. Clarified language in State During Reset column in **Table 2-3**; corrected flash data retention temperature in **Table 10-4**; moved input current high/low to**Table 10-19** and location of footnotes in **Table 10-5**; reorganized **Table 10-19**; clarified title of **Figure 10-1**.
Rev. 7	Added information on automotive device for 56F8013. Added information on 56F8011device; edited to indicate differences in 56F8013 and 56F8011 devices. Updated values for $V_{EI3.3}$ and $V_{EI2.5}$ in Table 10-7. Deleted values for input and output voltage in Table 10-8. Added row for MC56F8013MFAE in Table 10-12.

Part 1 Overview

1.1 56F8013/56F8011 Features

1.1.1 Digital Signal Controller Core

- Efficient 16-bit 56800E family Digital Signal Controller (DSC) engine with dual Harvard architecture
- As many as 32 Million Instructions Per Second (MIPS) at 32MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, processor speed-independent, real-time debugging

1.1.2 Differences Between Devices

Table 1-1 outlines the key differences between the 56F8013 and 56F8011 devices.

Table 1-1 Device Differences

Feature	56F8013	56F8011
Program Flash	16KB	*12KB*
Unified Data/Program RAM	4KB	*2KB*

1.1.3 Memory

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security and protection that prevent unauthorized users from gaining access to the internal Flash
- On-chip memory:
  - 16KB of Program Flash (56F8013 device)
    12KB of Program Flash (56F8011 device)
  - 4KB of Unified Data/Program RAM (56F8013 device)
    2KB of Unified Data/Program RAM (56F8011 device)
- EEPROM emulation capability using Flash

- Up to 26 General-Purpose I/O (GPIO) pins with 5V tolerance
- Integrated Power-On Reset and Low-Voltage Interrupt Module
- Phase Lock Loop (PLL) provides a high-speed clock to the core and peripherals
- Clock Sources:
  - On-chip relaxation oscillator
  - External clock source
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- JTAG/EOnCE debug programming interface for real-time debugging

1.1.5 Energy Information

- Fabricated in high-density CMOS with 5V tolerance
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available
- ADC smart power management
- Each peripheral can be individually disabled to save power

1.2 56F8013/56F8011 Description

The 56F8013/56F8011 is a member of the 56800E core-based family of Digital Signal Controllers (DSCs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F8013/56F8011 is well-suited for many applications. The 56F8013/56F8011 includes many peripherals that are especially useful for industrial control, motion control, home appliances, general purpose inverters, smart sensors, fire and security systems, switched mode power supply, power management, and medical monitoring applications.

The 56800E core is based on a dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The 56F8013/56F8011 supports program execution from internal memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. The 56F8013/56F8011 also offers up to 26 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56F8013 Digital Signal Controller includes 16KB of Program Flash and 4KB of Unified Data/Program RAM. *The 56F8011 Digital Signal Controller includes 12KB of Program Flash and 2KB of Unified Data/Program RAM.* Program Flash memory can be independently bulk erased or erased in pages. Program Flash page erase size is 512 Bytes (256 Words).

A full set of programmable peripherals—PWM, ADCs, SCI, SPI, I^2C, Quad Timer—supports various applications. Each peripheral can be independently shut down to save power. Any pin in these peripherals can also be used as General Purpose Input/Outputs (GPIOs).

1.3 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Architecture Block Diagram

The 56F8013/56F8011's architecture is shown in **Figure 1-1**, **Figure 1-2**, and **Figure 1-3**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories and the IPBus Bridge and the internal connections between each unit of the 56800E core. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. **Figure 1-3** details how the device's I/O pins are muxed. The figures do not show the on-board regulator and power and ground signals. Please see **Part 2, Signal/Connection Descriptions**, to see which signals are multiplexed with those of other peripherals.

1.5 Synchronize ADC with PWM

ADC conversion can be synchronized with PWM module via Quad Timer channel 2 and 3 if needed. Internally, the PWM synch signal, which is generated at every PWM reload, can be connected to the timer channel 3 input and the timer channel 2 and 3 outputs are connected to ADC sync inputs. Timer channel 3 output is connected to SYNC0 and Timer channel 2 is connected to SYNC1. The setting is controlled by TC3_INP bit in the SIM Control Register; see **Section 6.3.1**.

SYNC0 is the master ADC sync input is used to trigger both ADCA and ADCB in sequence and parallel mode. SYNC1 is used to trigger ADCB in parallel independent mode, while SYNC0 is used to trigger ADCA. See 56F801X Peripheral Reference Manual for additional information.

1.6 Multiple Frequency PWM

When both PWM channels of a complementary pair in software control mode and software control bits are set to 1, each complementary PWM signal pair—PWM 0 and 1; PWM 2 and 3; PWM 4 and 5—can select a PWM source of one of following sources that enables each PWM pair to output different frequency PWM signal.

- External GPIO input:
  - GPIOB2 input can be used to drive PWM 0 and 1
  - GPIOB3 input can be used to drive PWM 2 and 3
  - GPIOB4 input can be used to drive PWM 4 and 5
- Quad Timer output:
  - Timer0 output can be used to drive PWM 0 and 1

Table 2-3 56F8013/56F8011 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOB7	3	Input/ Output	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(TXD)		Output		**Transmit Data** — SCI transmit data output or transmit / receive in single wire operation.
(SCL[2])		Input/ Output		**Serial Clock** — This pin serves as the I^2C serial clock. After reset, the default state is GPIOB7. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.
2. This signal is also brought out on the GPIOB0 pin.				
$\overline{\text{RESET}}$	15	Input	Input with internal pull-up enabled	**Reset** — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the chip is initialized and placed in the reset state. A Schmitt trigger input is used for noise immunity. The internal reset signal will be deasserted synchronous with the internal clocks after a fixed number of internal clocks.
(GPIOA7)		Input/Open Drain Output		**Port A GPIO** — This GPIO pin can be individually programmed as an input or open drain output pin. Note that $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can only be reset via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.
GPIOB4	19	Input/ Output	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(T0)		Input/ Output		**T0** — Timer, Channel 0
(CLKO)		Output		**Clock Output** — This is a buffered clock signal. Using the SIM_CLKO Select Register (SIM_CLKOSR), this pin can be programmed as any of the following: disabled (logic 0), CLK_MSTR (system clock), IPBus clock, or oscillator output. See **Section 6.3.7**. After reset, the default state is GPIOB4. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.

Return to Table 2-2

5.5.16 Interrupt Control Register (ICTRL)

$Base + $12	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	INT	IPIC		VAB							INT_DIS	1	1	1	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0

Figure 5-18 Interrupt Control Register (ICTRL)

5.5.16.1 Interrupt (INT)—Bit 15

This *read-only* bit reflects the state of the interrupt to the 56800E core.

- 0 = No interrupt is being sent to the 56800E core
- 1 = An interrupt is being sent to the 56800E core

5.5.16.2 Interrupt Priority Level (IPIC)—Bits 14–13

These *read-only* bits reflect the state of the new interrupt priority level bits being presented to the 56800E core. These bits indicate the priority level needed for a new IRQ to interrupt the current interrupt being sent to the 56800E core. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

- 00 = Required nested exception priority levels are 0, 1, 2, or 3
- 01 = Required nested exception priority levels are 1, 2, or 3
- 10 = Required nested exception priority levels are 2 or 3
- 11 = Required nested exception priority level is 3

Table 5-3 Interrupt Priority Encoding

IPIC_VALUE[1:0]	Current Interrupt Priority Level	Required Nested Exception Priority
00	No interrupt or SWILP	Priorities 0, 1, 2, 3
01	Priority 0	Priorities 1, 2, 3
10	Priority 1	Priorities 2, 3
11	Priority 2 or 3	Priority 3

5.5.16.3 Vector Number - Vector Address Bus (VAB)—Bits 12–6

This *read-only* field shows the vector number (VAB[6:0]) used at the time the last IRQ was taken. In the case of a Fast Interrupt, it shows the lower address bits of the jump address. This field is only updated when the 56800E core jumps to a new interrupt service routine.

6.3 Register Descriptions

Table 6-1 SIM Registers (SIM_BASE = $00 F140)

Address Offset	Address Acronym	Register Name	Section Location
Base + $0	SIM_CTRL	Control Register	6.3.1
Base + $1	SIM_RSTAT	Reset Status Register	6.3.2
Base + $2	SIM_SWC0	Software Control Register 0	6.3.3
Base + $3	SIM_SWC1	Software Control Register 1	6.3.3
Base + $4	SIM_SWC2	Software Control Register 2	6.3.3
Base + $5	SIM_SWC3	Software Control Register 3	6.3.3
Base + $6	SIM_MSHID	Most Significant Half of JTAG ID	6.3.4
Base + $7	SIM_LSHID	Least Significant Half of JTAG ID	6.3.5
Base + $8	SIM_PWR	Power Control Register	6.3.6
		Reserved	
Base + $A	SIM_CLKOUT	CLKO Select Register	6.3.7
Base + $B	SIM_GPS	GPIO Peripheral Select Register	6.3.8
Base + $C	SIM_PCE	Peripheral Clock Enable Register	6.3.9
Base + $D	SIM_IOSAHI	I/O Short Address Location High Register	6.3.10
Base + $E	SIM_IOSALO	I/O Short Address Location Low Register	6.3.10

Add. Offset	Address Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	SIM_ CTRL	R	TC3_ SD	TC2_ SD	TC1_ SD	TC0_ SD	SCI_ SD	0	TC3_ INP	0	0	0	ONCE EBL	SW RST	STOP_ DISABLE		WAIT_ DISABLE	
		W																
$1	SIM_ RSTAT	R	0	0	0	0	0	0	0	0	0	0	SWR	COPR	EXTR	POR	0	0
		W																
$2	SIM_SWC0	R	Software Control Data 0															
		W																
$3	SIM_SWC1	R	Software Control Data 1															
		W																
$4	SIM_SWC2	R	Software Control Data 2															
		W																
$5	SIM_SWC3	R	Software Control Data 3															
		W																
$6	SIM_MSHID	R	0	0	0	0	0	0	0	1	1	1	1	1	0	0	1	0
		W																
$7	SIM_LSHID	R	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1
		W																
$8	SIM_PWR	R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LRSTDBY	
		W																
	Reserved																	
$A	SIM_ CLKOUT	R	0	0	0	0	0	0	$\overline{\text{PWM3}}$	$\overline{\text{PWM2}}$	$\overline{\text{PWM1}}$	$\overline{\text{PWM0}}$	CLK DIS	CLKOSEL				
		W																
$B	SIM_GPS	R	TCR	PCR	0	0	CFG_ B7	CFG_ B6	CFG_ B5	CFG_ B4	CFG_ B3	CFG_ B2	CFG_ B1	CFG_ B0	CFG_A5		CFG_A4	
		W																
$C	SIM_PCE	R	I2C	0	ADC	0	0	0	0	0	0	TMR	0	SCI	0	SPI	0	PWM
		W																
$D	SIM_IOSAHI	R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ISAL[23:22]	
		W																
$E	SIM_IOSALO	R	ISAL[21:6]															
		W																

0 = Read as 0
= Reserved

1 = Read as 1
= Reserved

Figure 6-1 SIM Register Map Summary

6.3.1 SIM Control Register (SIM_CTRL)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	TC3_ SD	TC2_ SD	TC1_ SD	TC0_ SD	SCI_ SD	0	TC3_ INP	0	0	0	ONCE EBL	SW RST	STOP_ DISABLE		WAIT_ DISABLE	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-2 SIM Control Register (SIM_CTRL)

6.3.1.1 Timer Channel 3 Stop Disable (TC3_SD)—Bit 15

This bit enables the operation of the Timer Channel 3 peripheral clock in Stop mode.

- 0 = Timer Channel 3 disabled in Stop mode

6.3.1.11 Stop Disable (STOP_DISABLE[1:0])—Bits 3–2

- 00 = Stop mode will be entered when the 56800E core executes a STOP instruction
- 01 = The 56800E STOP instruction will not cause entry into Stop mode
- 10 = Stop mode will be entered when the 56800E core executes a STOP instruction and the STOP_DISABLE field is write-protected until the next reset
- 11 = The 56800E STOP instruction will not cause entry into Stop mode and the STOP_DISABLE field is write-protected until the next reset

6.3.1.12 Wait Disable (WAIT_DISABLE[1:0])—Bits 1–0

- 00 = Wait mode will be entered when the 56800E core executes a WAIT instruction
- 01 = The 56800E WAIT instruction will not cause entry into Wait mode
- 10 = Wait mode will be entered when the 56800E core executes a WAIT instruction and the WAIT_DISABLE field is write-protected until the next reset
- 11 = The 56800E WAIT instruction will not cause entry into Wait mode and the WAIT_DISABLE field is write-protected until the next reset

6.3.2 SIM Reset Status Register (SIM_RSTAT)

This register is updated upon any system reset and indicates the cause of the most recent reset. It also controls whether the COP reset vector or regular reset vector in the vector table is used. This register is asynchronously reset during Power-On Reset (see power supervisor module) and subsequently is synchronously updated based on the level of the external reset, software reset, or cop reset inputs. Only one source will ever be indicated. In the event that multiple reset sources assert simultaneously, the highest-precedence source will be indicated. The precedence from highest to lowest is POR, EXTR, COPR, and SWR. While POR is always set during a Power-On Reset, EXTR will become set if the external reset pin is asserted or remains asserted after the Power-On Reset (POR) has deasserted.

Base + $1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	SWR	COPR	EXTR	POR	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0					0	0

Figure 6-3 SIM Reset Status Register (SIM_RSTAT)

6.3.2.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as zero and cannot be modified by writing.

6.3.2.2 Software Reset (SWR)—Bit 5

When set, this bit indicates that the previous system reset occurred as a result of a software reset (written 1 to SWRST bit in the SIM_CTRL register). It will not be set if a COP, external, or POR reset also occurred.

6.3.2.3 COP Reset (COPR)—Bit 4

When set, this bit indicates that the previous system reset was caused by the Computer Operating Properly

generation and SIM modules. All functionality is for test purposes only and is subject to unspecified latencies. Glitches may be produced when the clock is enabled or switched.

The lower four bits of the GPIO A register can function as GPIO, PWM, or as additional clock output signals. GPIO has priority and is enabled/disabled via the GPIOA_PEREN. If GPIOA[3:0] are programmed to operate as peripheral outputs, then the choice between PWM and additional clock outputs is done here in the CLKOUT. The default state is for the peripheral function of GPIOA[3:0] to be programmed as PWM. This can be changed by altering $\overline{\text{PWM3}}$ through $\overline{\text{PWM0}}$.

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	$\overline{\text{PWM3}}$	$\overline{\text{PWM2}}$	$\overline{\text{PWM1}}$	$\overline{\text{PWM0}}$	CLK DIS	CLKOSEL				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Figure 6-8 CLKO Select Register (SIM_CLKOUT)

6.3.7.1 Reserved—Bits 15–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.3.7.2 $\overline{\text{PWM3}}$—Bit 9

- 0 = Peripheral output function of GPIOA[3] is defined to be $\overline{\text{PWM3}}$
- 1 = Peripheral output function of GPIOA[3] is defined to be the Relaxation Oscillator Clock

6.3.7.3 $\overline{\text{PWM2}}$—Bit 8

- 0 = Peripheral output function of GPIOA[2] is defined to be $\overline{\text{PWM2}}$
- 1 = Peripheral output function of GPIOA[2] is defined to be the system clock

6.3.7.4 $\overline{\text{PWM1}}$—Bit 7

- 0 = Peripheral output function of GPIOA[1] is defined to be $\overline{\text{PWM1}}$
- 1 = Peripheral output function of GPIOA[1] is defined to be two times the rate of the system clock

6.3.7.5 $\overline{\text{PWM0}}$—Bit 6

- 0 = Peripheral output function of GPIOA[0] is defined to be $\overline{\text{PWM0}}$
- 1 = Peripheral output function of GPIOA[0] is defined to be three times the rate of the system clock

6.3.7.6 Clockout Disable (CLKDIS)—Bit 5

- 0 = CLKOUT output is enabled and will output the signal indicated by CLKOSEL
- 1 = CLKOUT is 0

6.3.7.7 Clockout Select (CLKOSEL)—Bits 4–0

Selects clock to be muxed out on the CLKO pin.

- 00000 = Reserved for factory test—Continuous system clock

6.3.8.1 Quad Timer Clock Rate (TCR)—Bit 15

This bit selects the clock speed for the Quad Timermodule.

- 0 = Quad Timer module clock rate equals system clock rate, to a maximum 32MHz (default)
- 1 = Quad Timer module clock rate equals three times system clock rate, to a maximum 96MHz

Note: This bit should only be changed while the TMR module's clock is disabled. See **Section 6.3.9**.

Note: High-speed clocking is only available when the PLL is being used.

Note: If the PWM sync signal pulse is used as input to Timer 3 (See SIM_CTRL: TC3_INP, **Section 6.3.1.7**), then the clocks of the Quad Timer and PWM must be related, as shown in **Table 6-2**.

6.3.8.2 PWM Clock Rate (PCR)—Bit 14

This bit selects the clock speed for the PWM module.

- 0 = PWM module clock rate equals system clock rate, to a maximum 32MHz (default)
- 1 = PWM module clock rate equals three times system clock rate, to a maximum 96MHz

Note: This bit should only be changed while the PWM module's clock is disabled. See **Section 6.3.9**.

Note: High-speed clocking is only available when the PLL is being used.

Note: If the PWM sync signal is used as input to Timer 3 (See SIM_CTRL: TC3_INP, **Section 6.3.1.7**), then the clocks of the Quad Timer and PWM must be related, as shown in **Table 6-2**.

Table 6-2 Allowable Quad Timer and PWM Clock Rates when Using PWM Reload Pulse

		Quad Timer	
Clock Speed		1X	3X
PWM	1X	OK	OK
	3X	NO	OK

6.3.8.3 Reserved—Bits 13–12

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.3.8.4 Configure GPIOB7 (CFG_B7)—Bit 11

This bit selects the alternate function for GPIOB7.

- 0 = TXD — SCI Transmit Data (default)
- 1 = SCL — I2C Serial Clock

6.3.8.5 Configure GPIOB6 (CFG_B6)—Bit 10

This bit selects the alternate function for GPIOB6.

Table 6-3 Clock Operation in Power-Down Modes (Continued)

Mode	Core Clocks	Peripheral Clocks	Description
Wait	Core and memory clocks disabled	Peripheral clocks enabled	Core executes WAIT instruction to enter this mode. Typically used for power-conscious applications. Possible recoveries from Wait mode to Run mode are: 1. Any interrupt 2. Executing a Debug mode entry command during the 56800E core JTAG interface 2. Any reset (POR, external, software, COP)
Stop	Master clock generation in the OCCS remains operational, but the SIM disables the generation of system and peripheral clocks.		Core executes STOP instruction to enter this mode. Possible recoveries from Stop mode to Run mode are: 1. Interrupt from Timer channels that have been configured to operate in Stop mode (TCx_SD) 2. Interrupt for SCI configured to operate in Stop mode (SCI_SD) 3. Low-voltage interrupt 4. Executing a Debug mode entry command using the 56800E core JTAG interface 5. Any reset (POR, external, software, COP)
Standby	The OCCS generates the 2X system clock at a reduced frequency (200kHz). The PLL and high speed peripheral clocks are disabled and the high-speed peripheral option is not available. System and peripheral clocks operate at 100kHz.		The user configures the OCCS and SIM to select the relaxation oscillator clock source (PRECS), shut down the PLL (PLLPD), put the relaxation oscillator in Standby mode (ROSB), and put the large regulator in Standby (LRSTDBY). The part is fully operational, but operating at a minimum frequency and power configuration. Recovery requires reversing the sequence used to enter this mode (allowing for PLL lock time).
Power-Down	Master clock generation in the OCCS is completely shut down. All system and peripheral clocks are disabled.		The user configures the OCCS and SIM to enter Standby mode as shown in the previous description, followed by powering down the oscillator (ROPD). The only possible recoveries from this mode are: 1. External Reset 2. Power-On Reset

The power modes provide additional means to disable clock domains, configure the voltage regulator, and configure clock generation to manage power utilization, as shown in **Table 6-3**. Run, Wait, and Stop modes provide means of enabling/disabling the peripheral and/or core clocking as a group. Stop disable controls are provided for selected peripherals in the control register so that these peripheral clocks can optionally continue to operate in Stop mode and generate interrupts which will return the part from Stop to Run mode. Standby mode provides normal operation but at very low speed and power utilization. It is possible to invoke Stop or Wait mode while in Standby mode for even greater levels of power reduction. A 200kHz clock external clock can optionally be used in Standby mode to produce the required Standby 100kHz system bus rate. Power-down mode, which selects the ROSC clock source but shuts it off, fully disables the part and minimizes its power utilization but is only recoverable via reset.

When the PLL is not selected and the system bus is operating at around 100kHz, the large regulator can be put into its Standby mode (LRSTDBY) to reduce the power utilization of that regulator.

All peripherals, except the COP/watchdog timer, run at the system clock (peripheral bus) frequency[1], which is the same as the main processor frequency in this architecture. The COP timer runs at MSTR_OSC / 1024. The maximum frequency of operation is SYS_CLK = 32MHz. The only exception is the Quad Timer and PWM, which can be configured to operate at three times the system bus rate using TCR and PCR controls, provided the PLL is active and selected.

6.6 Resets

The SIM supports four sources of reset, as shown in **Figure 6-15**. The two asynchronous sources are the external reset pin and the Power-On Reset (POR). The two synchronous sources are the software reset, which is generated within the SIM itself by writing the SIM_CTRL register in **Section 6.3.1**, and the COP reset. The SIM uses these to generate resets for the internal logic. These are outlined in **Table 6-4**. The first column lists the four primary resets which are calculated. The JTAG circuitry is reset by the Power-On Reset. Columns two through five indicate which reset sources trigger these reset signals. The last column provides additional detail.

Table 6-4 Primary System Resets

	Reset Sources				
Reset Signal	**POR**	**External**	**Software**	**COP**	**Comments**
EXTENDED_POR	X				Stretched version of $\overline{\text{POR}}$. Relevant 64 Relaxation Oscillator Clock cycles after $\overline{\text{POR}}$ deasserts.
CLKGEN_RST	X	X	X	X	Released 32 Relaxation Oscillator Clock cycles after all reset sources have released.
PERIP_RST	X	X	X	X	Releases 32 Relaxation Oscillator Clock cycles after the CLKGEN_$\overline{\text{RST}}$ is released.
CORE_RST	X	X	X	X	Releases 32 SYS_CLK periods after PERIP_$\overline{\text{RST}}$ is released.

Figure 6-15 provides a graphic illustration of the details in **Table 6-4**. Note that the POR_Delay blocks use the Relaxation Oscillator Clock as their time base since other system clocks are inactive during this phase of reset.

1. The Quad Timer and PWM modules can be operated at three times the IPBus clock frequency.

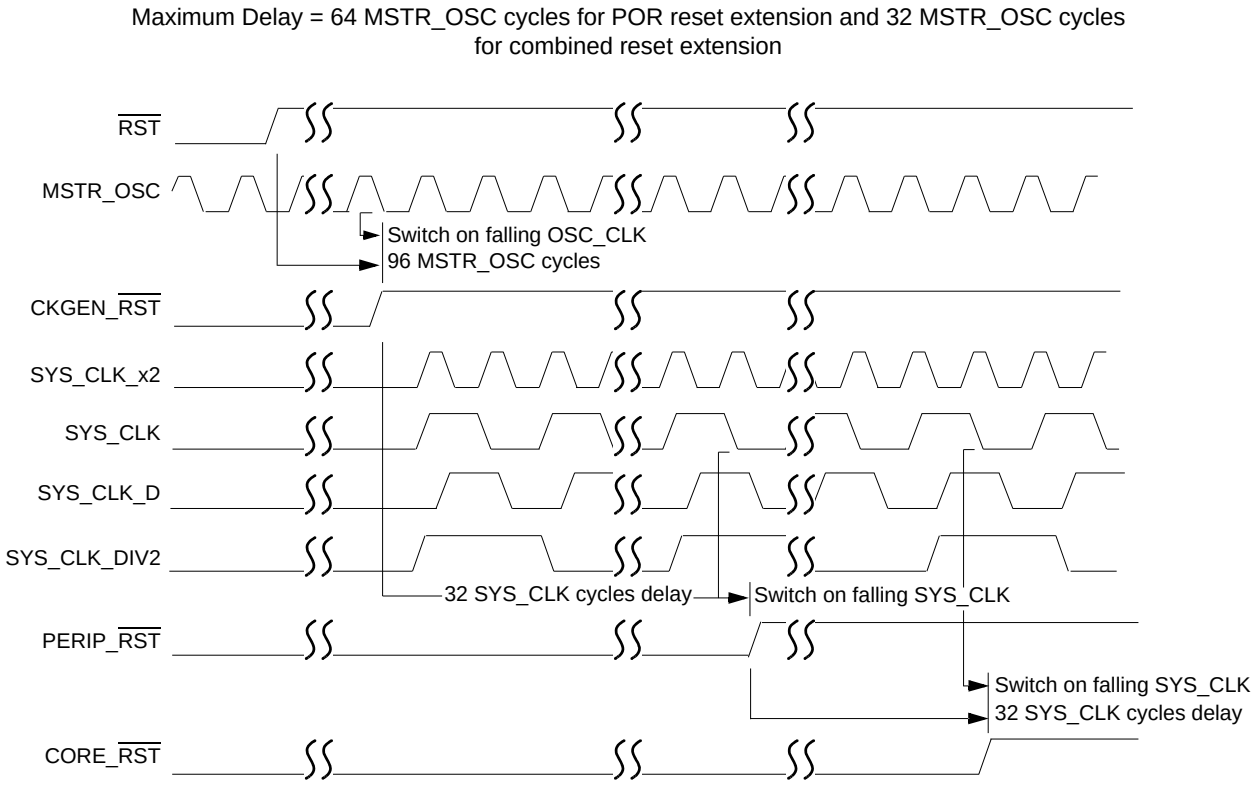

Figure 6-16 Timing Relationships of Reset Signal to Clocks

6.8 Interrupts

The SIM generates no interrupts.

Part 7 Security Features

The 56F8013/56F8011 offers security features intended to prevent unauthorized users from reading the contents of the flash memory (FM) array. The 56F8013/56F8011's flash security consists of several hardware interlocks that prevent unauthorized users from gaining access to the flash array.

After flash security is set, an authorized user is still able to access on-chip memory if the user purposely includes a subroutine to read and transfer the contents of internal memory via serial communication peripherals, as this code would defeat the purpose of security.

7.1 Operation with Security Enabled

After the user has programmed the flash with his application code, the 56F8013/56F8011 can be secured by programming a security word ($E70A) into program memory location $00 1FF7. This nonvolatile word will keep the device secured through reset and through power-down of the device. Refer to the flash

Add. Offset	Register Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	GPIOA_PUPEN	R	0	0	0	0	0	0	0	0	PU							
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$1	GPIOA_DATA	R	0	0	0	0	0	0	0	0	D							
		W																
		RS	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
$2	GPIOA_DDIR	R	0	0	0	0	0	0	0	0	DD							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3	GPIOA_PEREN	R	0	0	0	0	0	0	0	0	PE							
		W																
		RS	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
$4	GPIOA_IASSRT	R	0	0	0	0	0	0	0	0	IA							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$5	GPIOA_IEN	R	0	0	0	0	0	0	0	0	IEN							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$6	GPIOA_IEPOL	R	0	0	0	0	0	0	0	0	IEPOL							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$7	GPIOA_IPEND	R	0	0	0	0	0	0	0	0	IPR							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$8	GPIOA_IEDGE	R	0	0	0	0	0	0	0	0	IES							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$9	GPIOA_PPOUTM	R	0	0	0	0	0	0	0	0	OEN							
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$A	GPIOA_RDATA	R	0	0	0	0	0	0	0	0	RAW DATA							
		W																
		RS	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
$B	GPIOA_DRIVE	R	0	0	0	0	0	0	0	0	DRIVE							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R	0	Read as 0
W		Reserved
RS		Reset

Figure 8-1 GPIOA Register Map Summary

Table 10-7 Power-On Reset Low-Voltage Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Low-Voltage Interrupt for 3.3V supply[1]	$V_{EI3.3}$	2.58	2.7	—	V
Low-Voltage Interrupt for 2.5V supply[2]	$V_{E12.5}$	—	2.15	—	V
Low-Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power-On Reset[3]	POR	—	1.8	1.9	V

1. When V_{DD} drops below $V_{EI3.3}$, an interrupt is generated.
2. When V_{DD} drops below $V_{EI32.5}$, an interrupt is generated.
3. Power-On Reset occurs whenever the internally regulated 2.5V digital supply drops below 1.8V. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 2.15V or the 3.3V 1/O voltage is below 2.7V, no matter how long the ramp-up rate is. The internally regulated voltage is typically 100mV less than V_{DD} during ramp-up until 2.5V is reached, at which time it self-regulates.

10.2.1 Voltage Regulator Specifications

The 56F8013/56F8011 have two on-chip regulators. One supplies the PLL and relaxation oscillator. It has no external pins and therefore has no external characteristics which must be guaranteed (other than proper operation of the device). The second regulator supplies approximately 2.5V to the 56F8013/56F8011's core logic. This regulator requires an external 2.2μF, or greater, capacitor for proper operation. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator are shown in **Table 10-8**.

Table 10-8. Regulator Parameters

Characteristic	Symbol	Min	Typical	Max	Unit
Short Circuit Current	I_{SS}	—	450	650	mA
Short Circuit Tolerance (output shorted to ground)	T_{RSC}	—	—	30	Minutes

10.3 AC Electrical Characteristics

Tests are conducted using the input levels specified in **Table 10-5**. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in **Figure 10-2**.

10.12 Inter-Integrated Circuit Interface (I^2C) Timing

Table 10-17 I^2C Timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;\ STA}$	4.0		0.6		µs
LOW period of the SCL clock	t_{LOW}	4.7		1.25		µs
HIGH period of the SCL clock	t_{HIGH}	4.0		0.6		µs
Set-up time for a repeated START condition	$t_{SU;\ STA}$	4.7		0.6		µs
Data hold time for I^2C bus devices	$t_{HD;\ DAT}$	0[1]	3.45[2]	0[1]	0.9[2]	µs
Data set-up time	$t_{SU;\ DAT}$	250		100[3]		ns
Rise time of both SDA and SCL signals	t_r		1000	2 +0.1C_b[4]	300	ns
Fall time of both SDA and SCL signals	t_f		300	2 +0.1C_b[4]	300	ns
Set-up time for STOP condition	$t_{SU;\ STO}$	4.0		0.6		µs
Bus free time between STOP and START condition	t_{BUF}	4.7		1.3		µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0.0	50	ns

1. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
2. The maximum $t_{HD;\ DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. A Fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement $t_{SU;\ DAT}$ > = 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + $t_{SU;\ DAT}$ = 1000 + 250 = 1250ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
4. C_b = total capacitance of the one bus line in pF.

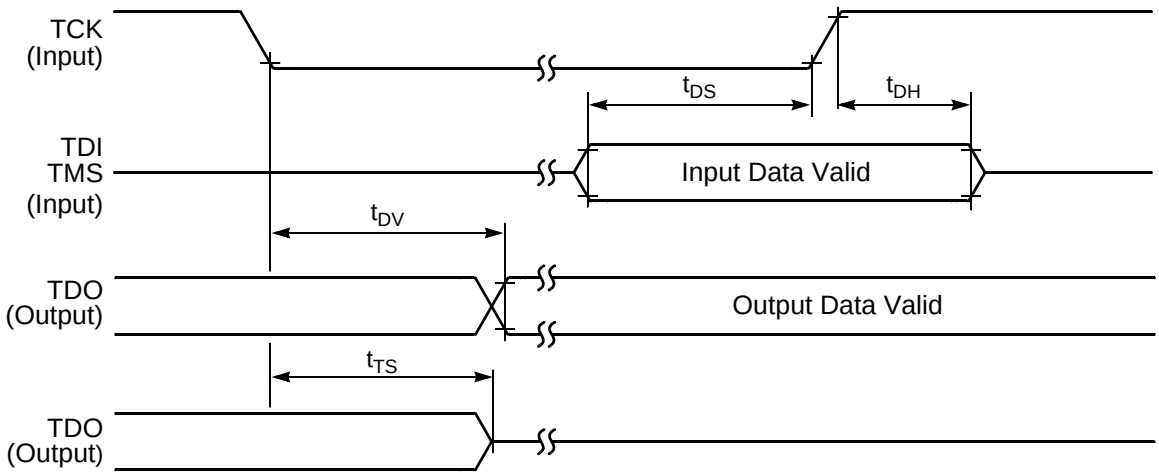

Figure 10-16 Test Access Port Timing Diagram

Table 11-1 56F8013/56F8011 32-Pin LQFP Package Identification by Pin Number[1]

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	**GPIOB6** *RXD,SDA,CLKIN*	9	**V_{SSA}**	17	**GPIOB2** *MISO,T2*	25	**V_{CAP}**
2	**GPIOB1** *$\overline{SS}$,SDA*	10	**ANA2** *V_{REFH},GPIOC2*	18	**GPIOA6** *FAULT0*	26	**V_{DD}**
3	**GPIOB7** *TXD,SCL*	11	**ANA1** *GPIOC1*	19	**GPIOB4** *T0,CLKO*	27	**V_{SS}**
4	**GPIOB5** *T1,FAULT3*	12	**ANA0** *GPIOC0*	20	**GPIOA5** *PWM5,FAULT2,T3*	28	**GPIOA1** *PWM1*
5	**ANB0** *GPIOC4*	13	**V_{SS}**	21	**GPIOB0** *SCLK,SCL*	28	**GPIOA0** *PWM0*
6	**ANB1** *GPIOC5*	14	**TCK** *GPIOD2*	22	**GPIOA4** *PWM4,FAULT1,T2*	30	**TDI** *GPIOD0*
7	**ANB2** *V_{REFL},GPIOC6*	15	**$\overline{RESET}$** *GPIOA7*	23	**GPIOA2** *PWM2*	31	**TMS** *GPIOD3*
8	**V_{DDA}**	16	**GPIOB3** *MOSI,T3*	24	**GPIOA3** *PWM3*	32	**TDO** *GPIOD1*

1.Alternate signals are in iltalic

Part 13 Ordering Information

Table 13-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 13-1 56F8013/56F8011 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Ambient Temperature Range	Order Number
MC56F8013	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	32	32	–40° to + 125°C	MC56F8013MFAE*
MC56F8013	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	32	32	–40° to + 125°C	S568013MFA00E*
MC56F8013	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	32	32	–40° to + 105°C	MC56F8013VFAE*
MC56F8011	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	32	32	–40° to + 105°C	MC56F8011VFAE*

*This package is RoHS compliant.

Part 14 Appendix

Register acronyms are revised from previous device data sheets to provide a cleaner register description. A cross reference to legacy and revised acronyms are provided in the following table.

Module	Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
		New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
ADC	Control Register 1	CTRL1	ADCR1	ADC_CTRL1	ADC_ADCR1	ADC_ADCR1	0xF080	
	Control Register 2	CTRL2	ADCR2	ADC_CTRL2	ADC_ADCR2	ADC_ADCR2	0xF081	
	Zero Crossing Control Register	ZXCTRL	ADZCC	ADC_ZXCTRL	ADC_ADZCC	ADC_ADZCC	0xF082	
	Channel List Register 1	CLIST1	ADLST1	ADC_CLIST1	ADC_ADLST1	ADC_ADLST1	0xF083	
	Channel List Register 2	CLIST2	ADLST2	ADC_CLIST2	ADC_ADLST2	ADC_ADLST2	0xF084	
	Sample Disable Register	SDIS	ADSDIS	ADC_SDIS	ADC_ADSDIS	ADC_ADSDIS	0xF085	
	Status Register	STAT	ADSTAT	ADC_STAT	ADC_ADSTAT	ADC_ADSTAT	0xF086	
	Limit Status Register	LIMSTAT	ADLSTAT	ADC_LIMSTAT	ADC_ADLSTAT	ADC_ADLSTAT	0xF087	
	Zero Crossing Status Register	ZXSTAT	ADZCSTAT	ADC_ZXSTAT	ADC_ADZCSTAT	ADC_ADZCSTAT	0xF088	
	Result Registers 0-7	RSLT0-7	ADRSLT0-7	ADC_RSLT0-7	ADC_ADRSLT0-7	ADC_ADRSLT0-7	0xF089	0XF090
	Low Limit Registers 0-7	LOLIM0-7	ADLLMT0-7	ADC_LOLIM0-7	ADC_ADLLMT0-7	ADC_ADLLMT0-7	0XF091	0XF098
	High Limit Registers 0-7	HILIM0-7	ADHLMT0-7	ADC_HILIM0-7	ADC_ADHLMT0-7	ADC_ADHLMT0-7	0XF099	0XF0A0
	Offset Registers 0-7	OFFST0-7	ADOFS0-7	ADC_OFFST0-7	ADC_ADOFS0-7	ADC_ADOFS0-7	0XF0A1	0XF0A8
	Power Control Register	PWR	ADPOWER	ADC_PWR	ADC_ADPOWER	ADC_ADPOWER	0XF0A9	
	Voltage Reference Register	CAL	ADCAL	ADC_VREF	ADC_ADCAL	ADC_CAL	0XF0AA	
COP	Control Register	CTRL	COPCTL	COP_CTRL	COPCTL	COPCTL	0XF0E0	
	Time-Out Register	TOUT	COPTO	COP_TOUT	COPTO	COPTO	0XF0E1	
	Counter Register	CNTR	COPCTR	COP_CNTR	COPCTR	COPCTR	0XF0E2	
I^2C	Address Register	ADDR	IBAD	I2C_ADDR	I2C_IBAD	IBAD	0xF0D0	
	Frequency Divider Register	FDIV	IBFD	I2C_FDIV	I2C_IBFD	IBFD	0xF0D1	
	Control Register	CTRL	IBCR	I2C_CTRL	I2C_IBCR	IBCR	0xF0D2	