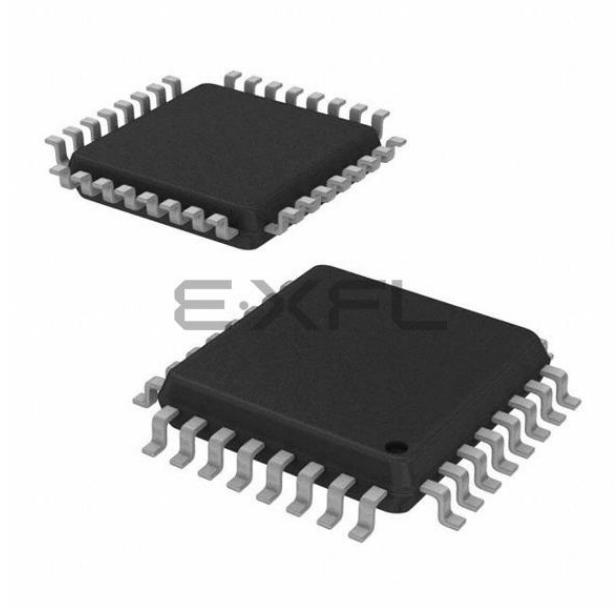

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	26
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8013vfaer2

56F8013/56F8011 Data Sheet Table of Contents

— Timer2 output can be used to drive PWM 2 and 3

— Timer3 output can be used to drive PWM 4 and 5

- ADC conversion result:
  - — Signal of Over/Under limit of ADC sample 0 can be used to drive PWM 0 and 1
  - — Signal of Over/Under limit of ADC sample 1 can be used to drive PWM 2 and 3
  - — Signal of Over/Under limit of ADC sample 2 can be used to drive PWM 4 and 5

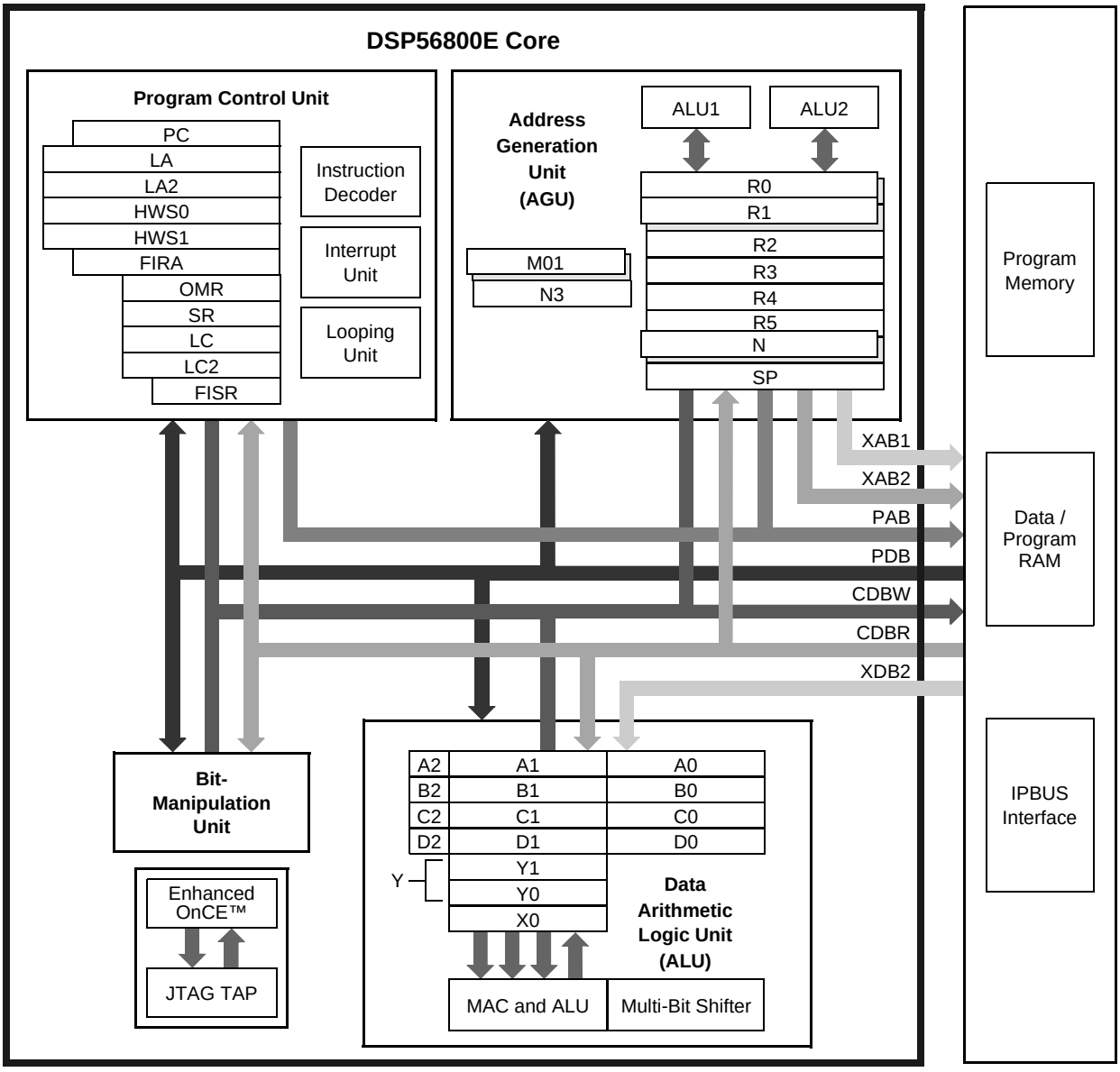

Figure 1-1 56800E Core Block Diagram

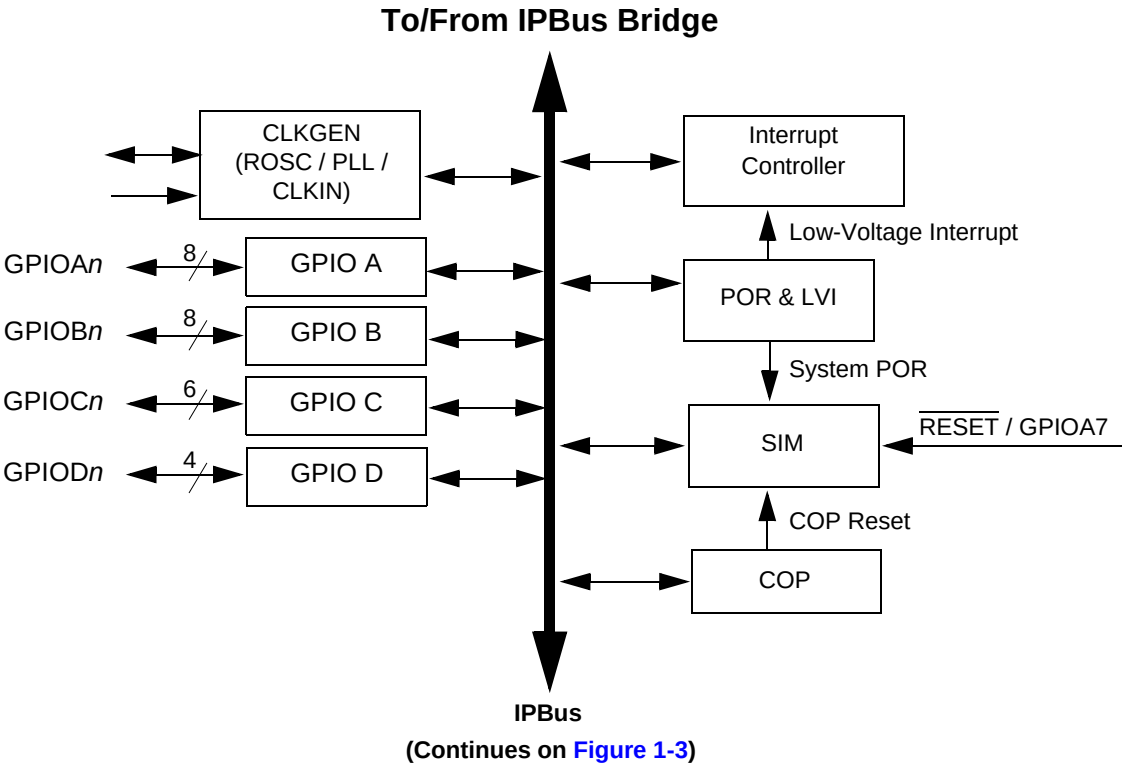

Figure 1-2 Peripheral Subsystem

(Continued from Figure 1-2)

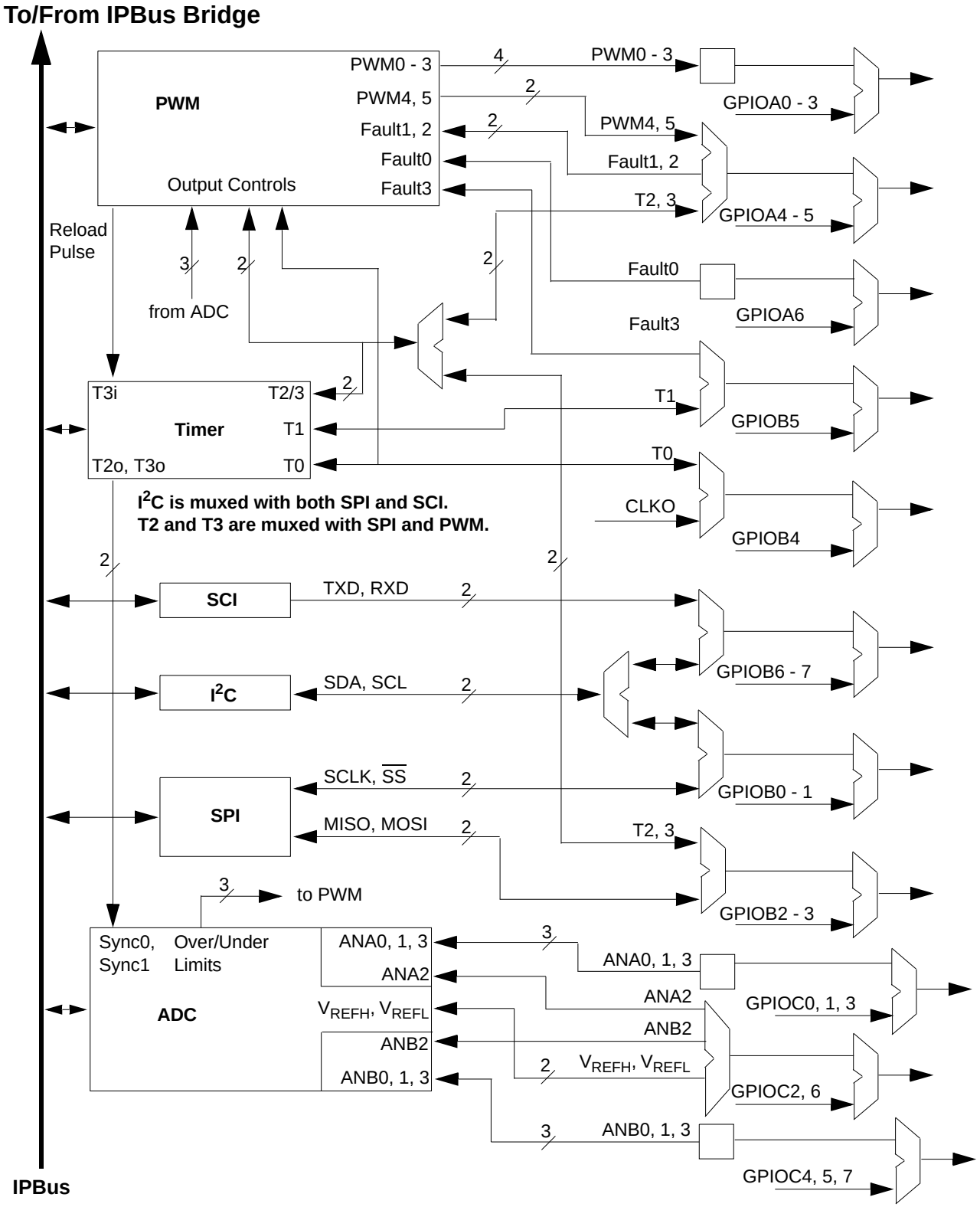

Figure 1-3 56F8013/56F8011 Peripheral I/O Pin-Out

1.7 Product Documentation

The documents listed in **Table 1-2** are required for a complete description and proper design with the 56F8013 or 56F8011. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at:
http://www.freescale.com

Table 1-2 56F8013/56F8011 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit Digital Signal Controller core processor, and the instruction set	DSP56800ERM
56F801X Peripheral Reference Manual	Detailed description of peripherals of the 56F801X family of devices	MC56F8000RM
56F801X Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F801x family of devices	56F801XBLUG
56F8013/56F8011 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8013
Errata	Details any chip issues that might be present	MC56F8013E MC56F8011E

1.8 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
“asserted”	A high true (active high) signal is high or a low true (active low) signal is low.
“deasserted”	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

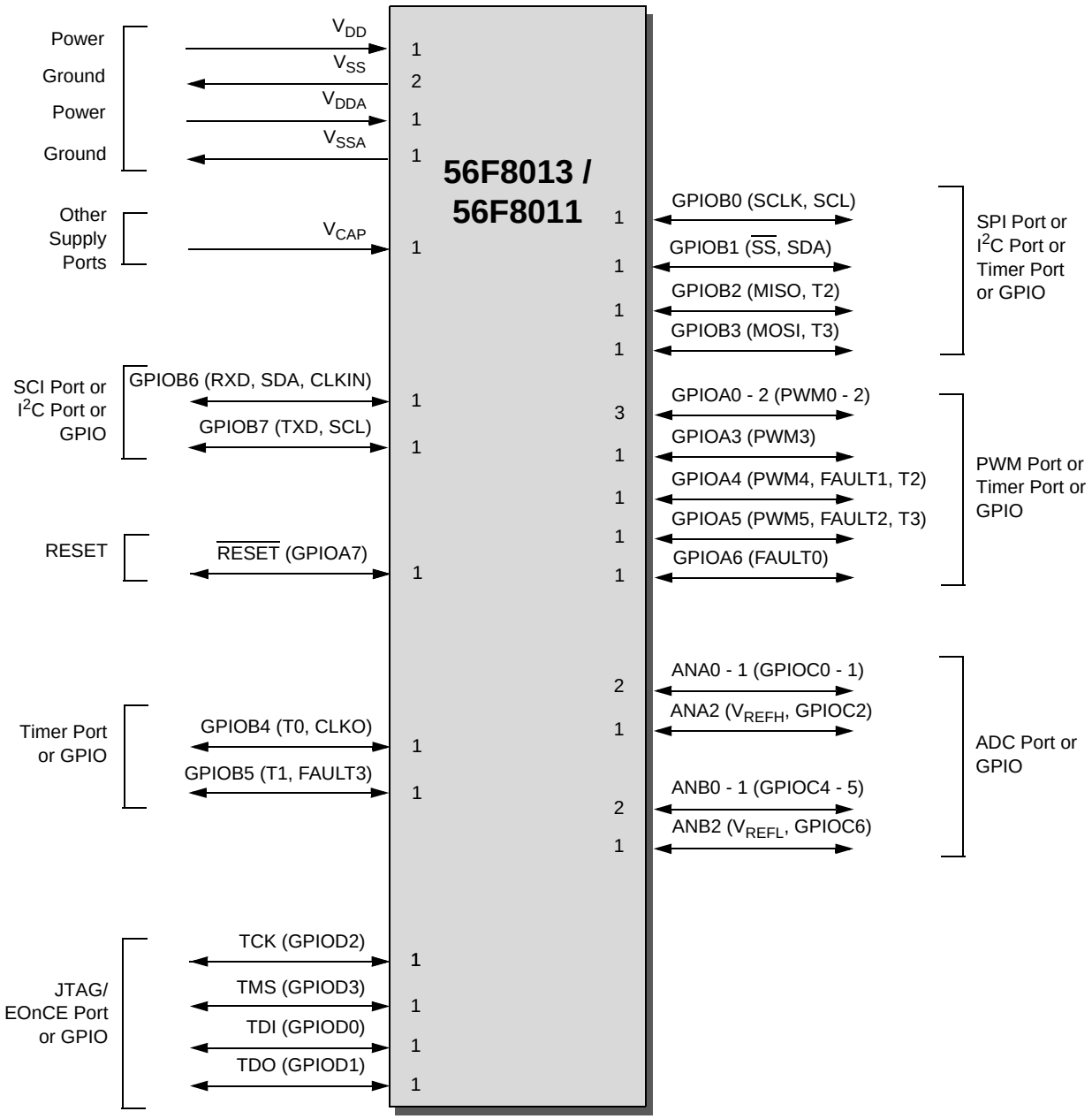

Figure 2-1 56F8013/56F8011 Signals Identified by Functional Group

Table 2-3 56F8013/56F8011 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
TDO	32	Output	Output	**Test Data Output** — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK.
(GPIOD1)		Input/ Output		**Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDO.
GPIOB0	21	Input/ Output	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(SCLK)		Input/ Output		**SPI Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. A Schmitt trigger input is used for noise immunity.
(SCL[3])		Input/ Output		**Serial Data** — This pin serves as the I^2C serial clock. After reset, the default state is GPIOB0. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.
3. This signal is also brought out on the GPIOB7 pin.				
GPIOB1	2	Input/ Output	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
($\overline{SS}$)		Input		**SPI Slave Select** — $\overline{SS}$ is used in slave mode to indicate to the SPI module that the current transfer is to be received.
(SDA[4])		Input/ Output		**Serial Clock** — This pin serves as the I^2C serial data line. After reset, the default state is GPIOB1. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.
4. This signal is also brought out on the GPIOB6 pin.				

Return to Table 2-2

Table 2-3 56F8013/56F8011 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOA5	20	Input/ Output	Input with internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(PWM5)		Output		**PWM5** — This is one of the six PWM output pins.
(FAULT2)		Input		**Fault2** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip.
(T3[8])		Input/ Output		**T3** — Timer, Channel 3 After reset, the default state is GPIOA5. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.
8. This signal is also brought out on the GPIOB3 pin.				
GPIOA6	18	Input/ Output	Input with internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(FAULT0)		Input		**Fault0** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip. After reset, the default state is GPIOA6.
ANA0	12	Input	Analog Input	**ANA0** — Analog input to ADC A, channel 0
(GPIOC0)		Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is ANA0.
ANA1	11	Input	Analog Input	**ANA1** — Analog input to ADC A, channel 1
(GPIOC1)		Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is ANA1.

Return to Table 2-2

Table 4-2 Interrupt Vector Table Contents[1]

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
core			P:$00	Reserved for Reset Overlay[2]
core			P:$02	Reserved for COP Reset Overlay
core	2	3	P:$04	Illegal Instruction
core	3	3	P:$06	SW Interrupt 3
core	4	3	P:$08	HW Stack Overflow
core	5	3	P:$0A	Misaligned Long Word Access
core	6	1-3	P:$0C	EOnCE Step Counter
core	7	1-3	P:$0E	EOnCE Breakpoint Unit 0
core	8	1-3	P:$10	EOnCE Trace Buffer
core	9	1-3	P:$12	EOnCE Transmit Register Empty
core	10	1-3	P:$14	EOnCE Receive Register Full
core	11	2	P:$16	SW Interrupt 2
core	12	1	P:$18	SW Interrupt 1
core	13	0	P:$1A	SW Interrupt 0
	14			Reserved
	15			Reserved
PS	16	0-2	P:$20	Power Sense
OCCS	17	0-2	P:$22	PLL Lock, Loss of Clock Reference Interrupt
FM	18	0-2	P:$24	FM Access Error Interrupt
FM	19	0-2	P:$26	FM Command Complete
FM	20	0-2	P:$28	FM Command, data and address Buffers Empty
	21			Reserved
GPIOD	22	0-2	P:$2C	GPIOD
GPIOC	23	0-2	P:$2E	GPIOC
GPIOB	24	0-2	P:$30	GPIOB
GPIOA	25	0-2	P:$32	GPIOA
SPI	26	0-2	P:$34	SPI Receiver Full / Error
SPI	27	0-2	P:$36	SPI Transmitter Empty
SCI	28	0-2	P:$38	SCI Transmitter Empty
SCI	29	0-2	P:$3A	SCI Transmitter Idle
SCI	30	0-2	P:$3C	SCI Reserved
SCI	31	0-2	P:$3E	SCI Receiver Error
SCI	32	0-2	P:$40	SCI Receiver Full
	33, 34			Reserved
I^2C	35	0-2	P:$46	I^2C
Timer	36	0-2	P:$48	Timer Channel 0
Timer	37	0-2	P:$4A	Timer Channel 1

(Continues next page)

Table 4-2 Interrupt Vector Table Contents[1] (Continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
Timer	38	0-2	P:$4C	Timer Channel 2
Timer	39	0-2	P:$4E	Timer Channel 3
ADC	40	0-2	P:$50	ADCA Conversion Complete
ADC	41	0-2	P:$52	ADCB Conversion Complete
ADC	42	0-2	P:$54	ADC Zero Crossing or Limit Error
PWM	43	0-2	P:$56	Reload PWM
PWM	44	0-2	P:$58	PWM Fault
SWILP	45	-1	P:$5A	SW Interrupt Low Priority

1. Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.
2. If the VBA is set to the reset value, the first two locations of the vector table will overlay the chip reset addresses.

4.3 Program Map

The Program Memory map is shown in **Table 4-3**.

Table 4-3 Program Memory Map for 56F8013[1]

Begin/End Address	Memory Allocation
P: $FF FFFF P: $00 8800	RESERVED
P: $00 87FF P: $00 8000	On-Chip RAM[2] 4KB
P: $00 7FFF P: $00 2000	RESERVED
P: $00 1FFF P: $00 0000	Internal Program Flash 16KB Cop Reset Address = $00 0002 Boot Location = $00 0000

1. All addresses are 16-bit Word addresses.
2. This RAM is shared with Data space starting at address X: $00 0000; see **Figure 4-1**.

Table 4-10 Pulse Width Modulator Registers Address Map (PWM_BASE = $00 F040)

Register Acronym	Address Offset	Register Description
PWM_CTRL	$0	Control Register
PWM_FCTRL	$1	Fault Control Register
PWM_FLTACK	$2	Fault Status Acknowledge Register
PWM_OUT	$3	Output Control Register
PWM_CNTR	$4	Counter Register
PWM_CMOD	$5	Counter Modulo Register
PWM_VAL0	$6	Value Register 0
PWM_VAL1	$7	Value Register 1
PWM_VAL2	$8	Value Register 2
PWM_VAL3	$9	Value Register 3
PWM_VAL4	$A	Value Register 4
PWM_VAL5	$B	Value Register 5
PWM_DTIM0	$C	Dead Time Register 0
PWM_DTIM1	$D	Dead Time Register 1
PWM_DMAP1	$E	Disable Mapping Register 1
PWM_DMAP2	$F	Disable Mapping Register 2
PWM_CNFG	$10	Configure Register
PWM_CCTRL	$11	Channel Control Register
PWM_PORT	$12	Port Register
PWM_ICCTRL	$13	Internal Correction Control Register
PWM_SCTRL	$14	Source Control Register

Table 4-11 Interrupt Control Registers Address Map (ITCN_BASE = $00 F060)

Register Acronym	Address Offset	Register Description
ITCN_IPR0	$0	Interrupt Priority Register 0
ITCN_IPR1	$1	Interrupt Priority Register 1
ITCN_IPR2	$2	Interrupt Priority Register 2
ITCN_IPR3	$3	Interrupt Priority Register 3
ITCN_IPR4	$4	Interrupt Priority Register 4
ITCN_VBA	$5	Vector Base Address Register
ITCN_FIM0	$6	Fast Interrupt Match 0 Register
ITCN_FIVAL0	$7	Fast Interrupt Vector Address Low 0 Register
ITCN_FIVAH0	$8	Fast Interrupt Vector Address High 0 Register
ITCN_FIM1	$9	Fast Interrupt Match 1 Register

5.5.3.4 SCI Transmitter Idle Interrupt Priority Level (SCI_TIDL IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.5.3.5 SCI Transmitter Empty Interrupt Priority Level (SCI_XMIT IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.5.3.6 SPI Transmitter Empty Interrupt Priority Level (SPI_XMIT IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.5.3.7 SPI Receiver Full Interrupt Priority Level (SPI_RCV IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

6.3.5 Least Significant Half of JTAG ID (SIM_LSHID)

This read-only register displays the least significant half of the JTAG ID for the chip. This register reads $401D.

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1
Write																
RESET	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1

Figure 6-6 Least Significant Half of JTAG ID (SIM_LSHID)

6.3.6 SIM Power Control Register (SIM_PWR)

This register controls the Standby mode of the large regulator. The large regulator derives the core digital logic power supply from the IO power supply. In some circumstances, the large regulator may be put in a reduced-power Standby mode without interfering with part operation. Refer to the overview of power-down modes and the overview of clock generation for more information on the use of large regulator standby.

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LRSTDBY	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-7 SIM Power Control Register (SIM_PWR)

6.3.6.1 Reserved—Bits 15–2

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.3.6.2 Large Regulator Standby Mode[1:0] (LRSTDBY)—Bits 1–0

This bit controls the pull-up resistors on the IRQA pin.

- 00 = Large regulator is in Normal mode
- 01 = Large regulator is in Standby (reduced-power) mode
- 10 = Large regulator is in Normal mode and the LRSTDBY field is write-protected until the next reset
- 11 = Large regulator is in Standby mode and the LRSTDBY field is write-protected until the next reset

NOTE:

Standby mode can be used when device operates below 200KHz with PLL shut down.

6.3.7 CLKO Select Register (SIM_CLKOUT)

The CLKO select register can be used to multiplex out selected clocks generated inside the clock

Add. Offset	Register Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	GPIOC_PUPEN	R	0	0	0	0	0	0	0	0	PU							
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$1	GPIOC_DATA	R	0	0	0	0	0	0	0	0	D							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$2	GPIOC_DDIR	R	0	0	0	0	0	0	0	0	DD							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3	GPIOC_PEREN	R	0	0	0	0	0	0	0	0	PE							
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$4	GPIOC_IASSRT	R	0	0	0	0	0	0	0	0	IA							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$5	GPIOC_IEN	R	0	0	0	0	0	0	0	0	IEN							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$6	GPIOC_IEPOL	R	0	0	0	0	0	0	0	0	IEPOL							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$7	GPIOC_IPEND	R	0	0	0	0	0	0	0	0	IPR							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$8	GPIOC_IEDGE	R	0	0	0	0	0	0	0	0	IES							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$9	GPIOC_PPOUTM	R	0	0	0	0	0	0	0	0	OEN							
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$A	GPIOC_RDATA	R	0	0	0	0	0	0	0	0	RAW DATA							
		W																
		RS	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
$B	GPIOC_DRIVE	R	0	0	0	0	0	0	0	0	DRIVE							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R	0	Read as 0
W		Reserved
RS		Reset

Figure 8-3 GPIOC Register Map Summary

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Pin Group 2: $\overline{\text{RESET}}$, GPIOA7

Pin Group 3: ADC Analog Inputs

10.1.1 ElectroStatic Discharge (ESD) Model

Table 10-2 56F8013/56F8011 ESD Protection

Characteristic	Min	Typ	Max	Unit
ESD for Human Body Model (HBM)	2000	—	—	V
ESD for Machine Model (MM)	200	—	—	V
ESD for Charge Device Model (CDM)	750	—	—	V

Table 10-3 LQFP Package Thermal Characteristics[6]

Characteristic	Comments	Symbol	Value (LQFP)	Unit	Notes
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	74	°C/W	1,2
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	50	°C/W	1,3
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	67	°C/W	1,3
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	46	°C/W	1,3
Junction to board		$R_{\theta JB}$	23	°C/W	4
Junction to case		$R_{\theta JC}$	20	°C/W	5
Junction to package top	Natural Convection	Ψ_{JT}	4	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESC51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. See **Section 12.1** for more details on thermal design considerations.

Table 10-4 Recommended Operating Conditions

(V_{REFL} = 0V, V_{SSA} = 0V, V_{SS} = 0V)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Supply voltage	V_{DD}		3	3.3	3.6	V
ADC Supply voltage	V_{DDA}		3	3.3	3.6	V
ADC High Voltage Reference	V_{REFH}		3	—	V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.1	0	0.1	V
Device Clock Frequency Using relaxation oscillator Using external clock source	FSYSCLK		 8 0	—	 32 32	MHz
Input Voltage High (digital inputs)	V_{IH}	Pin Groups 1, 2	2	—	5.5	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2	-0.3	—	0.8	V
Output Source Current High (at V_{OH} min.) When programmed for low drive strength When programmed for high drive strength	I_{OH}	 Pin Group 1 Pin Group 1	 — —	 — —	 -4 -8	mA
Output Source Current Low (at V_{OL} max.) When programmed for low drive strength When programmed for high drive strength	I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —	 — —	 4 8	mA
Ambient Operating Temperature (Automotive)	T_A		-40	—	125	°C
Ambient Operating Temperature (Industrial)	T_A		-40	—	105	°C
Flash Endurance (Program Erase Cycles)	N_F	T_A = -40°C to 105°C	10,000	—	—	Cycles
Flash Data Retention	T_R	T_J <= 85°C avg	15	—	—	Years
Flash Data Retention with <100 Program/Erase Cycles	t_{FLRET}	T_J <= 85°C avg	20	—	—	Years

Note: Total chip source or sink current cannot exceed 50mA

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Pin Group 2: $\overline{\text{RESET}}$, GPIOA7

Pin Group 3: ADC analog inputs

10.2 DC Electrical Characteristics

Table 10-5 DC Electrical Characteristics
At Recommended Operating Conditions

Characteristic	Symbol	Notes	Min	Typ	Max	Unit	Test Conditions
Output Voltage High	V_{OH}	Pin Group 1	2.4	—	—	V	$I_{OH} = I_{OHmax}$
Output Voltage Low	V_{OL}	Pin Groups 1, 2	—	—	0.4	V	$I_{OL} = I_{OLmax}$
Digital Input Current High pull-up enabled or disabled[1]	I_{IH}	Pin Groups 1, 2	—	0	+/- 2.5	µA	V_{IN} = 2.4V to 5.5V
Digital Input Current Low pull-up enabled pull-up disabled[1]	I_{IL}	Pin Groups 1, 2	 -15 —	 -30 0	 -60 +/- 2.5	µA	V_{IN} = 0V
Output Current High Impedance State[1]	I_{OZ}	Pin Groups 1, 2	—	0	+/- 2.5	µA	V_{OUT} = 2.4V to 5.5V or 0V
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 2	—	0.35	—	V	—
Input Capacitance	C_{IN}		—	10	—	pF	—
Output Capacitance	C_{OUT}		—	10	—	pF	—

1. See **Figure 10-1**

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Pin Group 2: $\overline{\text{RESET}}$, GPIOA7

Pin Group 3: ADC Analog Inputs

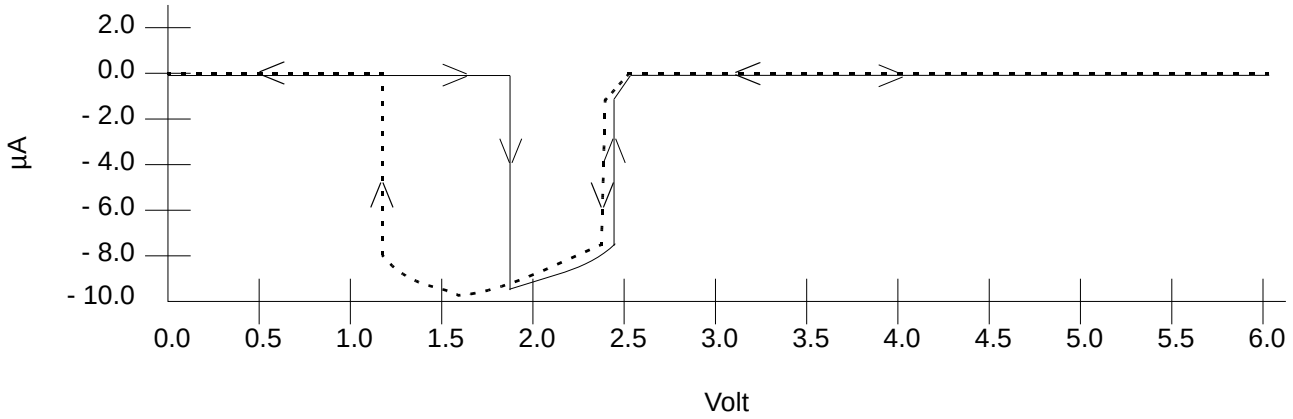

Figure 10-1 I_{IN}/I_{OZ} vs. V_{IN} (Typical; Pull-Up Disabled)

Table 10-7 Power-On Reset Low-Voltage Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Low-Voltage Interrupt for 3.3V supply[1]	$V_{EI3.3}$	2.58	2.7	—	V
Low-Voltage Interrupt for 2.5V supply[2]	$V_{E12.5}$	—	2.15	—	V
Low-Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power-On Reset[3]	POR	—	1.8	1.9	V

1. When V_{DD} drops below $V_{EI3.3}$, an interrupt is generated.
2. When V_{DD} drops below $V_{EI32.5}$, an interrupt is generated.
3. Power-On Reset occurs whenever the internally regulated 2.5V digital supply drops below 1.8V. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 2.15V or the 3.3V 1/O voltage is below 2.7V, no matter how long the ramp-up rate is. The internally regulated voltage is typically 100mV less than V_{DD} during ramp-up until 2.5V is reached, at which time it self-regulates.

10.2.1 Voltage Regulator Specifications

The 56F8013/56F8011 have two on-chip regulators. One supplies the PLL and relaxation oscillator. It has no external pins and therefore has no external characteristics which must be guaranteed (other than proper operation of the device). The second regulator supplies approximately 2.5V to the 56F8013/56F8011's core logic. This regulator requires an external 2.2μF, or greater, capacitor for proper operation. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator are shown in **Table 10-8**.

Table 10-8. Regulator Parameters

Characteristic	Symbol	Min	Typical	Max	Unit
Short Circuit Current	I_{SS}	—	450	650	mA
Short Circuit Tolerance (output shorted to ground)	T_{RSC}	—	—	30	Minutes

10.3 AC Electrical Characteristics

Tests are conducted using the input levels specified in **Table 10-5**. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in **Figure 10-2**.

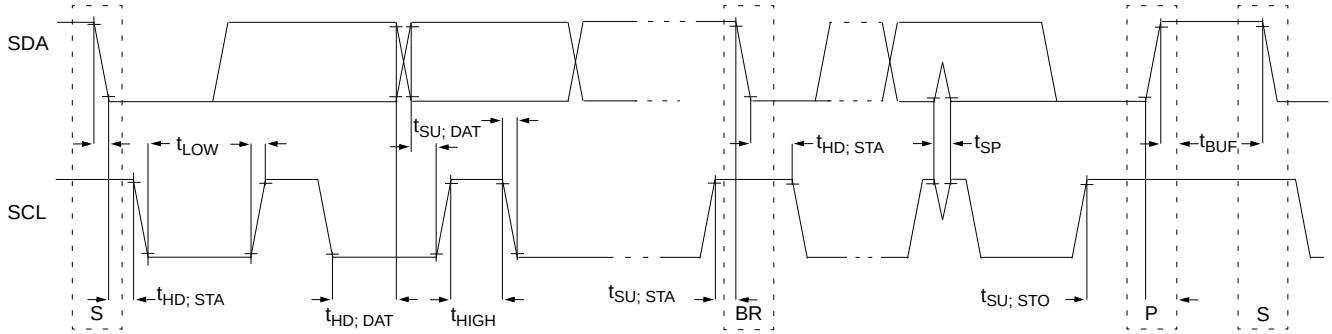

Figure 10-14 Timing Definition for Fast and Standard Mode Devices on the I^2C Bus

10.13 JTAG Timing

Table 10-18 JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation[1]	f_{OP}	DC	SYS_CLK/8	MHz	10-15
TCK clock pulse width	t_{PW}	50	—	ns	10-15
TMS, TDI data set-up time	t_{DS}	5	—	ns	10-16
TMS, TDI data hold time	t_{DH}	5	—	ns	10-16
TCK low to TDO data valid	t_{DV}	—	30	ns	10-16
TCK low to TDO tri-state	t_{TS}	—	30	ns	10-16

1. TCK frequency of operation must be less than 1/8 the processor rate.

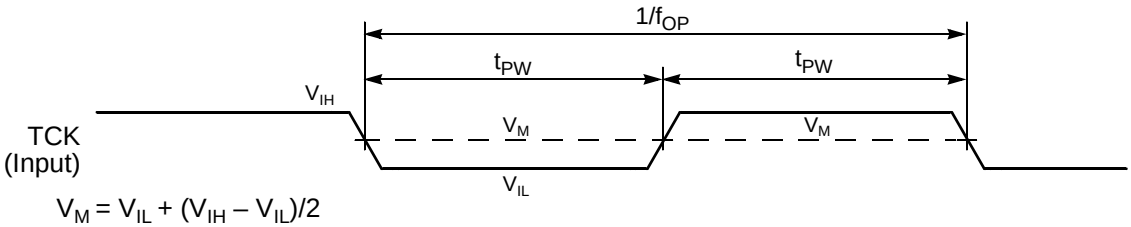

Figure 10-15 Test Clock Input Timing Diagram

5. LSB = Least Significant Bit = 0.806mV
6. Pin groups are detailed following **Table 10-1**.
7. For device S56F8013MFA00E, input leakage current is ± 1μA.
8. The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC.

10.15 Equivalent Circuit for ADC Inputs

Figure 10-17 illustrates the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed & S3 is open, one input of the sample and hold circuit moves to $(V_{REFH}\text{-}V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH}\text{-}V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). Note that there are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase.

One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.