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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, SD, SPI, UART/USART
Peripherals	DMA, I ² S, LCD, LVD, POR, PWM, WDT
Number of I/O	70
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 38x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mk30dx128vll7

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: PK30 and MK30.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	 M = Fully qualified, general market flow P = Prequalification
K##	Kinetis family	• K30
A	Key attribute	 D = Cortex-M4 w/ DSP F = Cortex-M4 w/ DSP and FPU
Μ	Flash memory type	 N = Program flash only X = Program flash and FlexMemory

Table continues on the next page...

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- Operating ratings apply during operation of the chip.
- Handling ratings apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	-0.3	1.2	V

3.5 Result of exceeding a rating



Terminology and guidelines



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level		3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	-0.3	3.8	V

Table continues on the next page ...



Figure 3. VLPR mode supply current vs. core frequency

5.2.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- 1. Go to www.freescale.com.
- 2. Perform a keyword search for "EMC design."

5.2.7 Capacitance attributes

Table 7. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C _{IN_A}	Input capacitance: analog pins	—	7	pF
C _{IN_D}	Input capacitance: digital pins		7	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
	Normal run mode	e			
f _{SYS}	System and core clock	_	72	MHz	
f _{BUS}	Bus clock	_	50	MHz	
f _{FLASH}	Flash clock	_	25	MHz	
f _{LPTMR}	LPTMR clock	_	25	MHz	
	VLPR mode ¹				
f _{SYS}	System and core clock	_	4	MHz	
f _{BUS}	Bus clock	_	4	MHz	
f _{FLASH}	Flash clock	_	0.5	MHz	
f _{ERCLK}	External reference clock	_	16	MHz	
f _{LPTMR_pin}	LPTMR clock	_	25	MHz	
f _{LPTMR_ERCLK}	LPTMR external reference clock	_	16	MHz	
f _{FlexCAN_ERCLK}	FlexCAN external reference clock	_	8	MHz	
f _{I2S_MCLK}	I2S master clock	_	12.5	MHz	
f _{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, CMT, and I²C signals.

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	_	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	_	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	16	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100		ns	3

Table 9. General switching specifications

Table continues on the next page...

6.1 Core modules

6.1.1 Debug trace timing specifications

 Table 11. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T _{cyc}	Clock period	Frequency	MHz	
T _{wl}	Low pulse width	2		ns
T _{wh}	High pulse width	2		ns
Tr	Clock and data rise time	—	3	ns
T _f	Clock and data fall time		3	ns
T _s	Data setup	3	_	ns
T _h	Data hold	2	_	ns



Figure 4. TRACE_CLKOUT specifications



Figure 5. Trace data specifications

6.3.1 MCG specifications Table 14. MCG specifications

Symbol	Description		Min.	Тур.	Max.	Unit	Notes
f _{ints_ft}	Internal reference factory trimmed at	frequency (slow clock) — nominal VDD and 25 °C	_	32.768	—	kHz	
f _{ints_t}	Internal reference trimmed	frequency (slow clock) — user	31.25	_	39.0625	kHz	
$\Delta_{fdco_res_t}$	Resolution of trimr frequency at fixed using SCTRIM and	ned average DCO output voltage and temperature — d SCFTRIM	_	± 0.3	± 0.6	%f _{dco}	1
$\Delta f_{dco_res_t}$	Resolution of trimr frequency at fixed using SCTRIM onl	ned average DCO output voltage and temperature — y	_	± 0.2	± 0.5	%f _{dco}	1
Δf_{dco_t}	Total deviation of t frequency over vol	rimmed average DCO output tage and temperature	—	+0.5/-0.7	—	%f _{dco}	1
Δf _{dco_t}	Total deviation of t frequency over fixe range of 0–70°C	rimmed average DCO output ed voltage and temperature	_	± 0.3	± 0.3	%f _{dco}	1
f _{intf_ft}	Internal reference factory trimmed at	frequency (fast clock) — nominal VDD and 25°C		4	—	MHz	
f _{intf_t}	Internal reference trimmed at nomina	frequency (fast clock) — user Il VDD and 25 °C	3	_	5	MHz	
f _{loc_low}	Loss of external cl RANGE = 00	ock minimum frequency —	(3/5) x f _{ints_t}	_	—	kHz	
f _{loc_high}	Loss of external cl RANGE = 01, 10,	ock minimum frequency — or 11	(16/5) x f _{ints_t}	_	—	kHz	
		FI	L	•			
f _{fll_ref}	FLL reference freq	uency range	31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fll ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f _{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fll_ref}	80	83.89	100	MHz	
f _{dco_t_} DMX32	DCO output frequency	Low range (DRS=00) 732 × f _{fll_ref}		23.99	_	MHz	4, 5
		Mid range (DRS=01) 1464 × f _{fll_ref}	_	47.97	_	MHz	
		Mid-high range (DRS=10) 2197 × feu rof	_	71.99	—	MHz	
		High range (DRS=11) $2929 \times f_{fll_ref}$		95.98		MHz	

Table continues on the next page...

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	—	3.6	V	
I _{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	_	200	_	μΑ	
	• 8 MHz (RANGE=01)	_	300	_	μΑ	
	• 16 MHz	_	950	_	μΑ	
	• 24 MHz	_	1.2	_	mA	
	• 32 MHz	_	1.5	_	mA	
I _{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	_	25	_	μΑ	
	• 4 MHz	_	400	_	μA	
	• 8 MHz (RANGE=01)	_	500	_	μA	
	• 16 MHz	_	2.5	_	mA	
	• 24 MHz	_	3	_	mA	
	• 32 MHz	_	4	_	mA	
C _x	EXTAL load capacitance	_	—	_		2, 3
Cy	XTAL load capacitance		—			2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	_	_		MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	_	10	_	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	_	_	_	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	_	1		MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	_	_		kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200		kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	_	—		kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
		_	0	_	kΩ	

6.3.2.1 Oscillator DC electrical specifications Table 15. Oscillator DC electrical specifications

Table continues on the next page...

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

Writes_subsystem = $\frac{EEPROM - 2 \times EEESPLIT \times EEESIZE}{EEESPLIT \times EEESIZE} \times Write_efficiency \times n_{nvmcycd}$

where

- Writes_subsystem minimum number of writes to each FlexRAM location for subsystem (each subsystem can have different endurance)
- EEPROM allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with the Program Partition command
- EEESPLIT FlexRAM split factor for subsystem; entered with the Program Partition command
- EEESIZE allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency
 - 0.25 for 8-bit writes to FlexRAM
 - 0.50 for 16-bit or 32-bit writes to FlexRAM
- n_{nvmcycd} data flash cycling endurance (the following graph assumes 10,000 cycles)

Peripheral operating requirements and behaviors



Figure 10. EEPROM backup writes to FlexRAM

6.4.2 EzPort Switching Specifications Table 23. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	f _{SYS} /2	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	f _{SYS} /8	MHz
EP2	EZP_CS negation to next EZP_CS assertion	2 x t _{EZP_CK}		ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5		ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5		ns
EP5	EZP_D input valid to EZP_CK high (setup)	2		ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5		ns
EP7	EZP_CK low to EZP_Q output valid	—	16	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	_	ns
EP9	EZP_CS negation to EZP_Q tri-state	—	12	ns



Figure 11. EzPort Timing Diagram

6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.6 Analog

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 24 and Table 25 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

The ADCx_DP2 and ADCx_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in Table 26 and Table 27.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.



Figure 18. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 31.	VREF full-range	operating	requirements
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Symbol	Description	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage	1.71	3.6	V	
T _A	Temperature	Operating temperature range of the device		°C	
CL	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.

 The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	
V _{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	
V _{out}	Voltage reference output — user trim	1.193	_	1.197	V	
V _{step}	Voltage reference trim step	—	0.5	—	mV	
V _{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	—	—	80	mV	
I _{bg}	Bandgap only current	—	—	80	μA	1
I _{lp}	Low-power buffer current	—	—	360	uA	1
I _{hp}	High-power buffer current	_	_	1	mA	1
ΔV_{LOAD}	Load regulation				μV	1, 2
	• current = ± 1.0 mA	_	200	—		
T _{stup}	Buffer startup time		_	100	μs	
V _{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)		2		mV	1

Table 32. VREF full-range operating behaviors

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.

2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 33. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T _A	Temperature	0	50	°C	

Table 34. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{out}	Voltage reference output with factory trim	1.173	1.225	V	

6.7 Timers

See General switching specifications.

6.8 Communication interfaces

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t _{BUS}		ns
DS10	DSPI_SCK input high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid		10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0		ns
DS13	DSPI_SIN to DSPI_SCK input setup	2		ns
DS14	DSPI_SCK to DSPI_SIN input hold	7		ns
DS15	DSPI_SS active to DSPI_SOUT driven		14	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven		14	ns





Figure 20. DSPI classic SPI timing — slave mode

6.8.3 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	4 x t _{BUS}		ns	

Table 37. Master mode DSPI timing (full voltage range)

Table continues on the next page...



Figure 22. DSPI classic SPI timing — slave mode

6.8.4 I²C switching specifications

See General switching specifications.

6.8.5 UART switching specifications

See General switching specifications.

6.8.6 I2S/SAI Switching Specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

6.8.6.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 40. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	5.8	-	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	_	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	5.8	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



Figure 24. I2S/SAI timing — slave modes

6.8.6.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 41. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes
(full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period

Table continues on the next page...

Pinout

121 MAP	100 LQFP	Pin Name	Default	ALTO	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
K2	19	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DW/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3								
L1	20	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								
L2	21	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
F5	22	VDDA	VDDA	VDDA								
G5	23	VREFH	VREFH	VREFH								
G6	24	VREFL	VREFL	VREFL								
F6	25	VSSA	VSSA	VSSA								
L3	26	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
K5	27	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
L7	-	RTC_ WAKEUP_B	RTC_ WAKEUP_B	RTC_ WAKEUP_B								
L4	28	XTAL32	XTAL32	XTAL32								
L5	29	EXTAL32	EXTAL32	EXTAL32								
K6	30	VBAT	VBAT	VBAT								
H5	31	PTE24	ADC0_SE17	ADC0_SE17	PTE24		UART4_TX			EWM_OUT_b		
J5	32	PTE25	ADC0_SE18	ADC0_SE18	PTE25		UART4_RX			EWM_IN		
H6	33	PTE26	DISABLED		PTE26		UART4_CTS_ b			RTC_CLKOUT		
J6	34	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTAO	UART0_CTS_ b/ UART0_COL_ b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
H8	35	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
J7	36	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UARTO_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
H9	37	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UARTO_RTS_ b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
J8	38	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
K7	39	PTA5	DISABLED		PTA5		FTM0_CH2		CMP2_OUT	I2S0_TX_ BCLK	JTAG_TRST_ b	
E5	40	VDD	VDD	VDD								
G3	41	VSS	VSS	VSS								



Figure 27. K30 100 LQFP Pinout Diagram

Rev. No.	Date	Substantial Changes
2	4/2012	 Replaced TBDs throughout. Updated "Power consumption operating behaviors" table. Updated "ADC electrical specifications" section. Updated "VREF full-range operating behaviors" table. Updated "I2S/SAI Switching Specifications" section. Updated "TSI electrical specifications" table.
3	11/2012	 Updated orderable part numbers. Updated the maximum input voltage (V_{ADIN}) specification in the "16-bit ADC operating conditions" section.

Table 45. Revision History (continued)