Silicon Labs - C8051F320 Datasheet





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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete		
Core Processor	8051		
Core Size	8-Bit		
Speed	25MHz		
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART, USB		
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT		
Number of I/O	25		
Program Memory Size	16KB (16K x 8)		
Program Memory Type	FLASH		
EEPROM Size	-		
RAM Size	2.25K x 8		
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V		
Data Converters	A/D 17x10b		
Oscillator Type	Internal		
Operating Temperature	-40°C ~ 85°C (TA)		
Mounting Type	Surface Mount		
Package / Case	32-LQFP		
Supplier Device Package	32-LQFP (7x7)		
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f320		

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Figure 16.4 shows the typical SCL generation described Equation 16.2 Notice that T_{HGH} is typically twice as large as T_{OW} . The actual SCL output may vary due to other devices on the bus (SCL may be extended low by slower slave devices, or driven low boontending master device 3 be bit rate when operating as master will never exceed the limits defined by equation 16.1.



Setting the EXTHOLD bit extends the minimum setund and times for the SDA line. The minimum SDA setup time defines the absolute minimum time that SDA is stable before SCL transitions from low-to-high. The minimum SDA hold time defines the absolute minimum time thetdbrrent SDA value remains stable after SCL transitions from high-to-low. EXTHOLD should be set so that the minimum setup and hold times meet the SMBus Specification requirements of 250s and 300s, respectivelyTable16.2 shows the minimum setup and hold times for the two EXTHOLD settings. Setup and hold time extensions are typically necessary when SYSCLK is allobus 10

Table 10.2. WITHING OF SELUD AND THUS	Table 16.	2.Minimum	SDA 3	Setup	and I	Hold	Times
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EXTHOLD	Minimum SDA Setup Time	Minimum SDA Hold Time		
	T _{low} - 4 system clocks			
0	OR	3 system clocks		
	1 system clock + s/w delay			
1	11 system clocks	12 system clocks		

[†]Setup Time for ACK bit transmissions and the MSB of all data transfers. The s/w delay occurs between the time SMB0DAT or ACK isitteen and when SI is cleared. Note that if SI is cleared in the same write that defines the outgoing ACK value, s/w delay is zero.

With the SMBTOE bit set, Time should be configured to overflow after **2**/**s** in order to detect SCL low timeouts (see). The SMBus interface will force Time to reload while SCL is high, and allow Times to count when SCL is low. The Time interrupt service routine should be used to reset SMBus communication by disabling and re-enabling the SMBus.

SMBus Free Timeout detection can be enabled by setting the SMBFTE bit. When this bit is set, the bus will be con sidered free if SDA and SCL remain high for more than SMB us clock source periods (seigure 16.4). When a Free Timeout is detected, the interface will respond a STGP was detected (an interpt will be generated, and STO will be set).

Built-in Temperature Sensor

• External Conversion Start Input

Two Comparators -

- Two Comparators
 Internal Voltage Reference
 POR/Brown-Out Detector
 USB FUNCTION CONTROLLER
 USB Specification 2.0 Compliant
 Full Speed (12Mbps) or Low Speed (1.5Ibps) Operation
 Integrated Clock RecoverNo External Crystal Required for Full Speed or Low Speed

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