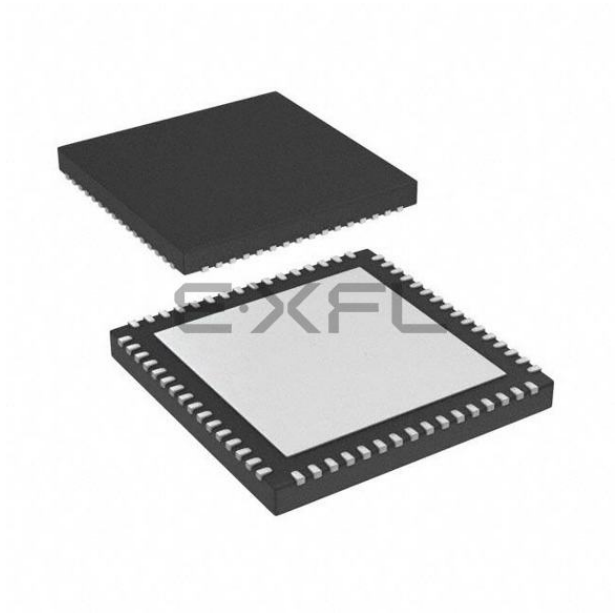
Microchip Technology - PIC32MZ0512EFE064-I/MR Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	46
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512efe064-i-mr

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTA							
RA0	—	17	A11	22	I/O	ST	PORTA is a bidirectional I/O port
RA1	—	38	B21	56	I/O	ST	
RA2	—	59	A41	85	I/O	ST	
RA3	—	60	B34	86	I/O	ST	
RA4	—	61	A42	87	I/O	ST	
RA5	—	2	B1	2	I/O	ST	
RA6	—	89	A61	129	I/O	ST	
RA7	—	90	B51	130	I/O	ST	
RA9	—	28	B15	39	I/O	ST	
RA10	—	29	A20	40	I/O	ST	
RA14	—	66	B37	95	I/O	ST	
RA15	—	67	A45	96	I/O	ST	
PORTB							
RB0	16	25	A18	36	I/O	ST	PORTB is a bidirectional I/O port
RB1	15	24	A17	35	I/O	ST	
RB2	14	23	A16	34	I/O	ST	
RB3	13	22	A14	31	I/O	ST	
RB4	12	21	A13	26	I/O	ST	
RB5	11	20	B11	25	I/O	ST	
RB6	17	26	B14	37	I/O	ST	
RB7	18	27	A19	38	I/O	ST	
RB8	21	32	B18	47	I/O	ST	
RB9	22	33	A23	48	I/O	ST	
RB10	23	34	B19	49	I/O	ST	
RB11	24	35	A24	50	I/O	ST	
RB12	27	41	A27	59	I/O	ST	
RB13	28	42	B23	60	I/O	ST	
RB14	29	43	A28	61	I/O	ST	
RB15	30	44	B24	62	I/O	ST	
PORTC							
RC1	—	6	B3	6	I/O	ST	PORTC is a bidirectional I/O port
RC2	—	7	A6	11	I/O	ST	
RC3	—	8	B5	12	I/O	ST	
RC4	—	9	A7	13	I/O	ST	
RC12	31	49	B28	71	I/O	ST	
RC13	47	72	B41	105	I/O	ST	
RC14	48	73	A49	106	I/O	ST	
RC15	32	50	A33	72	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source.For detailed information, refer to **Section 48. "Memory Organization and Permissions"** in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MZ EF microcontrollers provide 4 GB of unified virtual memory address space. All memory regions, including program, data memory, SFRs and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, PIC32MZ EF devices allow execution from data memory.

Key features include:

- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/ KSEG1/KSEG2/KSEG3) mode address space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Cacheable (KSEG0/KSEG2) and non-cacheable (KSEG1/KSEG3) address regions
- Read/write permission access to predefined memory regions

4.1 Memory Layout

PIC32MZ EF microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The main memory maps for the PIC32MZ EF devices are illustrated in Figure 4-1 through Figure 4-4. Figure 4-5 provides memory map information for boot Flash and boot alias. Table 4-1 provides memory map information for Special Function Registers (SFRs).

REGISTER 4-3: SBTxELOG1: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 1 ('x' = 0-13) (CONTINUED)

bit 7-4 **REGION<3:0>:** Requested Region Number bits
1111 - 0000 = Target's region that reported a permission group violation

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **CMD<2:0>:** Transaction Command of the Requester bits
111 = Reserved
110 = Reserved
101 = Write (a non-posted write)
100 = Reserved
011 = Read (a locked read caused by a Read-Modify-Write transaction)
010 = Read
001 = Write
000 = Idle

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

7.1 CPU Exceptions

CPU coprocessor 0 contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events or program errors. Table 7-1 lists the exception types in order of priority.

TABLE 7-1: MIPS32® M-CLASS MICROPROCESSOR CORE EXCEPTION TYPES

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Highest Priority						
Reset	Assertion $\overline{\text{MCLR}}$ or a Power-on Reset (POR).	0xBFC0_0000	BEV, ERL	—	—	_on_reset
Soft Reset	Assertion of a software Reset.	0xBFC0_0000	BEV, SR, ERL	—	—	_on_reset
DSS	EJTAG debug single step.	0xBFC0_0480	—	DSS	—	—
DINT	EJTAG debug interrupt. Caused by the assertion of the external EJ_DINT input or by setting the EjtagBrk bit in the ECR register.	0xBFC0_0480	—	DINT	—	—
NMI	Assertion of NMI signal.	0xBFC0_0000	BEV, NMI, ERL	—	—	_nmi_handler
Machine Check	TLB write that conflicts with an existing entry.	EBASE+0x180	MCHECK, EXL	—	0x18	_general_exception_handler
Interrupt	Assertion of unmasked hardware or software interrupt signal.	See Table 7-2.	IPL<2:0>	—	0x00	See Table 7-2.
Deferred Watch	Deferred watch (unmasked by K|DM=>!(K|DM) transition).	EBASE+0x180	WP, EXL	—	0x17	_general_exception_handler
DIB	EJTAG debug hardware instruction break matched.	0xBFC0_0480	—	DIB	—	—
WATCH	A reference to an address that is in one of the Watch registers (fetch).	EBASE+0x180	EXL	—	0x17	_general_exception_handler
AdEL	Fetch address alignment error. Fetch reference to protected address.	EBASE+0x180	EXL	—	0x04	_general_exception_handler
TLBL	Fetch TLB miss or fetch TLB hit to page with V = 0.	EBASE if Status.EXL = 0	—	—	0x02	—
		EBASE+0x180 if Status.EXL == 1	—	—	0x02	_general_exception_handler
TLBL Execute Inhibit	An instruction fetch matched a valid TLB entry that had the XI bit set.	EBASE+0x180	EXL	—	0x14	_general_exception_handler
IBE	Instruction fetch bus error.	EBASE+0x180	EXL	—	0x06	_general_exception_handler

7.3 Interrupt Control Registers

TABLE 7-3: INTERRUPT REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	INTCON	31:16	NMIKEY<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
0010	PRISS	31:16	PRI7SS<3:0>				PRI6SS<3:0>				PRI5SS<3:0>				PRI4SS<3:0>				0000
		15:0	PRI3SS<3:0>				PRI2SS<3:0>				PRI1SS<3:0>				—	—	—	SS0	0000
0020	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			SIRQ<7:0>								0000
0030	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
0040	IFS0	31:16	OC6IF	IC6IF	IC6EIF	T6IF	OC5IF	IC5IF	IC5EIF	T5IF	INT4IF	OC4IF	IC4IF	IC4EIF	T4IF	INT3IF	OC3IF	IC3IF	0000
		15:0	IC3EIF	T3IF	INT2IF	OC2IF	IC2IF	IC2EIF	T2IF	INT1IF	OC1IF	IC1IF	IC1EIF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
0050	IFS1	31:16	ADCD4IF	ADCD3IF	ADCD2IF	ADCD1IF	ADCD0IF	ADCFLTIF	ADCDF6IF	ADCDF5IF	ADCDF4IF	ADCDF3IF	ADCDF2IF	ADCDF1IF	ADCDC6IF	ADCDC5IF	ADCDC4IF	ADCDC3IF	0000
		15:0	ADCDC2IF	ADCDC1IF	ADCFIFOIF	ADCIF	OC9IF	IC9IF	IC9EIF	T9IF	OC8IF	IC8IF	IC8EIF	T8IF	OC7IF	IC7IF	IC7EIF	T7IF	0000
0060	IFS2(5)	31:16	ADCD36IF	ADCD35IF	ADCD34IF	ADCD33IF	ADCD32IF	ADCD31IF	ADCD30IF	ADCD29IF	ADCD28IF	ADCD27IF	ADCD26IF	ADCD25IF	ADCD24IF	ADCD23IF	ADCD22IF	ADCD21IF	0000
		15:0	ADCD20IF	ADCD19IF	ADCD18IF	ADCD17IF	ADCD16IF	ADCD15IF	ADCD14IF	ADCD13IF	ADCD12IF	ADCD11IF	ADCD10IF	ADCD9IF	ADCD8IF	ADCD7IF	ADCD6IF	ADCD5IF	0000
0070	IFS3(6)	31:16	CNKIF(8)	CNJIF	CNHIF	CNGIF	CNFIF	CNEIF	CNDIF	CNCIF	CNBIF	CNAIF	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	0000
		15:0	SPI1TXIF	SPI1RXIF	SPI1EIF	—	CRPTIF(7)	SBIF	CFDCIF	CPCIF	ADCD44IF	ADCD43IF	ADCD42IF	ADCD41IF	ADCD40IF	ADCD39IF	ADCD38IF	ADCD37IF	0000
0080	IFS4	31:16	U3TXIF	U3RXIF	U3EIF	SPI3TXIF	SPI3RXIF	SPI3EIF	ETHIF	CAN2IF(3)	CAN1IF(3)	I2C2MIF(2)	I2C2SIF(2)	I2C2BIF(2)	U2TXIF	U2RXIF	U2EIF	SPI2TXIF	0000
		15:0	SPI2RXIF	SPI2EIF	DMA7IF	DMA6IF	DMA5IF	DMA4IF	DMA3IF	DMA2IF	DMA1IF	DMA0IF	USBDMAIF	USBIF	CMP2IF	CMP1IF	PMPEIF	PMPIF	0000
0090	IFS5	31:16	—	U6TXIF	U6RXIF	U6EIF	SPI6TX(2)	SPI6RXIF(2)	SPI6IF(2)	I2C5MIF	I2C5SIF	I2C5BIF	U5TXIF	U5RXIF	U5EIF	SPI5TXIF(2)	SPI5RXIF(2)	SPI5EIF(2)	0000
		15:0	I2C4MIF	I2C4SIF	I2C4BIF	U4TXIF	U4RXIF	U4EIF	SQI1IF	PREIF	FCEIF	RTCCIF	SPI4TXIF	SPI4RXIF	SPI4EIF	I2C3MIF	I2C3SIF	I2C3BIF	0000
00A0	IFS6	31:16	—	—	—	—	—	—	—	—	—	—	ADC7WIF	—	—	ADC4WIF	ADC3WIF	ADC2WIF	0000
		15:0	ADC1WIF	ADC0WIF	ADC7EIF	—	—	ADC4EIF	ADC3EIF	ADC2EIF	ADC1EIF	ADC0EIF	—	ADCGRPIF	—	ADCURDYIF	ADCARDYIF	ADCEOSIF	0000
00C0	IEC0	31:16	OC6IE	IC6IE	IC6EIE	T6IE	OC5IE	IC5IE	IC5EIE	T5IE	INT4IE	OC4IE	IC4IE	IC4EIE	T4IE	INT3IE	OC3IE	IC3IE	0000
		15:0	IC3EIE	T3IE	INT2IE	OC2IE	IC2IE	IC2EIE	T2IE	INT1IE	OC1IE	IC1IE	IC1EIE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
00D0	IEC1	31:16	ADCD4IE	ADCD3IE	ADCD2IE	ADCD1IE	ADCD0IE	ADCFLTIE	ADCDF6IE	ADCDF5IE	ADCDF4IE	ADCDF3IE	ADCDF2IE	ADCDF1IE	ADCDC6IE	ADCDC5IE	ADCDC4IE	ADCDC3IE	0000
		15:0	ADCDC2IE	ADCDC1IE	ADCFIFOIE	ADCIE	OC9IE	IC9IE	IC9EIE	T9IE	OC8IE	IC8IE	IC8EIE	T8IE	OC7IE	IC7IE	IC7EIE	T7IE	0000
00E0	IEC2(5)	31:16	ADCD36IE	ADCD35IE	ADCD34IE	ADCD33IE	ADCD32IE	ADCD31IE	ADCD30IE	ADCD29IE	ADCD28IE	ADCD27IE	ADCD26IE	ADCD25IE	ADCD24IE	ADCD23IE	ADCD22IE	ADCD21IE	0000
		15:0	ADCD20IE	ADCD19IE	ADCD18IE	ADCD17IE	ADCD16IE	ADCD15IE	ADCD14IE	ADCD13IE	ADCD12IE	ADCD11IE	ADCD10IE	ADCD9IE	ADCD8IE	ADCD7IE	ADCD6IE	ADCD5IE	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

TABLE 8-2: OSCILLATOR CONFIGURATION REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets(2)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1360	PB7DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8800
1370	PB8DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
13C0	SLEWCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	SYSDIV<3:0>				0000
		15:0	—	—	—	—	—	SLWDIV<2:0>			—	—	—	—	—	UPEN	DNEN	BUSY	0204
13D0	CLKSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	LPRC RDY	SOSC RDY	—	POSC RDY	SPLL DIVRDY	FRCRDY	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3128	USB E2CSR2	31:16	Indexed by the same bits in USBIE2CSR2																0000
		15:0																	0000
312C	USB E2CSR3	31:16	Indexed by the same bits in USBIE2CSR3																0000
		15:0																	0000
3130	USB E3CSR0	31:16	Indexed by the same bits in USBIE3CSR0																0000
		15:0																	0000
3134	USB E3CSR1	31:16	Indexed by the same bits in USBIE3CSR1																0000
		15:0																	0000
3138	USB E3CSR2	31:16	Indexed by the same bits in USBIE3CSR2																0000
		15:0																	0000
313C	USB E3CSR3	31:16	Indexed by the same bits in USBIE3CSR3																0000
		15:0																	0000
3140	USB E4CSR0	31:16	Indexed by the same bits in USBIE4CSR0																0000
		15:0																	0000
3144	USB E4CSR1	31:16	Indexed by the same bits in USBIE4CSR1																0000
		15:0																	0000
3148	USB E4CSR2	31:16	Indexed by the same bits in USBIE4CSR2																0000
		15:0																	0000
314C	USB E4CSR3	31:16	Indexed by the same bits in USBIE4CSR3																0000
		15:0																	0000
3150	USB E5CSR0	31:16	Indexed by the same bits in USBIE5CSR0																0000
		15:0																	0000
3154	USB E5CSR1	31:16	Indexed by the same bits in USBIE5CSR1																0000
		15:0																	0000
3158	USB E5CSR2	31:16	Indexed by the same bits in USBIE5CSR2																0000
		15:0																	0000
315C	USB E5CSR3	31:16	Indexed by the same bits in USBIE5CSR3																0000
		15:0																	0000
3160	USB E6CSR0	31:16	Indexed by the same bits in USBIE6CSR0																0000
		15:0																	0000
3164	USB E6CSR1	31:16	Indexed by the same bits in USBIE6CSR1																0000
		15:0																	0000
3168	USB E6CSR2	31:16	Indexed by the same bits in USBIE6CSR2																0000
		15:0																	0000
316C	USB E6CSR3	31:16	Indexed by the same bits in USBIE6CSR3																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

REGISTER 11-1: USBCSR0: USB CONTROL STATUS REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS
	EP7TXIF	EP6TXIF	EP5TXIF	EP4TXIF	EP3TXIF	EP2TXIF	EP1TXIF	EP0IF
15:8	R/W-0	R/W-0	R/W-1	R-0, HS	R-0	R/W-0	R-0, HC	R/W-0
	ISOUPD	SOFTCONN	HSEN	HSMODE	RESET	RESUME	SUSPMODE	SUSPEN
	—	—						
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	FUNC<6:0>						
		—	—	—	—	—	—	—

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-17 **EP7TXIF:EP1TXIF:** Endpoint 'n' TX Interrupt Flag bit
1 = Endpoint has a transmit interrupt to be serviced
0 = No interrupt event

bit 16 **EP0IF:** Endpoint 0 Interrupt bit
1 = Endpoint 0 has an interrupt to be serviced
0 = No interrupt event

All EPxTX and EP0 bits are cleared when the byte is read. Therefore, these bits must be read independently from the remaining bits in this register to avoid accidental clearing.

bit 15 **ISOUPD:** ISO Update bit (*Device mode only; unimplemented in Host mode*)
1 = USB module will wait for a SOF token from the time TXPKTRDY is set before sending the packet
0 = No change in behavior

This bit only affects endpoints performing isochronous transfers when in *Device mode*. This bit is unimplemented in *Host mode*.

bit 14 **SOFTCONN:** Soft Connect/Disconnect Feature Selection bit
1 = The USB D+/D- lines are enabled and active
0 = The USB D+/D- lines are disabled and are tri-stated

This bit is only available in *Device mode*.

bit 13 **HSEN:** Hi-Speed Enable bit
1 = The USB module will negotiate for Hi-Speed mode when the device is reset by the hub
0 = Module only operates in Full-Speed mode

bit 12 **HSMODE:** Hi-Speed Mode Status bit
1 = Hi-Speed mode successfully negotiated during USB reset
0 = Module is not in Hi-Speed mode

In *Device mode*, this bit becomes valid when a USB reset completes. In *Host mode*, it becomes valid when the RESET bit is cleared.

bit 11 **RESET:** Module Reset Status bit
1 = Reset signaling is present on the bus
0 = Normal module operation

In *Device mode*, this bit is read-only. In *Host mode*, this bit is read/write.

REGISTER 11-3: USBCSR2: USB CONTROL STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0
	VBUSERRIE	SESSRQIE	DISCONIE	CONNIE	SOFIE	RESETIE	RESUMEIE	SUSPIE
23:16	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS
	VBUSERRIF	SESSRQIF	DISCONIF	CONNIF	SOFIF	RESETIF	RESUMEIF	SUSPIF
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	U-0
	EP7RXIE	EP6RXIE	EP5RXIE	EP4RXIE	EP3RXIE	EP2RXIE	EP1RXIE	—

Legend:	HS = Hardware Set		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **VBUSERRIE:** VBUS Error Interrupt Enable bit
1 = VBUS error interrupt is enabled
0 = VBUS error interrupt is disabled

bit 30 **SESSRQIE:** Session Request Interrupt Enable bit
1 = Session request interrupt is enabled
0 = Session request interrupt is disabled

bit 29 **DISCONIE:** Device Disconnect Interrupt Enable bit
1 = Device disconnect interrupt is enabled
0 = Device disconnect interrupt is disabled

bit 28 **CONNIE:** Device Connection Interrupt Enable bit
1 = Device connection interrupt is enabled
0 = Device connection interrupt is disabled

bit 27 **SOFIE:** Start of Frame Interrupt Enable bit
1 = Start of Frame event interrupt is enabled
0 = Start of Frame event interrupt is disabled

bit 26 **RESETIE:** Reset/Babble Interrupt Enable bit
1 = Interrupt when reset (*Device mode*) or Babble (*Host mode*) is enabled
0 = Reset/Babble interrupt is disabled

bit 25 **RESUMEIE:** Resume Interrupt Enable bit
1 = Resume signaling interrupt is enabled
0 = Resume signaling interrupt is disabled

bit 24 **SUSPIE:** Suspend Interrupt Enable bit
1 = Suspend signaling interrupt is enabled
0 = Suspend signaling interrupt is disabled

bit 23 **VBUSERRIF:** VBUS Error Interrupt bit
1 = VBUS has dropped below the VBUS valid threshold during a session
0 = No interrupt

bit 22 **SESSRQIF:** Session Request Interrupt bit
1 = Session request signaling has been detected
0 = No session request detected

bit 21 **DISCONIF:** Device Disconnect Interrupt bit
1 = In *Host mode*, indicates when a device disconnect is detected. In *Device mode*, indicates when a session ends.
0 = No device disconnect detected

bit 20 **CONNIF:** Device Connection Interrupt bit
1 = In *Host mode*, indicates when a device connection is detected
0 = No device connection detected

REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)

bit 18 **OVERRUN:** Data Overrun Status bit (*Device mode*)

1 = An OUT packet cannot be loaded into the RX FIFO.
0 = Written by software to clear this bit

This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.

ERROR: No Data Packet Received Status bit (*Host mode*)

1 = Three attempts have been made to receive a packet and no data packet has been received. An interrupt is generated.

0 = Written by the software to clear this bit.

This bit is only valid when the RX endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns zero.

bit 17 **FIFOFULL:** FIFO Full Status bit

1 = No more packets can be loaded into the RX FIFO
0 = The RX FIFO has at least one free space

bit 16 **RXPKTRDY:** Data Packet Reception Status bit

1 = A data packet has been received. An interrupt is generated.
0 = Written by software to clear this bit when the packet has been unloaded from the RX FIFO.

bit 15-11 **MULT<4:0>:** Multiplier Control bits

For Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints, multiplies TXMAXP by MULT+1 for the payload size.

For Bulk endpoints, MULT can be up to 32 and defines the number of “USB” packets of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. The data packet is required to be an exact multiple of the payload specified by TXMAXP.

For Isochronous/Interrupts endpoints operating in Hi-Speed mode, MULT may be either 2 or 3 and specifies the maximum number of such transactions that can take place in a single microframe.

bit 10-0 **RXMAXP<10:0>:** Maximum RX Payload Per Transaction Control bits

This field sets the maximum payload (in bytes) transmitted in a single transaction. The value is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-Speed and Hi-Speed operations.

RXMAXP must be set to an even number of bytes for proper interrupt generation in DMA Mode 1.

REGISTER 11-20: USBDMAINT: USB DMA INTERRUPT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS
	DMA8IF	DMA7IF	DMA6IF	DMA5IF	DMA4IF	DMA3IF	DMA2IF	DMA1IF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **DMAxIF:** DMA Channel 'x' Interrupt bit

1 = The DMA channel has an interrupt event
0 = No interrupt event

All bits are cleared on a read of the register.

REGISTER 11-29: USBLPMR2: USB LINK POWER MANAGEMENT CONTROL REGISTER 2 (CONTINUED)

bit 0 **LPMSTIF:** LPM STALL Interrupt Flag bit

When in *Device mode*:

1 = A LPM transaction was received and the USB Module responded with a STALL

0 = No Stall condition

When in *Host mode*:

1 = A LPM transaction was transmitted and the device responded with a STALL

0 = No Stall condition

27.1 RNG Control Registers

TABLE 27-2: RANDOM NUMBER GENERATOR (RNG) REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6000	RNGVER	31:16	ID<15:0>																xxxx
		15:0	VERSION<7:0>								REVISION<7:0>								xxxx
6004	RNGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	LOAD	TRNGMODE	CONT	PRNGEN	TRNGEN	PLEN<7:0>								0064
6008	RNGPOLY1	31:16	POLY<31:0>																FFFF
		15:0																	0000
600C	RNGPOLY2	31:16	POLY<31:0>																FFFF
		15:0																	0000
6010	RNGNUMGEN1	31:16	RNG<31:0>																FFFF
		15:0																	FFFF
6014	RNGNUMGEN2	31:16	RNG<31:0>																FFFF
		15:0																	FFFF
6018	RNGSEED1	31:16	SEED<31:0>																0000
		15:0																	0000
601C	RNGSEED2	31:16	SEED<31:0>																0000
		15:0																	0000
6020	RNGCNT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	RCNT<6:0>							0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 28-5: ADCIMCON1: ADC INPUT MODE CONTROL REGISTER 1 (CONTINUED)

bit 20 **SIGN10:** AN10 Signed Data Mode bit
1 = AN10 is using Signed Data mode
0 = AN10 is using Unsigned Data mode

bit 19 **DIFF9:** AN9 Mode bit
1 = AN9 is using Differential mode
0 = AN9 is using Single-ended mode

bit 18 **SIGN9:** AN9 Signed Data Mode bit
1 = AN9 is using Signed Data mode
0 = AN9 is using Unsigned Data mode

bit 17 **DIFF8:** AN 8 Mode bit
1 = AN8 is using Differential mode
0 = AN8 is using Single-ended mode

bit 16 **SIGN8:** AN8 Signed Data Mode bit
1 = AN8 is using Signed Data mode
0 = AN8 is using Unsigned Data mode

bit 15 **DIFF7:** AN7 Mode bit
1 = AN7 is using Differential mode
0 = AN7 is using Single-ended mode

bit 14 **SIGN7:** AN7 Signed Data Mode bit
1 = AN7 is using Signed Data mode
0 = AN7 is using Unsigned Data mode

bit 13 **DIFF6:** AN6 Mode bit
1 = AN6 is using Differential mode
0 = AN6 is using Single-ended mode

bit 12 **SIGN6:** AN6 Signed Data Mode bit
1 = AN6 is using Signed Data mode
0 = AN6 is using Unsigned Data mode

bit 11 **DIFF5:** AN5 Mode bit
1 = AN5 is using Differential mode
0 = AN5 is using Single-ended mode

bit 10 **SIGN5:** AN5 Signed Data Mode bit
1 = AN5 is using Signed Data mode
0 = AN5 is using Unsigned Data mode

bit 9 **DIFF4:** AN4 Mode bit
1 = AN4 is using Differential mode
0 = AN4 is using Single-ended mode

bit 8 **SIGN4:** AN4 Signed Data Mode bit
1 = AN4 is using Signed Data mode
0 = AN4 is using Unsigned Data mode

bit 7 **DIFF3:** AN3 Mode bit
1 = AN3 is using Differential mode
0 = AN3 is using Single-ended mode

bit 6 **SIGN3:** AN3 Signed Data Mode bit
1 = AN3 is using Signed Data mode
0 = AN3 is using Unsigned Data mode

bit 5 **DIFF2:** AN2 Mode bit
1 = AN2 is using Differential mode
0 = AN2 is using Single-ended mode

REGISTER 28-25: ADCDATAx: ADC OUTPUT DATA REGISTER ('x' = 0 THROUGH 44)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>:** ADC Converted Data Output bits.

Note 1: The registers, ADCDATA19 through ADCDATA34, are not available on 64-pin devices.

2: The registers, ADCDATA35 through ADCDATA42, are not available on 64-pin and 100-pin devices.

3: When an alternate input is used as the input source for a dedicated ADC module, the data output is still read from the Primary input Data Output Register.

4: Reading the ADCDATAx register value after changing the FRACT bit converts the data into the format specified by FRACT bit.

33.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS60001130) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This section describes power-saving features for the PIC32MZ EF devices. These devices offer various methods and modes that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

33.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the speed of PBCLK7, or selecting a lower power clock source (i.e., LPRC or SOSC).

In addition, the Peripheral Bus Scaling mode is available for each peripheral bus where peripherals are clocked at reduced speed by selecting a higher divider for the associated PBCLKx, or by disabling the clock completely.

33.2 Power-Saving with CPU Halted

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

33.2.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted and the associated clocks are disabled. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the peripheral bus clocks will start running and the device will enter into Idle mode.

33.2.2 IDLE MODE

In Idle mode, the CPU is Halted; however, all clocks are still enabled. This allows peripherals to continue to operate. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

TABLE 37-39: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS(2)			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period	20	—	6250	ns	—
Throughput Rate							
AD51	FTP	Sample Rate for ADC0-ADC4 (Class 1 Inputs)	— — — —	— — — —	3.125 3.57 4.16 5	Msps Msps Msps Msps	12-bit resolution Source Impedance ≤ 200Ω 10-bit resolution Source Impedance ≤ 200Ω 8-bit resolution Source Impedance ≤ 200Ω 6-bit resolution Source Impedance ≤ 200Ω
		Sample Rate for ADC7 (Class 2 and Class 3 Inputs)	— — — —	— — — —	2.94 3.33 3.84 4.55	Msps Msps Msps Msps	12-bit resolution Source Impedance ≤ 200Ω 10-bit resolution Source Impedance ≤ 200Ω 8-bit resolution Source Impedance ≤ 200Ω 6-bit resolution Source Impedance ≤ 200Ω
Timing Parameters							
AD60	TSAMP	Sample Time for ADC0-ADC4 (Class 1 Inputs)	3 4 5 13	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
		Sample Time for ADC7 (Class 2 and 3 Inputs)	4 5 6 14	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
		Sample Time for ADC7 (Class 2 and 3 Inputs)	See Table 37-40	—	—	TAD	CVDEN (ADCCON1<11>) = 1
AD62	TCONV	Conversion Time (after sample time is complete)	— — — —	— — — —	13 11 9 7	TAD	12-bit resolution 10-bit resolution 8-bit resolution 6-bit resolution
AD65	TWAKE	Wake-up time from Low-Power Mode	— —	500 20	— —	TAD µs	Lesser of 500 TAD or 20 µs.

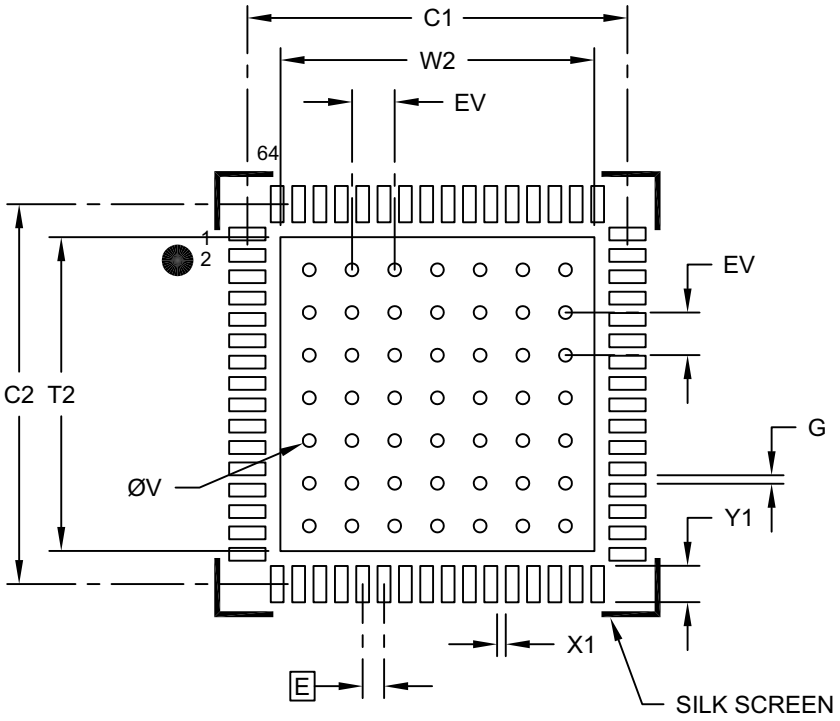
Note 1: These parameters are characterized, but not tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

41.2 Package Details

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length and 7.70x7.70mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			7.50
Optional Center Pad Length	T2			7.50
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.90
Contact Pad to Center Pad (X20)	G	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-2213B

TABLE A-1: OSCILLATOR CONFIGURATION DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Secondary Oscillator Enable	
FSOSCEN (DEVCFG1<**5**>)	The location of the SOSCEN bit in the Flash Configuration Words has moved. FSOSCEN (DEVCFG1<**6**>)
PLL Configuration	
The FNOSC<2:0> and NOSC<2:0> bits select between POSC and FRC. **FNOSC<2:0> (DEVCFG1<2:0>)** **NOSC<2:0> (OSCCON<10:8>)**	Selection of which input clock (POSC or FRC) is now done through the FPLLICLK/PLLICLK bits. **FPLLICLK (DEVCFG2<7>)** **PLLICLK (SPLLCON<7>)**
On PIC32MX devices, the input frequency to the PLL had to be between 4 MHz and 5 MHz. FPLLIDIV selected how to divide the input frequency to give it the appropriate range. FPLLIDIV<2:0> (DEVCFG2<2:0>) **111 = 12x divider** **110 = 10x divider** 101 = 6x divider 100 = 5x divider 011 = 4x divider 010 = 3x divider 001 = 2x divider 000 = 1x divider	On PIC32MZ EF devices, the input range for the PLL is wider (5 MHz to 64 MHz). The input divider values have changed, and new FPLLRNG/PLLRNG bits have been added to indicate under what range the input frequency falls. FPLLIDIV<2:0> (DEVCFG2<2:0>) **PLLIDIV<2:0> (SPLLCON<2:0>)** **111 = Divide by 8** **110 = Divide by 7** 101 = Divide by 6 100 = Divide by 5 011 = Divide by 4 010 = Divide by 3 001 = Divide by 2 000 = Divide by 1 **FPLLRNG<2:0> (DEVCFG2<6:4>)** **PLLRNG<2:0> (SPLLCON<2:0>)** **111 = Reserved** **110 = Reserved** **101 = 34-64 MHz** **100 = 21-42 MHz** **011 = 13-26 MHz** **010 = 8-16 MHz** **001 = 5-10 MHz** **000 = Bypass**
On PIC32MX devices, the output frequency of PLL is between 60 MHz and 120 MHz. The PLL multiplier and divider bits configure the PLL for this range. FPLLMUL<**2**:0> (DEVCFG2<**6:4**>) PLLMULT<**2**:0> (OSCCON<18:16>) **111 = 24x multiplier** **110 = 21x multiplier** **101 = 20x multiplier** **100 = 19x multiplier** **011 = 18x multiplier** **010 = 17x multiplier** **001 = 16x multiplier** **000 = 15x multiplier** FPLLODIV<2:0> (DEVCFG2<18:16>) PLLODIV<2:0> (OSCCON<29:27>) **111 = 24x multiplier** **110 = 21x multiplier** **101 = 20x multiplier** **100 = 19x multiplier** **011 = 18x multiplier** **010 = 17x multiplier** **001 = 16x multiplier** **000 = 15x multiplier**	The PLL multiplier and divider on PIC32MZ EF devices have a wider range to accommodate the wider PLL specification range. FPLLMUL**T**<**6**:0> (DEVCFG2<**14:8**>) PLLMULT<**6**:0> (**SPLLCON<22:16>**) **1111111 = Multiply by 128** **1111110 = Multiply by 127** **1111101 = Multiply by 126** **1111100 = Multiply by 125** • • • **0000000 = Multiply by 1** FPLLODIV<2:0> (DEVCFG2<18:16>) PLLODIV<2:0> (**SPLLCON<26:24>**) **111 = PLL Divide by 32** **110 = PLL Divide by 32** **101 = PLL Divide by 32** **100 = PLL Divide by 16** **011 = PLL Divide by 8** **010 = PLL Divide by 4** **001 = PLL Divide by 2** **000 = PLL Divide by 2**

TABLE A-3: ADC DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Scan Trigger Source	
On PIC32MX devices, there are four sources that can trigger a scan conversion in the ADC module: Auto, Timer3, INT0, and clearing the SAMP bit. SSRC<2:0> (AD1CON1<7:5>) 111 = Auto convert 110 = Reserved 101 = Reserved 100 = Reserved 011 = Reserved 010 = Timer3 period match 001 = Active transition on INT0 pin 000 = Clearing SAMP bit	On PIC32MZ EF devices, the list of sources for triggering a scan conversion has been expanded to include the comparators, Output Compare, and two additional Timers. In addition, trigger sources can be simulated by setting the RQCNVRT (ADCCON3<8>) bit. STRGSRC<4:0> (ADCCON1<20:16>) 11111 = Reserved • • • 01101 = Reserved 01100 = Comparator 2 COUT 01011 = Comparator 1 COUT 01010 = OCMP5 01001 = OCMP3 01000 = OCMP1 00111 = TMR5 match 00110 = TMR3 match 00101 = TMR1 match 00100 = INT0 00011 = Reserved 00010 = Global level software trigger (GLSWTRG) 00001 = Global software trigger (GSWTRG) 00000 = No trigger
Output Format	
On PIC32MX devices, the output format was decided for all ADC channels based on the setting of the FORM<2:0> bits. FORM<2:0> (AD1CON1<10:8>) 011 = Signed Fractional 16-bit 010 = Fractional 16-bit 001 = Signed Integer 16-bit 000 = Integer 16-bit 111 = Signed Fractional 32-bit 110 = Fractional 32-bit 101 = Signed Integer 32-bit 100 = Integer 32-bit	On PIC32MZ EF devices, the FRACT bit determines whether fractional or integer format is used. Then, each input can have its own setting for input (differential or single-ended) and sign (signed or unsigned) using the DIFFx and SIGNx bits in the ADCIMODx registers. FRACT (ADCCON1<23>) 1 = Fractional 0 = Integer DIFFx (ADCIMODy) 1 = Channel x is using Differential mode 0 = Channel x is using Single-ended mode SIGNx (ADCMODy) 1 = Channel x is using Signed Data mode 0 = Channel x is using Unsigned Data mode
Interrupts	
On PIC32MX devices, an interrupt is triggered from the ADC module when a certain number of conversions have taken place, irrespective of which channel was converted. SMPI<3:0> (AD1CON2<5:2>) 1111 = Interrupt for each 16th sample/convert sequence 1110 = Interrupt for each 15th sample/convert sequence • • • 0001 = Interrupt for each 2nd sample/convert sequence 0000 = Interrupt for each sample/convert sequence	On PIC32MZ EF devices, the ADC module can trigger an interrupt for each channel when it is converted. Use the Interrupt Controller bits, IEC1<31:27>, IEC2<31:0>, and IEC3<7:0>, to enable/disable them. In addition, the ADC support one global interrupt to indicate conversion on any number of channels. AGIENxx (ADCGIRQENx<y>) 1 = Data ready event will generate a Global ADC interrupt 0 = No global interrupt In addition, interrupts can be generated for filter and comparator events.