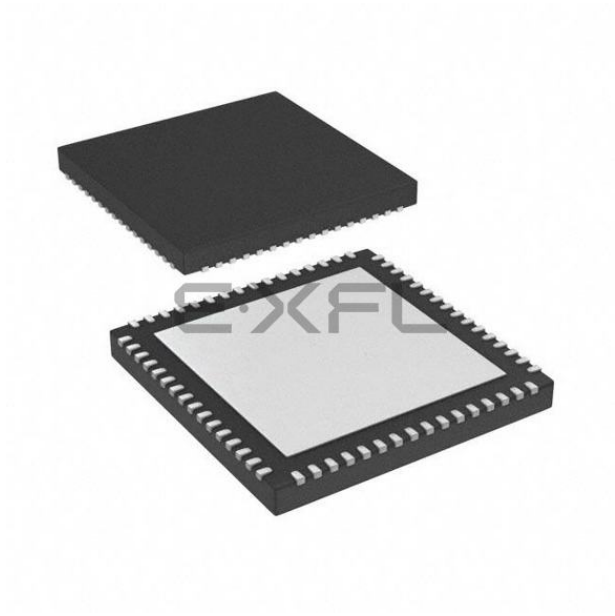

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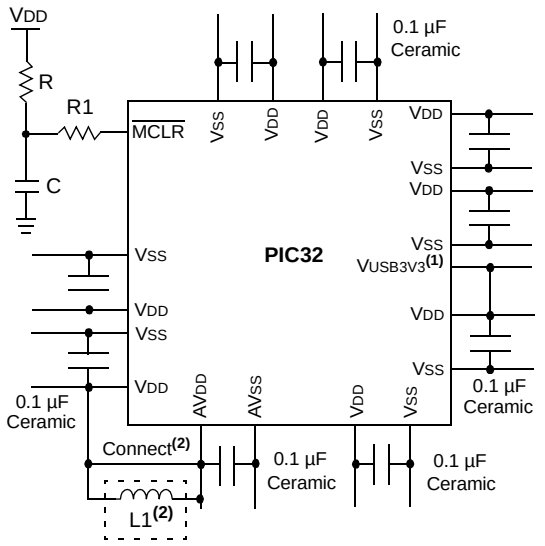
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M-Class |
| Core Size | 32-Bit Single-Core |
| Speed | 200MHz |
| Connectivity | Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 46 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.1V ~ 3.6V |
| Data Converters | A/D 24x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-QFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512efe064t-i-mr |

**FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION**




**Note 1:** If the USB module is not used, this pin must be connected to VSS.

**2:** As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{FCNV}{2} \quad \text{(i.e., ADC conversion rate/2)}$$

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

### 2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

## 2.3 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

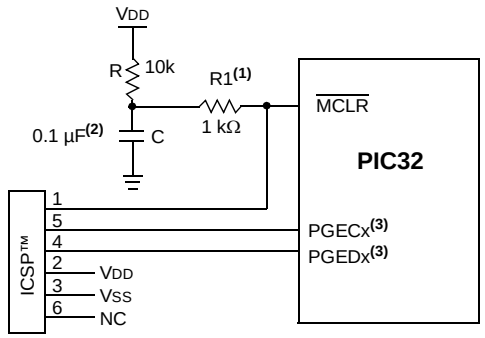
- Device Reset
- Device programming and debugging

Pulling The MCLR pin low generates either a device Reset or a POR, depending on the setting of the SMCLR bit (DEVCFG0<15>). Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

**FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS**




**Note 1:** 470Ω ≤ R1 ≤ 1kΩ will limit any current flowing into MCLR from the external capacitor C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met without interfering with the Debug/Programmer tools.

**2:** The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

**3:** No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

**REGISTER 5-8: NVMBWP: FLASH BOOT (PAGE) WRITE-PROTECT REGISTER**

bit 4 **UBWP4:** Upper Boot Alias Page 4 Write-protect bit(1)
1 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF enabled
0 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF disabled

bit 3 **UBWP3:** Upper Boot Alias Page 3 Write-protect bit(1)
1 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF enabled
0 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF disabled

bit 2 **UBWP2:** Upper Boot Alias Page 2 Write-protect bit(1)
1 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF enabled
0 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF disabled

bit 1 **UBWP1:** Upper Boot Alias Page 1 Write-protect bit(1)
1 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF enabled
0 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF disabled

bit 0 **UBWP0:** Upper Boot Alias Page 0 Write-protect bit(1)
1 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF enabled
0 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF disabled

**Note 1:** These bits are only available when the NVMKEY unlock sequence is performed and the associated Lock bit (LBWPULOCK or UBWPULOCK) is set.

| **Note:** | The bits in this register are only writable when the NVMKEY unlock sequence is followed. |
|---|---|

## 7.0 CPU EXCEPTIONS AND INTERRUPT CONTROLLER

**Note:** This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupt Controller"** (DS60001108) and **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MZ EF devices generate interrupt requests in response to interrupt events from peripheral modules. The Interrupt Controller module exists outside of the CPU and prioritizes the interrupt events before presenting them to the CPU.

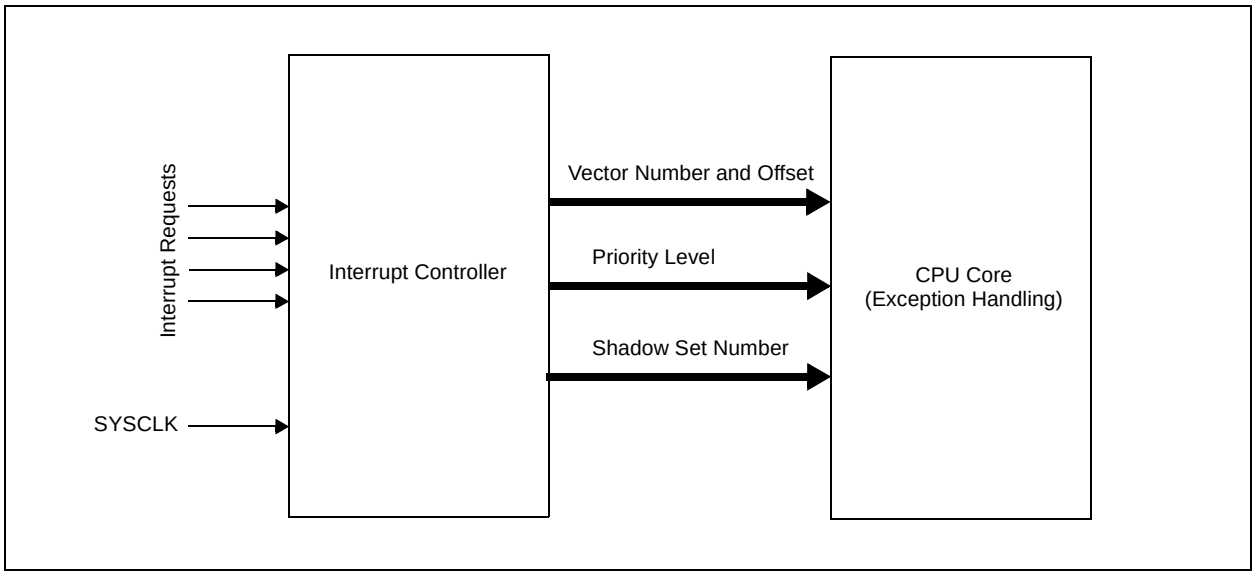
The CPU handles interrupt events as part of the exception handling mechanism, which is described in **Section 7.1 "CPU Exceptions"**.

The Interrupt Controller module includes the following features:

- Up to 213 interrupt sources and vectors with dedicated programmable offsets, eliminating the need for redirection
- Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable subpriority levels within each priority
- Seven shadow register sets that can be used for any priority level, eliminating software context switch and reducing interrupt latency
- Software can generate any interrupt

Figure 7-1 shows the block diagram for the Interrupt Controller and CPU exceptions.

**FIGURE 7-1: CPU EXCEPTIONS AND INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM**



## 10.1 DMA Control Registers

### TABLE 10-1: DMA GLOBAL REGISTER MAP

| Virtual Address (BF81_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1000 | DMACON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | SUSPEND | DMABUSY | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 1010 | DMASTAT | 31:16 | RDWR | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | DMACH<2:0> | | | 0000 |
| 1020 | DMAADDR | 31:16 | DMAADDR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

### TABLE 10-2: DMA CRC REGISTER MAP

| Virtual Address (BF81_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1030 | DCRCCON | 31:16 | — | — | BYTO<1:0> | | WBO | — | — | BITO | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | PLEN<4:0> | | | | | CRCEN | CRCAPP | CRCTYP | — | — | CRCCH<2:0> | | | 0000 |
| 1040 | DCRCDATA | 31:16 | DCRCDATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 1050 | DCRCXOR | 31:16 | DCRCXOR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

**REGISTER 11-4: USBCSR3: USB CONTROL STATUS REGISTER 3 (CONTINUED)**

bit 19-16 **ENDPOINT<3:0>:** Endpoint Registers Select bits
1111 = Reserved
•
•
•
1000 = Reserved
0111 = Endpoint 7
•
•
•
0000 = Endpoint 0
These bits select which endpoint registers are accessed through addresses 3010-301F.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **RFRMNUM<10:0>:** Last Received Frame Number bits

**REGISTER 11-29: USBLPMR2: USB LINK POWER MANAGEMENT CONTROL REGISTER 2 (CONTINUED)**

bit 0 **LPMSTIF:** LPM STALL Interrupt Flag bit

When in *Device mode*:

1 = A LPM transaction was received and the USB Module responded with a STALL

0 = No Stall condition

When in *Host mode*:

1 = A LPM transaction was transmitted and the device responded with a STALL

0 = No Stall condition

**TABLE 12-18: PORTH REGISTER MAP FOR 144-PIN DEVICES ONLY**

| Virtual Address (BF86_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0700 | ANSELH | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | ANSH6 | ANSH5 | ANSH4 | — | — | ANSH1 | ANSH0 | 0073 |
| 0710 | TRISH | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISH15 | TRISH14 | TRISH13 | TRISH12 | TRISH11 | TRISH10 | TRISH9 | TRISH8 | TRISH7 | TRISH6 | TRISH5 | TRISH4 | TRISH3 | TRISH2 | TRISH1 | TRISH0 | FFFF |
| 0720 | PORTH | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RH15 | RH14 | RH13 | RH12 | RH11 | RH10 | RH9 | RH8 | RH7 | RH6 | RH5 | RH4 | RH3 | RH2 | RH1 | RH0 | xxxx |
| 0730 | LATH | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATH15 | LATH14 | LATH13 | LATH12 | LATH11 | LATH10 | LATH9 | LATH8 | LATH7 | LATH6 | LATH5 | LATH4 | LATH3 | LATH2 | LATH1 | LATH0 | xxxx |
| 0740 | ODCH | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCH15 | ODCH14 | ODCH13 | ODCH12 | ODCH11 | ODCH10 | ODCH9 | ODCH8 | ODCH7 | ODCH6 | ODCH5 | ODCH4 | ODCH3 | ODCH2 | ODCH1 | ODCH0 | 0000 |
| 0750 | CNPUH | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPUH15 | CNPUH14 | CNPUH13 | CNPUH12 | CNPUH11 | CNPUH10 | CNPUH9 | CNPUH8 | CNPUH7 | CNPUH6 | CNPUH5 | CNPUH4 | CNPUH3 | CNPUH2 | CNPUH1 | CNPUH0 | 0000 |
| 0760 | CNPDH | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPDH15 | CNPDH14 | CNPDH13 | CNPDH12 | CNPDH11 | CNPDH10 | CNPDH9 | CNPDH8 | CNPDH7 | CNPDH6 | CNPDH5 | CNPDH4 | CNPDH3 | CNPDH2 | CNPDH1 | CNPDH0 | 0000 |
| 0770 | CNCONH | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | — | EDGE DETECT | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 0780 | CNENH | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNENH15 | CNENH14 | CNENH13 | CNENH12 | CNENH11 | CNENH10 | CNENH9 | CNENH8 | CNENH7 | CNENH6 | CNENH5 | CNENH4 | CNENH3 | CNENH2 | CNENH1 | CNENH0 | 0000 |
| 0790 | CNSTATH | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CN STATH15 | CN STATH14 | CN STATH13 | CN STATH12 | CN STATH11 | CN STATH10 | CN STATH9 | CN STATH8 | CN STATH7 | CN STATH6 | CN STATH5 | CN STATH4 | CN STATH3 | CN STATH2 | CN STATH1 | CN STATH0 | 0000 |
| 07A0 | CNNEH | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNNEH15 | CNNEH14 | CNNEH13 | CNNEH12 | CNNEH11 | CNNEH10 | CNNEH9 | CNNEH8 | CNNEH7 | CNNEH6 | CNNEH5 | CNNEH4 | CNNEH3 | CNNEH2 | CNNEH1 | CNNEH0 | 0000 |
| 07B0 | CNFH | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNFH15 | CNFH14 | CNFH13 | CNFH12 | CNFH11 | CNFH10 | CNFH9 | CNFH8 | CNFH7 | CNFH6 | CNFH5 | CNFH4 | CNFH3 | CNFH2 | CNFH1 | CNFH0 | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

**REGISTER 15-1: DMTCON: DEADMAN TIMER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-y | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| Legend: | | y = Value set from Configuration bits on POR | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Deadman Timer Module Enable bit(1)
1 = Deadman Timer module is enabled
0 = Deadman Timer module is disabled
The reset value of this bit is determined by the setting of the FDMTEN bit (DEVCFG1<3>).

bit 13-0 **Unimplemented:** Read as '0'

**Note 1:** This bit only has control when FDMTEN (DEVCFG1<3>) = 0.

**REGISTER 15-2: DMTPRECLR: DEADMAN TIMER PRECLEAR REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | STEP1<7:0> | | | | | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STEP1<7:0>:** Preclear Enable bits
01000000 = Enables the Deadman Timer Preclear (Step 1)
All other write patterns = Set BAD1 flag.
These bits are cleared when a DMT reset event occurs. STEP1<7:0> is also cleared if the STEP2<7:0> bits are loaded with the correct value in the correct sequence.

bit 7-0 **Unimplemented:** Read as '0'

## 21.0 INTER-INTEGRATED CIRCUIT ($I^2C$)

**Note:** This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. "Inter-Integrated Circuit ($I^2C$)"** (DS60001116) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The $I^2C$ module provides complete hardware support for both Slave and Multi-Master modes of the $I^2C$ serial communication standard.

Each $I^2C$ module has a 2-pin interface:

- SCLx pin is clock
- SDAx pin is data

Each $I^2C$ module offers the following key features:

- $I^2C$ interface supporting both master and slave operation
- $I^2C$ Slave mode supports 7-bit and 10-bit addressing
- $I^2C$ Master mode supports 7-bit and 10-bit addressing
- $I^2C$ port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the $I^2C$ port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- $I^2C$ supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking
- SMBus support

Figure 21-1 illustrates the $I^2C$ module block diagram.

**REGISTER 28-2: ADCCON2: ADC CONTROL REGISTER 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BGVRRDY | REFFLT | EOSRDY | CVDCPL<2:0> | | | SAMC<9:8> | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SAMC<7:0> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | BGVRIEN | REFFLTIEN | EOSIEN | ADCEIOVR | — | ADCEIS<2:0> | | |
| 7:0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | ADCDIV<6:0> | | | | | | |

| Legend: | HC = Hardware Set | HS = Hardware Cleared | r = Reserved |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **BGVRRDY:** Band Gap Voltage/ADC Reference Voltage Status bit

1 = Both band gap voltage and ADC reference voltages ($V_{REF}$) are ready
0 = Either or both band gap voltage and ADC reference voltages ($V_{REF}$) are not ready

Data processing is valid only after BGVRRDY is set by hardware, so the application code must check that the BGVRRDY bit is set to ensure data validity. This bit set to '0' when ON (ADCCON1<15>) = 0.

bit 30 **REFFLT:** Band Gap/$V_{REF}$/$AV_{DD}$ BOR Fault Status bit

1 = Fault in band gap or the $V_{REF}$ voltage while the ON bit (ADCCON1<15>) was set. Most likely a band gap or $V_{REF}$ fault will be caused by a BOR of the analog $V_{DD}$ supply.
0 = Band gap and $V_{REF}$ voltage are working properly

This bit is cleared when the ON bit (ADCCON1<15>) = 0 and the BGVRRDY bit = 1.

bit 29 **EOSRDY:** End of Scan Interrupt Status bit

1 = All analog inputs are considered for scanning through the scan trigger (all analog inputs specified in the ADCCSS1 and ADCCSS2 registers) have completed scanning
0 = Scanning has not completed

This bit is cleared when ADCCON2<31:24> are read in software.

bit 28-26 **CVDCPL<2:0>:** Capacitor Voltage Divider (CVD) Setting bit

111 = 7 * 2.5 pF = 17.5 pF
110 = 6 * 2.5 pF = 15 pF
101 = 5 * 2.5 pF = 12.5 pF
100 = 4 * 2.5 pF = 10 pF
011 = 3 * 2.5 pF = 7.5 pF
010 = 2 * 2.5 pF = 5 pF
001 = 1 * 2.5 pF = 2.5 pF
000 = 0 * 2.5 pF = 0 pF

bit 25-16 **SAMC<9:0>:** Sample Time for the Shared ADC (ADC7) bits

1111111111 = 1025 $T_{AD7}$
•
•
•
0000000001 = 3 $T_{AD7}$
0000000000 = 2 $T_{AD7}$

Where $T_{AD7}$ = period of the ADC conversion clock for the Shared ADC (ADC7) controlled by the ADCDIV<6:0> bits.

bit 15 **BGVRIEN:** Band Gap/$V_{REF}$ Voltage Ready Interrupt Enable bit

1 = Interrupt will be generated when the BGVRDDY bit is set
0 = No interrupt is generated when the BGVRRDY bit is set

**REGISTER 30-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | HTEN | MPEN | — | NOTPM | PMMODE<3:0> | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CRCERREN | CRCOKEN | RUNTERREN | RUNTEN | UCEN | NOTMEEN | MCEN | BCEN |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **HTEN:** Enable Hash Table Filtering bit
1 = Enable Hash Table Filtering
0 = Disable Hash Table Filtering

bit 14 **MPEN:** Magic Packet™ Enable bit
1 = Enable Magic Packet Filtering
0 = Disable Magic Packet Filtering

bit 13 **Unimplemented:** Read as '0'

bit 12 **NOTPM:** Pattern Match Inversion bit
1 = The Pattern Match Checksum must not match for a successful Pattern Match to occur
0 = The Pattern Match Checksum must match for a successful Pattern Match to occur
This bit determines whether Pattern Match Checksum must match in order for a successful Pattern Match to occur.

bit 11-8 **PMMODE<3:0>:** Pattern Match Mode bits
1001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Packet = Magic Packet)**(1,3)**
1000 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Hash Table Filter match)**(1,1)**
0111 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)**(1)**
0110 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)**(1)**
0101 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)**(1)**
0100 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)**(1)**
0011 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)**(1)**
0010 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)**(1)**
0001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches)**(1)**
0000 = Pattern Match is disabled; pattern match is always unsuccessful

**Note 1:** XOR = True when either one or the other conditions are true, but not both.
**2:** This Hash Table Filter match is active regardless of the value of the HTEN bit.
**3:** This Magic Packet Filter match is active regardless of the value of the MPEN bit.

**Note 1:** This register is only used for RX operations.
**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

**REGISTER 31-1: CMxCON: COMPARATOR CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | R-0 |
| | ON | COE | CPOL(1) | — | — | — | — | COUT |
| 7:0 | R/W-1 | R/W-1 | U-0 | R/W-0 | U-0 | U-0 | R/W-1 | R/W-1 |
| | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator ON bit
- 1 = Module is enabled. Setting this bit does not affect the other bits in this register
- 0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register

bit 14 **COE:** Comparator Output Enable bit
- 1 = Comparator output is driven on the output CxOUT pin
- 0 = Comparator output is not driven on the output CxOUT pin

bit 13 **CPOL:** Comparator Output Inversion bit(1)
- 1 = Output is inverted
- 0 = Output is not inverted

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **COUT:** Comparator Output bit
- 1 = Output of the Comparator is a '1'
- 0 = Output of the Comparator is a '0'

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits
- 11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
- 10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
- 01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
- 00 = Comparator interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Positive Input Configure bit
- 1 = Comparator non-inverting input is connected to the internal CVREF
- 0 = Comparator non-inverting input is connected to the CXINA pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator
- 11 = Comparator inverting input is connected to the IVREF
- 10 = Comparator inverting input is connected to the CxIND pin
- 01 = Comparator inverting input is connected to the CxINC pin
- 00 = Comparator inverting input is connected to the CxINB pin

**Note 1:** Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

## 32.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

**Note:** This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 20. "Comparator Voltage Reference (CVREF)"** (DS60001109) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

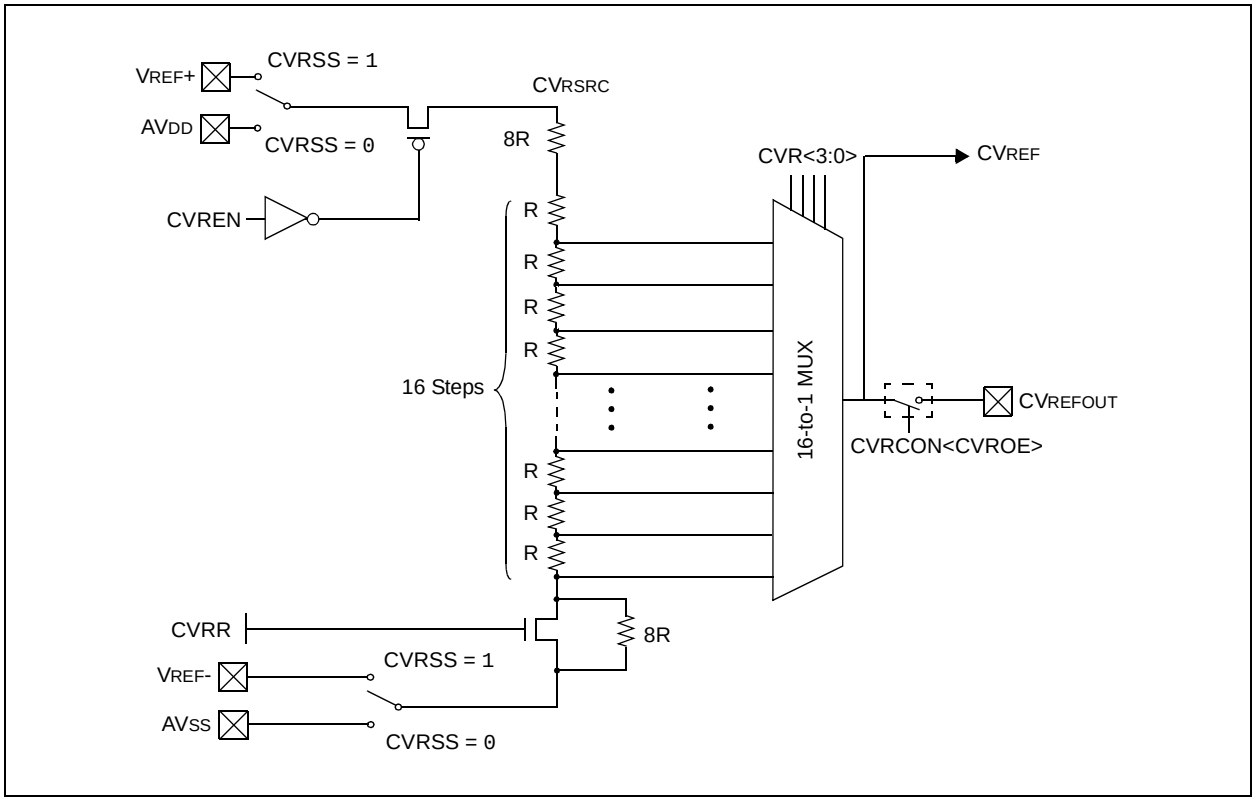
The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The comparator voltage reference has the following features:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

A block diagram of the CVREF module is illustrated in Figure 32-1.

**FIGURE 32-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM**



**NOTES:**

## 36.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

## 36.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

## 36.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## 36.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

**TABLE 37-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS (CONTINUED)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Sym.** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions(1)** |
| DO20a | VOH1 | **Output High Voltage**<br>I/O Pins:<br>4x Source Driver Pins -<br>RA3, RA9, RA10, RA14, RA15<br>RB0-RB2, RB4, RB6-RB7, RB11, RB13<br>RC12-RC15<br>RD0, RD6-RD7, RD11, RD14<br>RE8, RE9<br>RF2, RF3, RF8<br>RG15<br>RH0, RH1, RH4-RH6, RH8-RH13<br>RJ0-RJ2, RJ8, RJ9, RJ11 | 1.5 | — | — | V | IOH ≥ -14 mA, VDD = 3.3V |
| | | | 2.0 | — | — | V | IOH ≥ -12 mA, VDD = 3.3V |
| | | | 3.0 | — | — | V | IOH ≥ -7 mA, VDD = 3.3V |
| | | **Output High Voltage**<br>I/O Pins:<br>8x Source Driver Pins -<br>RA0-RA2, RA4, RA5<br>RB3, RB5, RB8-RB10, RB12, RB14, RB15<br>RC1-RC4<br>RD1-RD5, RD9, RD10, RD12, RD13, RD15<br>RE4-RE7<br>RF0, RF4, RF5, RF12, RF13<br>RG0, RG1, RG6-RG9<br>RH2, RH3, RH7, RH14, RH15<br>RJ3-RJ7, RJ10, RJ12-RJ15<br>RK0-RK7 | 1.5 | — | — | V | IOH ≥ -22 mA, VDD = 3.3V |
| | | | 2.0 | — | — | V | IOH ≥ -18 mA, VDD = 3.3V |
| | | | 3.0 | — | — | V | IOH ≥ -10 mA, VDD = 3.3V |
| | | **Output High Voltage**<br>I/O Pins:<br>12x Source Driver Pins -<br>RA6, RA7<br>RE0-RE3<br>RF1<br>RG12-RG14 | 1.5 | — | — | V | IOH ≥ -32 mA, VDD = 3.3V |
| | | | 2.0 | — | — | V | IOH ≥ -25 mA, VDD = 3.3V |
| | | | 3.0 | — | — | V | IOH ≥ -14 mA, VDD = 3.3V |

**Note 1:** Parameters are characterized, but not tested.

**FIGURE 37-2: EXTERNAL CLOCK TIMING**

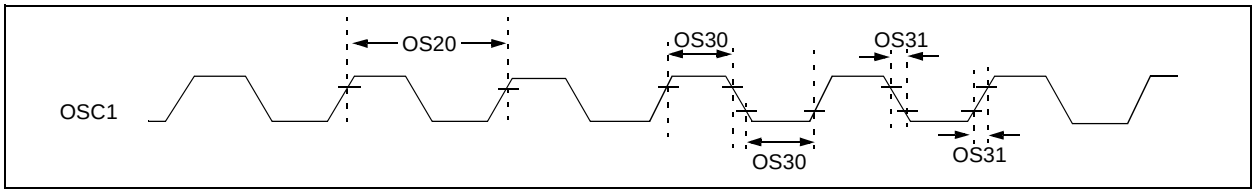



**TABLE 37-17: EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Minimum** | **Typical(1)** | **Maximum** | **Units** | **Conditions** |
| OS10 | FOSC | External CLKI Frequency (External clocks allowed only in EC and ECPLL modes) | DC | — | 64 | MHz | EC **(Note 2,3)** |
| OS13 | | Oscillator Crystal Frequency | 4 | — | 32 | MHz | HS **(Note 2,3)** |
| OS15 | | | 32 | 32.768 | 100 | kHz | SOSC **(Note 2)** |
| OS20 | TOSC | TOSC = 1/FOSC | — | — | — | — | See parameter OS10 for FOSC value |
| OS30 | TOSL, TOSH | External Clock In (OSC1) High or Low Time | 0.375 x TOSC | — | — | ns | EC **(Note 2)** |
| OS31 | TOSR, TOSF | External Clock In (OSC1) Rise or Fall Time | — | — | 7.5 | ns | EC **(Note 2)** |
| OS40 | TOST | Oscillator Start-up Timer Period (Only applies to HS, HSPLL, and SOSC Clock Oscillator modes) | — | 1024 | — | TOSC | **(Note 2)** |
| OS41 | TFSCM | Primary Clock Fail Safe Time-out Period | — | 2 | — | ms | **(Note 2)** |
| OS42 | GM | External Oscillator Transconductance | — | 400 | — | µA/V | VDD = 3.3V, TA = +25°C, HS **(Note 2)** |

**Note 1:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are characterized but are not tested.

**2:** This parameter is characterized, but not tested in manufacturing.

**3:** See parameter OS50 for PLL input frequency limitations.

## 38.1 DC Characteristics

**TABLE 38-1: OPERATING MIPS VS. VOLTAGE**

| Characteristic | VDD Range (in Volts) (Note 1) | Temp. Range (in °C) | Max. Frequency | Comment |
|---|---|---|---|---|
| | | | PIC32MZ EF Devices | |
| EDC5 | 2.1V-3.6V | -40°C to +125°C | 180 MHz | — |

**Note 1:** Overall functional device operation at VBORMIN < VDD < VDDMIN is guaranteed, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 37-5 for BOR values.

**TABLE 38-2: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +125°C for Extended | |
|---|---|---|---|---|
| Parameter No. | Typical(3) | Maximum(6) | Units | Conditions |
| **Operating Current (IDD)(1)** | | | | |
| EDC20 | 8 | 54 | mA | 4 MHz **(Note 4,5)** |
| EDC21 | 10 | 60 | mA | 10 MHz **(Note 5)** |
| EDC22 | 32 | 95 | mA | 60 MHz **(Note 2,4)** |
| EDC23 | 40 | 105 | mA | 80 MHz **(Note 2,4)** |
| EDC25 | 61 | 125 | mA | 130 MHz **(Note 2,4)** |
| EDC26 | 72 | 140 | mA | 160 MHz **(Note 2,4)** |
| EDC28 | 81 | 150 | mA | 180 MHz **(Note 2,4)** |

**Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

**2:** The test conditions for IDD measurements are as follows:

- Oscillator mode is EC+PLL with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBMD = 1), VUSB3V3 is connected to VSS
- CPU, Program Flash, and SRAM data memory are operational, Program Flash memory Wait states are equal to four
- L1 Cache and Prefetch modules are enabled
- No peripheral modules are operating, (ON bit = 0), and the associated PMD bit is set. All clocks are disabled ON bit (PBxDIV<15>) = 0 (x ≠ 1,7)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled

**3:** Data in "Typical" column is at 3.3V, +25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

**4:** This parameter is characterized, but not tested in manufacturing.

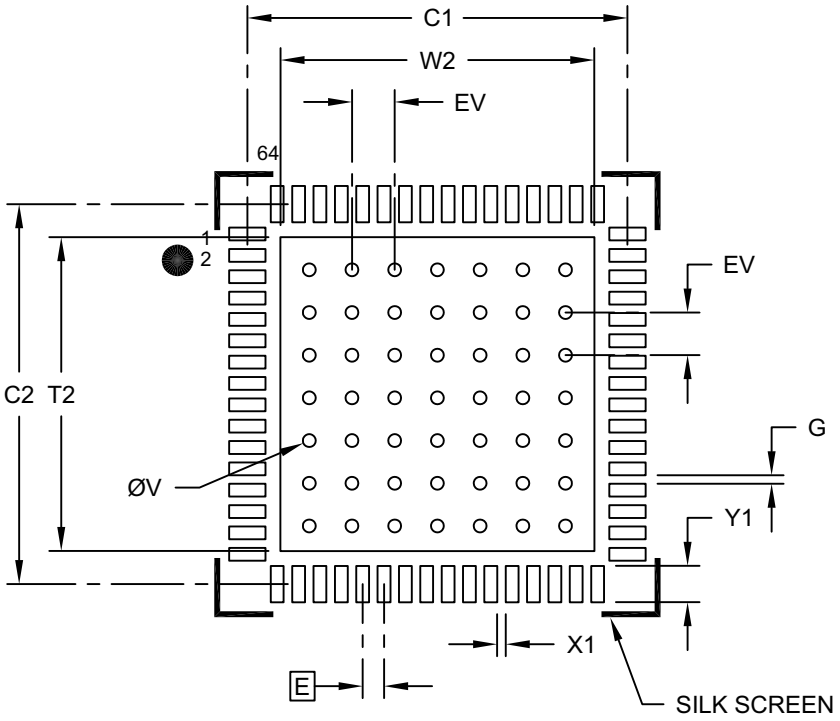
**5:** Note 2 applies with the following exceptions: L1 Cache and Prefetch modules are disabled, Program Flash memory Wait states are equal to seven.

**6:** Data in the "Maximum" column is at 3.3V, +125ºC at specified operating frequency. Parameters are for design guidance only and are not tested.

## 41.2 Package Details

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length and 7.70x7.70mm Exposed Pad

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | W2 | | | 7.50 |
| Optional Center Pad Length | T2 | | | 7.50 |
| Contact Pad Spacing | C1 | | 8.90 | |
| Contact Pad Spacing | C2 | | 8.90 | |
| Contact Pad Width (X20) | X1 | | | 0.30 |
| Contact Pad Length (X20) | Y1 | | | 0.90 |
| Contact Pad to Center Pad (X20) | G | 0.20 | | |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

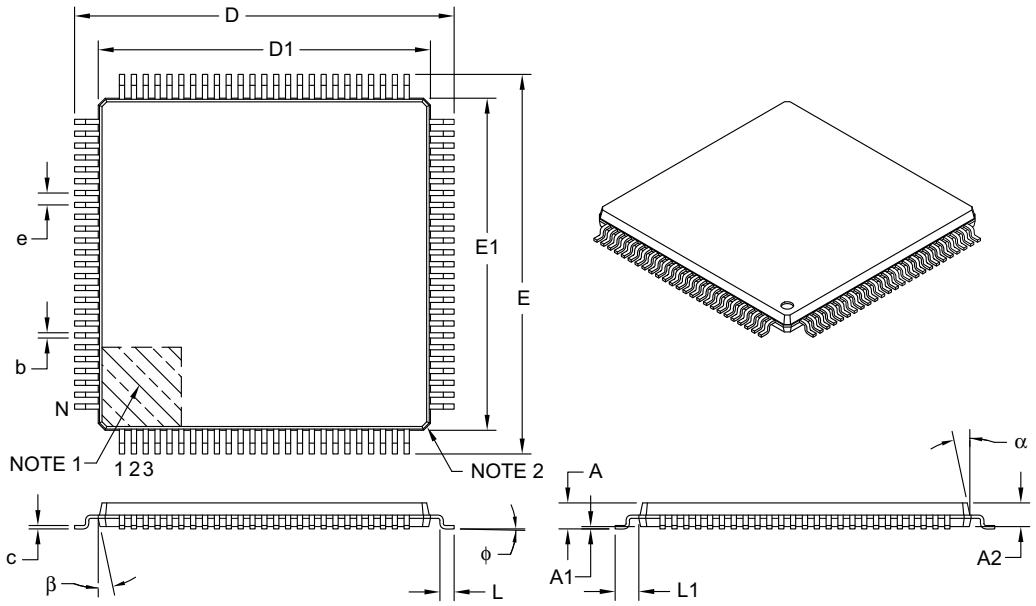
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-2213B

### 100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 100 | |
| Lead Pitch | e | | 0.50 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | | 16.00 BSC | |
| Overall Length | D | | 16.00 BSC | |
| Molded Package Width | E1 | | 14.00 BSC | |
| Molded Package Length | D1 | | 14.00 BSC | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B