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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512efe100-i-pf

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 1-2: OSCILLATOR PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
CLKI	31	49	B28	71	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	32	50	A33	72	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	31	49	B28	71	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	32	50	A33	72	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	47	72	B41	105	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	48	73	A49	106	O	—	32.768 low-power oscillator crystal output.
REFCLKI1	PPS	PPS	PPS	PPS	I	—	Reference Clock Generator Inputs 1-4
REFCLKI3	PPS	PPS	PPS	PPS	I	—	
REFCLKI4	PPS	PPS	PPS	PPS	I	—	
REFCLKO1	PPS	PPS	PPS	PPS	O	—	Reference Clock Generator Outputs 1-4
REFCLKO3	PPS	PPS	PPS	PPS	O	—	
REFCLKO4	PPS	PPS	PPS	PPS	O	—	

Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer
Analog = Analog input
O = Output
PPS = Peripheral Pin Select
P = Power
I = Input

TABLE 1-3: IC1 THROUGH IC9 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Input Capture							
IC1	PPS	PPS	PPS	PPS	I	ST	Input Capture Inputs 1-9
IC2	PPS	PPS	PPS	PPS	I	ST	
IC3	PPS	PPS	PPS	PPS	I	ST	
IC4	PPS	PPS	PPS	PPS	I	ST	
IC5	PPS	PPS	PPS	PPS	I	ST	
IC6	PPS	PPS	PPS	PPS	I	ST	
IC7	PPS	PPS	PPS	PPS	I	ST	
IC8	PPS	PPS	PPS	PPS	I	ST	
IC9	PPS	PPS	PPS	PPS	I	ST	

Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer
Analog = Analog input
O = Output
PPS = Peripheral Pin Select
P = Power
I = Input

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 5-2: NVMCON2: FLASH PROGRAMMING CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
	SWAPLOCK<1:0>		—	—	—	—	—	—

Legend:

R = Readable bit

-n = Value at POR

HC = Hardware Set

W = Writable bit

'1' = Bit is set

HC = Hardware Cleared

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-6 **SWAPLOCK<1:0>:** Flash Memory Swap Lock Control bits

11 = PFSWAP and BFSWAP are not writable and SWAPLOCK is not writable

10 = PFSWAP and BFSWAP are not writable and SWAPLOCK is writable

01 = PFSWAP and BFSWAP are not writable and SWAPLOCK is writable

00 = PFSWAP and BFSWAP are writable and SWAPLOCK is writable

bit 5-0 **Unimplemented:** Read as '0'

7.1 CPU Exceptions

CPU coprocessor 0 contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events or program errors. Table 7-1 lists the exception types in order of priority.

TABLE 7-1: MIPS32® M-CLASS MICROPROCESSOR CORE EXCEPTION TYPES

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Highest Priority						
Reset	Assertion $\overline{\text{MCLR}}$ or a Power-on Reset (POR).	0xBFC0_0000	BEV, ERL	—	—	_on_reset
Soft Reset	Assertion of a software Reset.	0xBFC0_0000	BEV, SR, ERL	—	—	_on_reset
DSS	EJTAG debug single step.	0xBFC0_0480	—	DSS	—	—
DINT	EJTAG debug interrupt. Caused by the assertion of the external EJ_DINT input or by setting the EjtagBrk bit in the ECR register.	0xBFC0_0480	—	DINT	—	—
NMI	Assertion of NMI signal.	0xBFC0_0000	BEV, NMI, ERL	—	—	_nmi_handler
Machine Check	TLB write that conflicts with an existing entry.	EBASE+0x180	MCHECK, EXL	—	0x18	_general_exception_handler
Interrupt	Assertion of unmasked hardware or software interrupt signal.	See Table 7-2.	IPL<2:0>	—	0x00	See Table 7-2.
Deferred Watch	Deferred watch (unmasked by K DM=>!(K DM) transition).	EBASE+0x180	WP, EXL	—	0x17	_general_exception_handler
DIB	EJTAG debug hardware instruction break matched.	0xBFC0_0480	—	DIB	—	—
WATCH	A reference to an address that is in one of the Watch registers (fetch).	EBASE+0x180	EXL	—	0x17	_general_exception_handler
AdEL	Fetch address alignment error. Fetch reference to protected address.	EBASE+0x180	EXL	—	0x04	_general_exception_handler
TLBL	Fetch TLB miss or fetch TLB hit to page with V = 0.	EBASE if Status.EXL = 0	—	—	0x02	—
		EBASE+0x180 if Status.EXL == 1	—	—	0x02	_general_exception_handler
TLBL Execute Inhibit	An instruction fetch matched a valid TLB entry that had the XI bit set.	EBASE+0x180	EXL	—	0x14	_general_exception_handler
IBE	Instruction fetch bus error.	EBASE+0x180	EXL	—	0x06	_general_exception_handler

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	BYTO<1:0>		WBO ⁽¹⁾	—	—	BITO
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0>				
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCEN	CRCAPP ⁽¹⁾	CRCTYP	—	—	CRCCH<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>**: CRC Byte Order Selection bits

11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)

10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)

01 = Endian byte swap on word boundaries (i.e., reverse source byte order)

00 = No swapping (i.e., source byte order)

bit 27 **WBO**: CRC Write Byte Order Selection bit⁽¹⁾

1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>

0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO**: CRC Bit Order Selection bit

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)

0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)

0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>**: Polynomial Length bits⁽¹⁾

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Denotes the length of the polynomial – 1.

bit 7 **CRCEN**: CRC Enable bit

1 = CRC module is enabled and channel transfers are routed through the CRC module

0 = CRC module is disabled and channel transfers proceed normally

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 10-5: DCRCDATA: DMA CRC DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **DCRCDATA<31:0>**: CRC Data Register bits

Writing to this register will seed the CRC generator. Reading from this register will return the current value of the CRC. Bits greater than PLEN will return '0' on any read.

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

Only the lower 16 bits contain IP header checksum information. The upper 16 bits are always '0'. Data written to this register is converted and read back in 1's complement form (i.e., current IP header checksum value).

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Bits greater than PLEN will return '0' on any read.

REGISTER 10-6: DCRCXOR: DMA CRCXOR ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **DCRCXOR<31:0>**: CRC XOR Register bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

This register is unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

1 = Enable the XOR input to the Shift register

0 = Disable the XOR input to the Shift register; data is shifted in directly from the previous stage in the register

TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address (BF8E #)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
309C	USB E3RXA	31:16	—	RXHUBPRT<6:0>						MULTTRAN	RXHUBADD<6:0>						0000		
		15:0	—	—	—	—	—	—	—	—	RXFADDR<6:0>						0000		
30A0	US BE4TXA	31:16	—	TXHUBPRT<6:0>						MULTTRAN	TXHUBADD<6:0>						0000		
		15:0	—	—	—	—	—	—	—	—	TXFADDR<6:0>						0000		
30A4	USB E4RXA	31:16	—	RXHUBPRT<6:0>						MULTTRAN	RXHUBADD<6:0>						0000		
		15:0	—	—	—	—	—	—	—	—	RXFADDR<6:0>						0000		
30A8	USB E5TXA	31:16	—	TXHUBPRT<6:0>						MULTTRAN	TXHUBADD<6:0>						0000		
		15:0	—	—	—	—	—	—	—	—	TXFADDR<6:0>						0000		
30AC	USB E5RXA	31:16	—	RXHUBPRT<6:0>						MULTTRAN	RXHUBADD<6:0>						0000		
		15:0	—	—	—	—	—	—	—	—	RXFADDR<6:0>						0000		
30B0	USB E6TXA	31:16	—	TXHUBPRT<6:0>						MULTTRAN	TXHUBADD<6:0>						0000		
		15:0	—	—	—	—	—	—	—	—	TXFADDR<6:0>						0000		
30B4	USB E6RXA	31:16	—	RXHUBPRT<6:0>						MULTTRAN	RXHUBADD<6:0>						0000		
		15:0	—	—	—	—	—	—	—	—	RXFADDR<6:0>						0000		
30B8	USB E7TXA	31:16	—	TXHUBPRT<6:0>						MULTTRAN	TXHUBADD<6:0>						0000		
		15:0	—	—	—	—	—	—	—	—	TXFADDR<6:0>						0000		
30BC	USB E7RXA	31:16	—	RXHUBPRT<6:0>						MULTTRAN	RXHUBADD<6:0>						0000		
		15:0	—	—	—	—	—	—	—	—	RXFADDR<6:0>						0000		
3100	USB E0CSR0	31:16	Indexed by the same bits in USBIE0CSR0																0000
		15:0																	0000
3108	USB E0CSR2	31:16	Indexed by the same bits in USBIE0CSR2																0000
		15:0																	0000
310C	USB E0CSR3	31:16	Indexed by the same bits in USBIE0CSR3																0000
		15:0																	0000
3110	USB E1CSR0	31:16	Indexed by the same bits in USBIE1CSR0																0000
		15:0																	0000
3114	USB E1CSR1	31:16	Indexed by the same bits in USBIE1CSR1																0000
		15:0																	0000
3118	USB E1CSR2	31:16	Indexed by the same bits in USBIE1CSR2																0000
		15:0																	0000
311C	USB E1CSR3	31:16	Indexed by the same bits in USBIE1CSR3																0000
		15:0																	0000
3120	USB E2CSR0	31:16	Indexed by the same bits in USBIE2CSR0																0000
		15:0																	0000
3124	USB E2CSR1	31:16	Indexed by the same bits in USBIE2CSR1																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: Device mode.
 - 2: Host mode.
 - 3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
 - 4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

REGISTER 11-1: USBCSR0: USB CONTROL STATUS REGISTER 0 (CONTINUED)

- bit 10 **RESUME:** Resume from Suspend control bit
 1 = Generate Resume signaling when the device is in Suspend mode
 0 = Stop Resume signaling
- In *Device mode*, the software should clear this bit after 10 ms (a maximum of 15 ms) to end Resume signaling. In *Host mode*, the software should clear this bit after 20 ms.
- bit 9 **SUSPMODE:** Suspend Mode status bit
 1 = The USB module is in Suspend mode
 0 = The USB module is in Normal operations
- This bit is read-only in *Device mode*. In *Host mode*, it can be set by software, and is cleared by hardware.
- bit 8 **SUSPEN:** Suspend Mode Enable bit
 1 = Suspend mode is enabled
 0 = Suspend mode is not enabled
- bit 7 **Unimplemented:** Read as '0'
- bit 6-0 **FUNC<6:0>:** Device Function Address bits
- These bits are only available in *Device mode*. This field is written with the address received through a SET_ADDRESS command, which will then be used for decoding the function address in subsequent token packets.

TABLE 12-22: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
14DC	SS6R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS6R<3:0>				0000
14E0	C1RXR ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C1RXR<3:0>				0000
14E4	C2RXR ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C2RXR<3:0>				0000
14E8	REFCLKI1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFCLKI1R<3:0>				0000
14F0	REFCLKI3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFCLKI3R<3:0>				0000
14F4	REFCLKI4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFCLKI4R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: This register is not available on 64-pin devices.
 2: This register is not available on devices without a CAN module.

14.2 Timer2-Timer9 Control Registers

TABLE 14-1: TIMER2 THROUGH TIMER9 REGISTER MAP

Virtual Address (BF84_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0210	TMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
0220	PR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>																FFFF
0400	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
0410	TMR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR3<15:0>																0000
0420	PR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR3<15:0>																FFFF
0600	T4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0610	TMR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR4<15:0>																0000
0620	PR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR4<15:0>																FFFF
0800	T5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
0810	TMR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR5<15:0>																0000
0820	PR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR5<15:0>																FFFF
0A00	T6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0A10	TMR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR6<15:0>																0000
0A20	PR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR6<15:0>																FFFF
0C00	T7CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

TABLE 14-1: TIMER2 THROUGH TIMER9 REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0C10	TMR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR7<15:0>																0000
0C20	PR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR7<15:0>																FFFF
0E00	T8CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0E10	TMR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR8<15:0>																0000
0E20	PR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR8<15:0>																FFFF
1000	T9CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
1010	TMR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR9<15:0>																0000
1020	PR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR9<15:0>																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 20-18: SQI1BDPOLLCON: SQI BUFFER DESCRIPTOR POLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLLCON<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLLCON<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **POLLCON<15:0>**: Buffer Descriptor Processor Poll Status bits

These bits indicate the number of cycles the BDP would wait before refetching the descriptor control word if the previous descriptor fetched was disabled.

REGISTER 20-19: SQI1BDTXDSTAT: SQI BUFFER DESCRIPTOR DMA TRANSMIT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-x	R-x	R-x	R-x	U-0
	—	—	—	TXSTATE<3:0>				—
23:16	U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
	—	—	—	TXBUFCNT<4:0>				—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	TXCURBUFLEN<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-25 **TXSTATE<3:0>**: Current DMA Transmit State Status bits

These bits provide information on the current DMA receive states.

bit 24-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFCNT<4:0>**: DMA Buffer Byte Count Status bits

These bits provide information on the internal FIFO space.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **TXCURBUFLEN<7:0>**: Current DMA Transmit Buffer Length Status bits

These bits provide the length of the current DMA transmit buffer.

21.0 INTER-INTEGRATED CIRCUIT (I²C)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. “Inter-Integrated Circuit (I²C)”** (DS60001116) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

The I²C module provides complete hardware support for both Slave and Multi-Master modes of the I²C serial communication standard.

Each I²C module has a 2-pin interface:

- SCLx pin is clock
- SDAx pin is data

Each I²C module offers the following key features:

- I²C interface supporting both master and slave operation
- I²C Slave mode supports 7-bit and 10-bit addressing
- I²C Master mode supports 7-bit and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking
- SMBus support

Figure 21-1 illustrates the I²C module block diagram.

23.0 PARALLEL MASTER PORT (PMP)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. “Parallel Master Port (PMP)”** (DS60001128) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

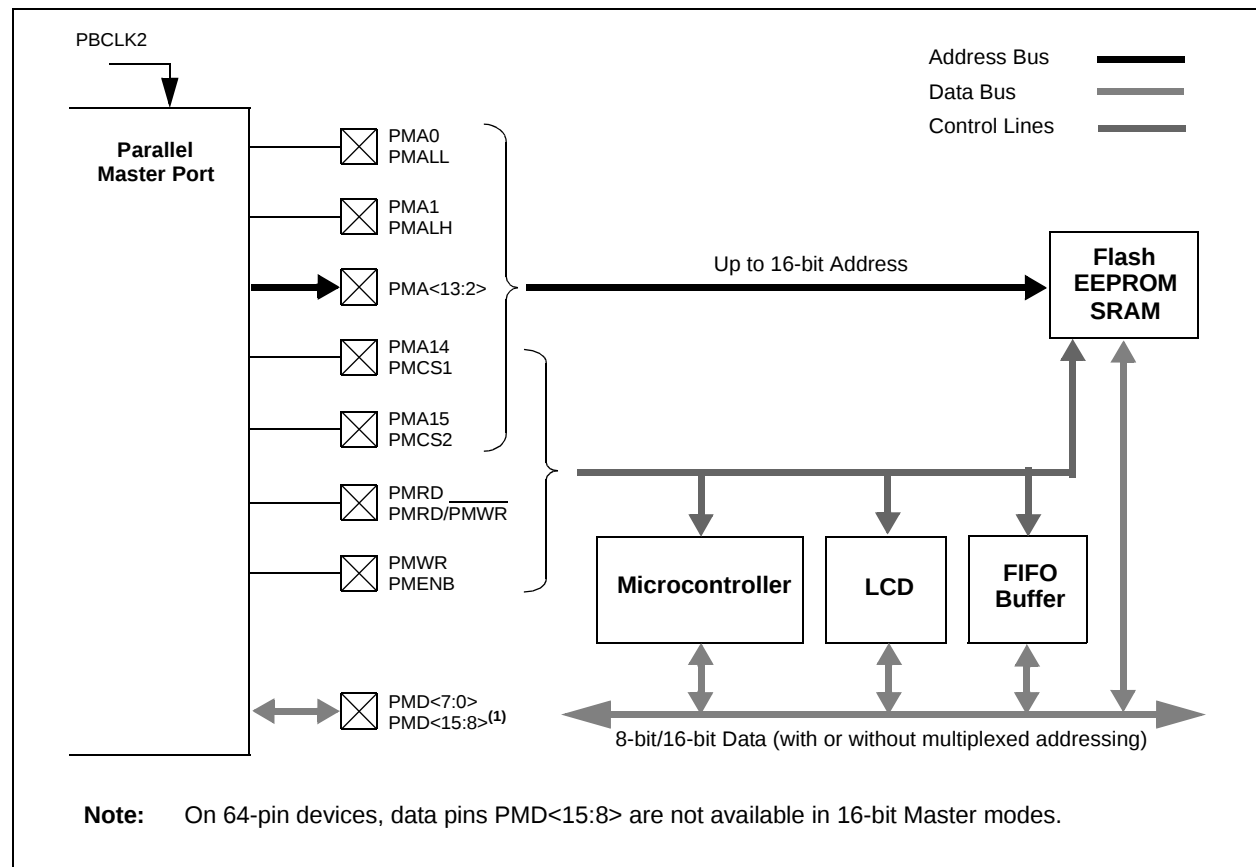
The PMP is a parallel 8-bit/16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

The following are key features of the PMP module:

- 8-bit,16-bit interface
- Up to 16 programmable address lines
- Up to two Chip Select lines
- Programmable strobe options:
 - Individual read and write strobes, or
 - Read/write strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Parallel Slave Port support:
 - Legacy addressable
 - Address support
 - 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Operate during Sleep and Idle modes
- Separate configurable read/write registers or dual buffers for Master mode
- Fast bit manipulation using CLR, SET, and INV registers

Note: On 64-pin devices, data pins PMD<15:8> are not available in 16-bit Master modes.

FIGURE 23-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 28-14: ADCCMPENx: ADC DIGITAL COMPARATOR 'x' ENABLE REGISTER
(‘x’ = 1 THROUGH 6)**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 CMPE31 ⁽¹⁾	R/W-0 CMPE30 ⁽¹⁾	R/W-0 CMPE29 ⁽¹⁾	R/W-0 CMPE28 ⁽¹⁾	R/W-0 CMPE27 ⁽¹⁾	R/W-0 CMPE26 ⁽¹⁾	R/W-0 CMPE25 ⁽¹⁾	R/W-0 CMPE24 ⁽¹⁾
23:16	R/W-0 CMPE23 ⁽¹⁾	R/W-0 CMPE22 ⁽¹⁾	R/W-0 CMPE21 ⁽¹⁾	R/W-0 CMPE20 ⁽¹⁾	R/W-0 CMPE19 ⁽¹⁾	R/W-0 CMPE18	R/W-0 CMPE17	R/W-0 CMPE16
15:8	R/W-0 CMPE15	R/W-0 CMPE14	R/W-0 CMPE13	R/W-0 CMPE12	R/W-0 CMPE11	R/W-0 CMPE10	R/W-0 CMPE9	R/W-0 CMPE8
7:0	R/W-0 CMPE7	R/W-0 CMPE6	R/W-0 CMPE5	R/W-0 CMPE4	R/W-0 CMPE3	R/W-0 CMPE2	R/W-0 CMPE1	R/W-0 CMPE0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **CMPE31:CMPE0**: ADC Digital Comparator 'x' Enable bits^(2,3)

These bits enable conversion results corresponding to the Analog Input to be processed by the Digital Comparator. CMPE0 enables AN0, CMPE1 enables AN1, and so on.

Note 1: This bit is not available on 64-pin devices.

2: CMPE_x = AN_x, where 'x' = 0-31 (Digital Comparator inputs are limited to AN0 through AN31).

3: Changing the bits in this register while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 32-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	CVROE	CVRR	CVRSS	CVR<3:0>			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator Voltage Reference On bit

1 = Module is enabled

Setting this bit does not affect other bits in the register.

0 = Module is disabled and does not consume current.

Clearing this bit does not affect the other bits in the register.

bit 14-7 **Unimplemented:** Read as '0'

bit 6 **CVROE:** CVREFOUT Enable bit

1 = Voltage level is output on CVREFOUT pin

0 = Voltage level is disconnected from CVREFOUT pin

bit 5 **CVRR:** CVREF Range Selection bit

1 = 0 to 0.67 CVRSRC, with CVRSRC/24 step size

0 = 0.25 CVRSRC to 0.75 CVRSRC, with CVRSRC/32 step size

bit 4 **CVRSS:** CVREF Source Selection bit

1 = Comparator voltage reference source, $CVRSRC = (VREF+) - (VREF-)$

0 = Comparator voltage reference source, $CVRSRC = AVDD - AVSS$

bit 3-0 **CVR<3:0>:** CVREF Value Selection $0 \leq CVR<3:0> \leq 15$ bits

When CVRR = 1:

$CVREF = (CVR<3:0>/24) \cdot (CVRSRC)$

When CVRR = 0:

$CVREF = 1/4 \cdot (CVRSRC) + (CVR<3:0>/32) \cdot (CVRSRC)$

TABLE 34-5: DEVICE ADC CALIBRATION SUMMARY

Virtual Address (BFC5_#)	Register Name	Bit Range	Bits															All Resets ⁽¹⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
4000	DEVADC0	31:16	ADC Calibration Data <31:16>															xxxx
		15:0	ADC Calibration Data <15:0>															xxxx
4004	DEVADC1	31:16	ADC Calibration Data <31:16>															xxxx
		15:0	ADC Calibration Data <15:0>															xxxx
4008	DEVADC2	31:16	ADC Calibration Data <31:16>															xxxx
		15:0	ADC Calibration Data <15:0>															xxxx
400C	DEVADC3	31:16	ADC Calibration Data <31:16>															xxxx
		15:0	ADC Calibration Data <15:0>															xxxx
4010	DEVADC4	31:16	ADC Calibration Data <31:16>															xxxx
		15:0	ADC Calibration Data <15:0>															xxxx
401C	DEVADC7	31:16	ADC Calibration Data <31:16>															xxxx
		15:0	ADC Calibration Data <15:0>															xxxx

Legend: x = unknown value on Reset.

Note 1: Reset values are dependent on the device variant.

NOTES:

NOTES:

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 37-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Param.	Sym.	Characteristic	Min.	Typ.	Max.	Units	Conditions ⁽¹⁾
DO10	VOL	Output Low Voltage I/O Pins 4x Sink Driver Pins - RA3, RA9, RA10, RA14, RA15 RB0-RB2, RB4, RB6, RB7, RB11, RB13 RC12-RC15 RD0, RD6-RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8 RG15 RH0, RH1, RH4-RH6, RH8-RH13 RJ0-RJ2, RJ8, RJ9, RJ11	—	—	0.4	V	$I_{OL} \leq 10 \text{ mA}$, $V_{DD} = 3.3\text{V}$
		Output Low Voltage I/O Pins: 8x Sink Driver Pins - RA0-RA2, RA4, RA5 RB3, RB5, RB8-RB10, RB12, RB14, RB15 RC1-RC4 RD1-RD5, RD9, RD10, RD12, RD13, RD15 RE4-RE7 RF0, RF4, RF5, RF12, RF13 RG0, RG1, RG6-RG9 RH2, RH3, RH7, RH14, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	—	—	0.4	V	$I_{OL} \leq 15 \text{ mA}$, $V_{DD} = 3.3\text{V}$
		Output Low Voltage I/O Pins: 12x Sink Driver Pins - RA6, RA7 RE0-RE3 RF1 RG12-RG14	—	—	0.4	V	$I_{OL} \leq 20 \text{ mA}$, $V_{DD} = 3.3\text{V}$

Note 1: Parameters are characterized, but not tested.

NOTES: