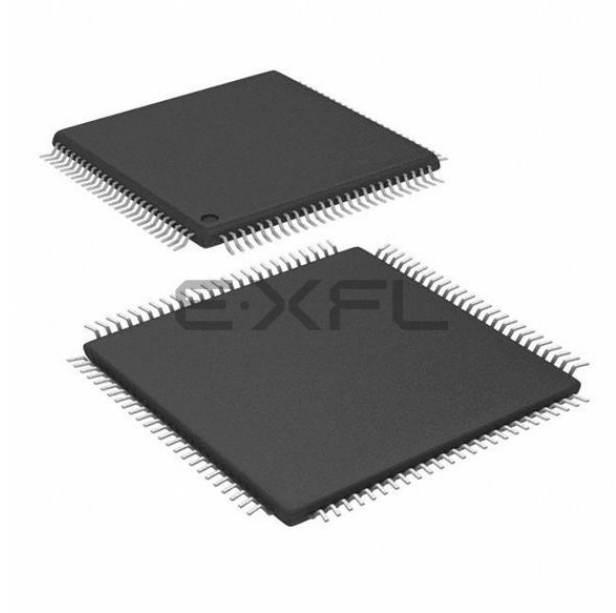
Microchip Technology - PIC32MZ0512EFE100T-I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512efe100t-i-pt

2.9 Designing for High-Speed Peripherals

The PIC32MZ EF family devices have peripherals that operate at frequencies much higher than typical for an embedded environment. Table 2-1 lists the peripherals that produce high-speed signals on their external pins:

TABLE 2-1: PERIPHERALS THAT PRODUCE HS SIGNALS ON EXTERNAL PINS

Peripheral	High-Speed Signal Pins	Maximum Speed on Signal Pin
EBI	EBIAx, EBIDx	50 MHz
SQI1	SQICLK, SQICSx, SQIDx	50 MHz
HS USB	D+, D-	480 MHz

Due to these high-speed signals, it is important to consider several factors when designing a product that uses these peripherals, as well as the PCB on which these components will be placed. Adhering to these recommendations will help achieve the following goals:

- Minimize the effects of electromagnetic interference to the proper operation of the product
- Ensure signals arrive at their intended destination at the same time
- Minimize crosstalk
- Maintain signal integrity
- Reduce system noise
- Minimize ground bounce and power sag

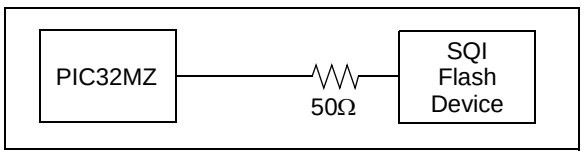
2.9.1 SYSTEM DESIGN

2.9.1.1 Impedance Matching

When selecting parts to place on high-speed buses, particularly the SQI bus, if the impedance of the peripheral device does not match the impedance of the pins on the PIC32MZ EF device to which it is connected, signal reflections could result, thereby degrading the quality of the signal.

If it is not possible to select a product that matches impedance, place a series resistor at the load to create the matching impedance. See Figure 2-4 for an example.

FIGURE 2-4: SERIES RESISTOR



2.9.1.2 PCB Layout Recommendations

The following list contains recommendations that will help ensure the PCB layout will promote the goals previously listed.

- **Component Placement**
  - Place bypass capacitors as close to their component power and ground pins as possible, and place them on the same side of the PCB
  - Devices on the same bus that have larger setup times should be placed closer to the PIC32MZ EF device
- **Power and Ground**
  - Multi-layer PCBs will allow separate power and ground planes
  - Each ground pin should be connected to the ground plane individually
  - Place bypass capacitor vias as close to the pad as possible (preferably inside the pad)
  - If power and ground planes are not used, maximize width for power and ground traces
  - Use low-ESR, surface-mount bypass capacitors
- **Clocks and Oscillators**
  - Place crystals as close as possible to the PIC32MZ EF device OSC/SOSC pins
  - Do not route high-speed signals near the clock or oscillator
  - Avoid via usage and branches in clock lines (SQICLK)
  - Place termination resistors at the end of clock lines
- **Traces**
  - Higher-priority signals should have the shortest traces
  - Match trace lengths for parallel buses (EBIAx, EBIDx, SQIDx)
  - Avoid long run lengths on parallel traces to reduce coupling
  - Make the clock traces as straight as possible
  - Use rounded turns rather than right-angle turns
  - Have traces on different layers intersect on right angles to minimize crosstalk
  - Maximize the distance between traces, preferably no less than three times the trace width
  - Power traces should be as short and as wide as possible
  - High-speed traces should be placed close to the ground plane

TABLE 3-3: COPROCESSOR 0 REGISTERS (CONTINUED)

Register Number	Register Name	Function
12	Status	Processor status and control.
	IntCtl	Interrupt control of vector spacing.
	SRSCtl	Shadow register set control.
	SRSMap	Shadow register mapping control.
	View_IPL	Allows the Priority Level to be read/written without extracting or inserting that bit from/to the Status register.
	SRSMAP2	Contains two 4-bit fields that provide the mapping from a vector number to the shadow set number to use when servicing such an interrupt.
13	Cause	Describes the cause of the last exception.
	NestedExc	Contains the error and exception level status bit values that existed prior to the current exception.
	View_RIPL	Enables read access to the RIPL bit that is available in the Cause register.
14	EPC	Program counter at last exception.
	NestedEPC	Contains the exception program counter that existed prior to the current exception.
15	PRID	Processor identification and revision
	Ebase	Exception base address of exception vectors.
	CDMMBase	Common device memory map base.
16	Config	Configuration register.
	Config1	Configuration register 1.
	Config2	Configuration register 2.
	Config3	Configuration register 3.
	Config4	Configuration register 4.
	Config5	Configuration register 5.
	Config7	Configuration register 7.
17	LLAddr	Load link address (MPU only).
18	WatchLo	Low-order watchpoint address (MPU only).
19	WatchHi	High-order watchpoint address (MPU only).
20-22	Reserved	Reserved in the PIC32 core.
23	Debug	EJTAG debug register.
	TraceControl	EJTAG trace control.
	TraceControl2	EJTAG trace control 2.
	UserTraceData1	EJTAG user trace data 1 register.
	TraceBPC	EJTAG trace breakpoint register.
	Debug2	Debug control/exception status 1.
24	DEPC	Program counter at last debug exception.
	UserTraceData2	EJTAG user trace data 2 register.
25	PerfCtl0	Performance counter 0 control.
	PerfCnt0	Performance counter 0.
	PerfCtl1	Performance counter 1 control.
	PerfCnt1	Performance counter 1.
26	ErrCtl	Software test enable of way-select and data RAM arrays for I-Cache and D-Cache (MPU only).
27	Reserved	Reserved in the PIC32 core.
28	TagLo/DataLo	Low-order portion of cache tag interface (MPU only).
29	Reserved	Reserved in the PIC32 core.
30	ErrorEPC	Program counter at last error exception.
31	DeSave	Debug exception save.

TABLE 4-19: SYSTEM BUS TARGET 11 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
AC20	SBT11ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
AC24	SBT11ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
AC28	SBT11ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
AC30	SBT11ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
AC38	SBT11ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
AC40	SBT11REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
AC50	SBT11RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
AC58	SBT11WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
AC60	SBT11REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
AC70	SBT11RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
AC78	SBT11WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

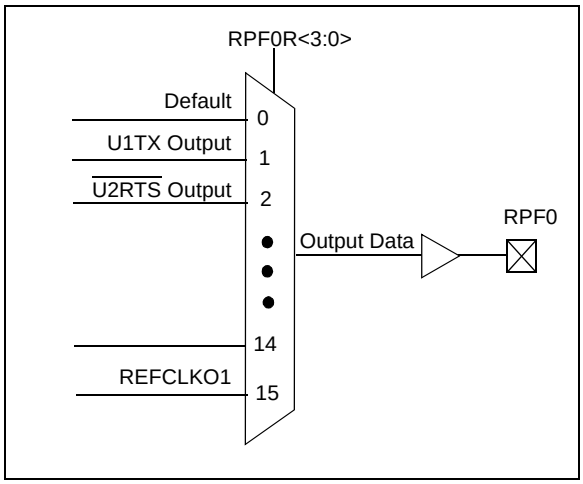
Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

12.4.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the PPS options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPnR registers (Register 12-2) are used to control output mapping. Like the [*pin name*]R registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 12-3 and Figure 12-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 12-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPF0



12.4.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32MZ EF devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

12.4.6.1 Control Register Lock

Under normal operation, writes to the RPnR and [*pin name*]R registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK Configuration bit (CFGCON<13>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** in the *"PIC32 Family Reference Manual"* for details.

12.4.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPnR and [*pin name*]R registers. The IOL1WAY Configuration bit (DEVCFG3<29>) blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.

18.1 Output Compare Control Registers

TABLE 18-2: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 9 REGISTER MAP

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4000	OC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4010	OC1R	31:16	OC1R<31:0>																xxxx
		15:0																	xxxx
4020	OC1RS	31:16	OC1RS<31:0>																xxxx
		15:0																	xxxx
4200	OC2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4210	OC2R	31:16	OC2R<31:0>																xxxx
		15:0																	xxxx
4220	OC2RS	31:16	OC2RS<31:0>																xxxx
		15:0																	xxxx
4400	OC3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4410	OC3R	31:16	OC3R<31:0>																xxxx
		15:0																	xxxx
4420	OC3RS	31:16	OC3RS<31:0>																xxxx
		15:0																	xxxx
4600	OC4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4610	OC4R	31:16	OC4R<31:0>																xxxx
		15:0																	xxxx
4620	OC4RS	31:16	OC4RS<31:0>																xxxx
		15:0																	xxxx
4800	OC5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4810	OC5R	31:16	OC5R<31:0>																xxxx
		15:0																	xxxx
4820	OC5RS	31:16	OC5RS<31:0>																xxxx
		15:0																	xxxx

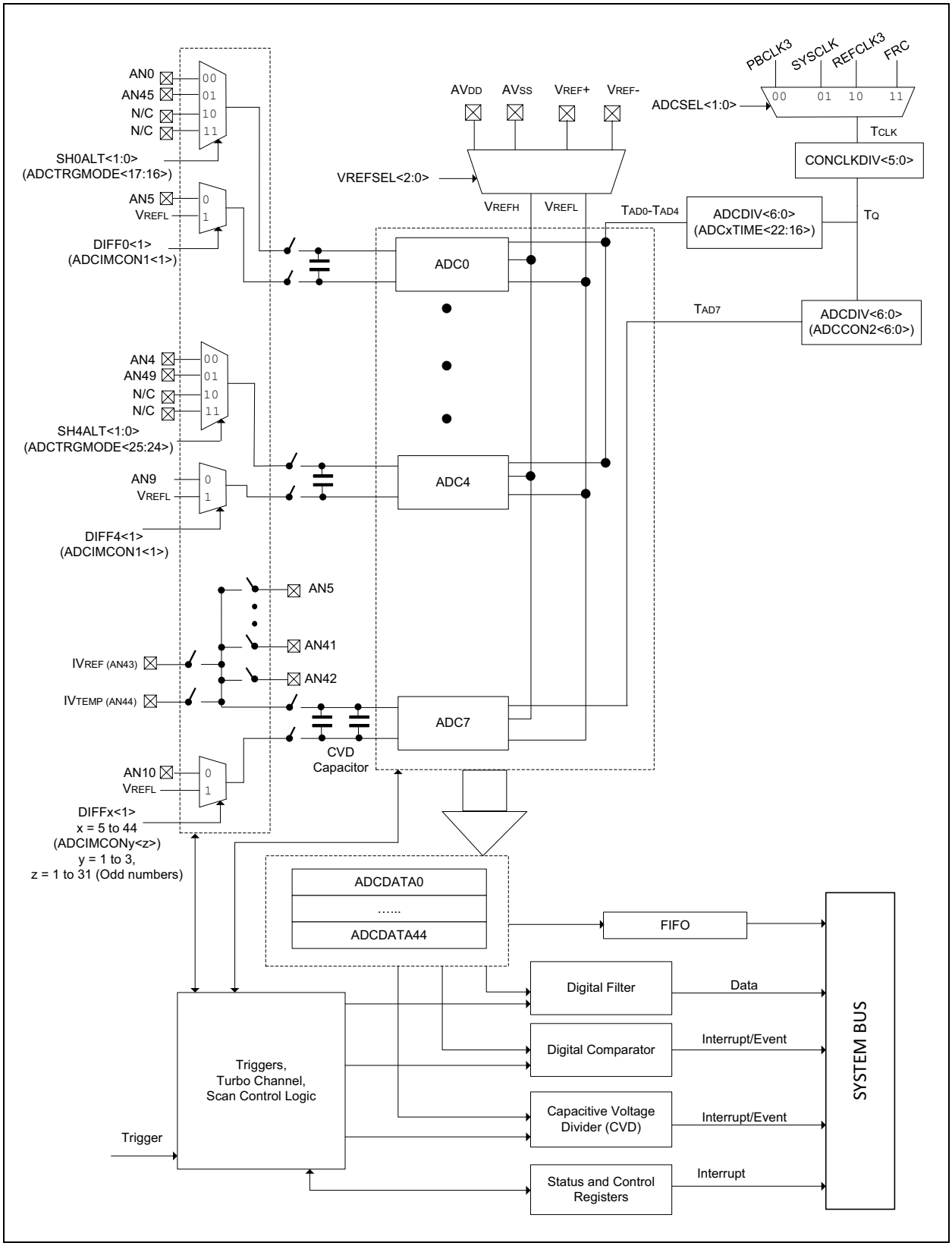
Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

TABLE 26-4: CRYPTO ENGINE SECURITY ASSOCIATION STRUCTURE (CONTINUED)

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SA_ENCIV1	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV2	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV3	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV4	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							

FIGURE 28-1: ADC BLOCK DIAGRAM



REGISTER 28-17: ADCTRG1: ADC TRIGGER SOURCE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC3<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC2<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC1<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC0<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC3<4:0>:** Trigger Source for Conversion of Analog Input AN3 Select bits
11111 = Reserved
•
•
•
01101 = Reserved
01100 = Comparator 2 (COUT)
01011 = Comparator 1 (COUT)
01010 = OCMP5
01001 = OCMP3
01000 = OCMP1
00111 = TMR5 match
00110 = TMR3 match
00101 = TMR1 match
00100 = INT0 External interrupt
00011 = STRIG
00010 = Global level software trigger (GLSWTRG)
00001 = Global software edge Trigger (GSWTRG)
00000 = No Trigger

For STRIG, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSS*x* registers.

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TRGSRC2<4:0>:** Trigger Source for Conversion of Analog Input AN2 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC1<4:0>:** Trigger Source for Conversion of Analog Input AN1 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC0<4:0>:** Trigger Source for Conversion of Analog Input AN0 Select bits
See bits 28-24 for bit value definitions.

REGISTER 28-25: ADCDATAx: ADC OUTPUT DATA REGISTER ('x' = 0 THROUGH 44)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>:** ADC Converted Data Output bits.

Note 1: The registers, ADCDATA19 through ADCDATA34, are not available on 64-pin devices.

2: The registers, ADCDATA35 through ADCDATA42, are not available on 64-pin and 100-pin devices.

3: When an alternate input is used as the input source for a dedicated ADC module, the data output is still read from the Primary input Data Output Register.

4: Reading the ADCDATAx register value after changing the FRACT bit converts the data into the format specified by FRACT bit.

REGISTER 29-1: CiCON: CAN MODULE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	S/HC-0	R/W-1	R/W-0	R/W-0
	—	—	—	—	ABAT	REQOP<2:0>		
23:16	R-1	R-0	R-0	R/W-0	U-0	U-0	U-0	U-0
	OPMOD<2:0>			CANCAP	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R-0	U-0	U-0	U-0
	ON(1)	—	SIDLE	—	CANBUSY	—	—	—
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DNCNT<4:0>				

Legend:	HC = Hardware Clear	S = Settable bit	
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-28 **Unimplemented:** Read as ‘0’

bit 27 **ABAT:** Abort All Pending Transmissions bit
1 = Signal all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions aborted

bit 26-24 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved - Do not use
101 = Reserved - Do not use
100 = Set Configuration mode
011 = Set Listen Only mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode

bit 23-21 **OPMOD<2:0>:** Operation Mode Status bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 20 **CANCAP:** CAN Message Receive Time Stamp Timer Capture Enable bit
1 = CANTMR value is stored on valid message reception and is stored with the message
0 = Disable CAN message receive time stamp timer capture and stop CANTMR to conserve power

bit 19-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** CAN On bit(1)
1 = CAN module is enabled
0 = CAN module is disabled

bit 14 **Unimplemented:** Read as ‘0’

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

REGISTER 29-17: CiFLTCON7: CAN FILTER CONTROL REGISTER 7 (CONTINUED)

bit 15 **FLTEN29:** Filter 29 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL29<1:0>:** Filter 29 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL29<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN28:** Filter 28 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL28<1:0>:** Filter 28 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL28<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-38: EMAC1SA1: ETHERNET CONTROLLER MAC STATION ADDRESS 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR4<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR3<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STNADDR4<7:0>:** Station Address Octet 4 bits
These bits hold the fourth transmitted octet of the station address.

bit 7-0 **STNADDR3<7:0>:** Station Address Octet 3 bits
These bits hold the third transmitted octet of the station address.

Note 1: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

2: This register is loaded at reset from the factory preprogrammed station address.

33.3 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 33-1 for more information.

Note:	Disabling a peripheral module while it's ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits.

TABLE 33-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS(1)

Peripheral	PMDx bit Name	Register Name and Bit Location
ADC	ADCMD	PMD1<0>
Comparator Voltage Reference	CVRMD	PMD1<12>
Comparator 1	CMP1MD	PMD2<0>
Comparator 2	CMP2MD	PMD2<1>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Input Capture 6	IC6MD	PMD3<5>
Input Capture 7	IC7MD	PMD3<6>
Input Capture 8	IC8MD	PMD3<7>
Input Capture 9	IC9MD	PMD3<8>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Output Compare 6	OC6MD	PMD3<21>
Output Compare 7	OC7MD	PMD3<22>
Output Compare 8	OC8MD	PMD3<23>
Output Compare 9	OC9MD	PMD3<24>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
Timer6	T6MD	PMD4<5>
Timer7	T7MD	PMD4<6>
Timer8	T8MD	PMD4<7>
Timer9	T9MD	PMD4<8>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>

Note 1: Not all modules and associated PMDx bits are available on all devices. See **TABLE 1: "PIC32MZ EF Family Features"** for the lists of available peripherals.

2: Module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

TABLE 33-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS(1) (CONTINUED)

Peripheral	PMDx bit Name	Register Name and Bit Location
UART3	U3MD	PMD5<2>
UART4	U4MD	PMD5<3>
UART5	U5MD	PMD5<4>
UART6	U6MD	PMD5<5>
SPI1	SPI1MD	PMD5<8>
SPI2	SPI2MD	PMD5<9>
SPI3	SPI3MD	PMD5<10>
SPI4	SPI4MD	PMD5<11>
SPI5	SPI5MD	PMD5<12>
SPI6	SPI6MD	PMD5<13>
I2C1	I2C1MD	PMD5<16>
I2C2	I2C2MD	PMD5<17>
I2C3	I2C3MD	PMD5<18>
I2C4	I2C4MD	PMD5<19>
I2C5	I2C5MD	PMD5<20>
USB(2)	USBMD	PMD5<24>
CAN1	CAN1MD	PMD5<28>
CAN2	CAN2MD	PMD5<29>
RTCC	RTCCMD	PMD6<0>
Reference Clock Output 1	REFO1MD	PMD6<8>
Reference Clock Output 2	REFO2MD	PMD6<9>
Reference Clock Output 3	REFO3MD	PMD6<10>
Reference Clock Output 4	REFO4MD	PMD6<11>
PMP	PMPMD	PMD6<16>
EBI	EBIMD	PMD6<17>
SQI1	SQI1MD	PMD6<23>
Ethernet	ETHMD	PMD6<28>
DMA	DMAMD	PMD7<4>
Random Number Generator	RNGMD	PMD7<20>
Crypto	CRYPTMD	PMD7<22>

Note 1: Not all modules and associated PMDx bits are available on all devices. See **TABLE 1: "PIC32MZ EF Family Features"** for the lists of available peripherals.

2: Module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

REGISTER 34-9: CFGEBIC: EXTERNAL BUS INTERFACE CONTROL PIN CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0
	EBI RDYINV3	EBI RDYINV2	EBI RDYIN1	—	EBI RDYEN3	EBI RDYEN2	EBI RDYEN1	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	EBIRDYLVL	EBIRPEN
15:8	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	—	EBIWEEN	EBIOEEN	—	—	EBIBSEN1	EBIBSEN0
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	EBICSEN3	EBICSEN2	EBICSEN1	EBICSEN0	—	—	EBIDEN1	EBIDEN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **EBIRDYINV3:** EBIRDY3 Inversion Control bit
1 = Invert EBIRDY3 pin before use
0 = Do not invert EBIRDY3 pin before use

bit 30 **EBIRDYINV2:** EBIRDY2 Inversion Control bit
1 = Invert EBIRDY2 pin before use
0 = Do not invert EBIRDY2 pin before use

bit 29 **EBIRDYINV1:** EBIRDY1 Inversion Control bit
1 = Invert EBIRDY1 pin before use
0 = Do not invert EBIRDY1 pin before use

bit 28 **Unimplemented:** Read as '0'

bit 27 **EBIRDYEN3:** EBIRDY3 Pin Enable bit
1 = EBIRDY3 pin is enabled for use by the EBI module
0 = EBIRDY3 pin is available for general use

bit 26 **EBIRDYEN2:** EBIRDY2 Pin Enable bit
1 = EBIRDY2 pin is enabled for use by the EBI module
0 = EBIRDY2 pin is available for general use

bit 25 **EBIRDYEN1:** EBIRDY1 Pin Enable bit
1 = EBIRDY1 pin is enabled for use by the EBI module
0 = EBIRDY1 pin is available for general use

bit 24-18 **Unimplemented:** Read as '0'

bit 17 **EBIRDYLVL:** EBIRDYx Pin Sensitivity Control bit
1 = Use level detect for EBIRDYx pins
0 = Use edge detect for EBIRDYx pins

bit 16 **EBIRPEN:** $\overline{\text{EBIRP}}$ Pin Sensitivity Control bit
1 = $\overline{\text{EBIRP}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIRP}}$ pin is available for general use

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **EBIWEEN:** $\overline{\text{EBIWE}}$ Pin Enable bit
1 = $\overline{\text{EBIWE}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIWE}}$ pin is available for general use

Note: When EBIMD = 1, the bits in this register are ignored and the pins are available for general use.

TABLE 37-14: COMPARATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	—	±10	—	mV	AVDD = VDD, AVSS = VSS
D301	VICM	Input Common Mode Voltage	0	—	VDD	V	AVDD = VDD, AVSS = VSS **(Note 2)**
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	Max VICM = (VDD – 1)V **(Note 2, 4)**
D303	TRESP	Response Time	—	150	—	ns	AVDD = VDD, AVSS = VSS **(Notes 1, 2)**
D304	ON2OV	Comparator Enabled to Output Valid	—	—	10	µs	Comparator module is configured before setting the comparator ON bit **(Note 2)**
D305	IVREF	Internal Voltage Reference	1.194	1.2	1.206	V	—

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

2: These parameters are characterized but not tested.

3: The Comparator module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

4: CMRR measurement characterized with a 1 MΩ resistor in parallel with a 25 pF capacitor to VSS.

TABLE 37-15: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time	—	—	10	µs	See **Note 1**
D313	DACREFH	CVREF Input Voltage Reference Range	AVSS	—	AVDD	V	CVRSRC with CVRSS = 0
			VREF-	—	VREF+	V	CVRSRC with CVRSS = 1
D314	DVREF	CVREF Programmable Output Range	0	—	0.625 x DACREFH	V	0 to 0.625 DACREFH with DACREFH/24 step size
			0.25 x DACREFH	—	0.719 x DACREFH	V	0.25 x DACREFH to 0.719 DACREFH with DACREFH/32 step size
D315	DACRES	Resolution	—	—	DACREFH/24		CVRCON<CVRR> = 1
			—	—	DACREFH/32		CVRCON<CVRR> = 0
D316	DACACC	Absolute Accuracy(2)	—	—	1/4	LSB	DACREFH/24, CVRCON<CVRR> = 1
			—	—	1/2	LSB	DACREFH/32, CVRCON<CVRR> = 0

Note 1: Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

2: These parameters are characterized but not tested.

TABLE 37-18: SYSTEM TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
OS51	FSYS	System Frequency	DC	—	200	MHz	USB module disabled
			60	—	200	MHz	USB module enabled
OS55a	FPB	Peripheral Bus Frequency	DC	—	100	MHz	For PBCLKx, 'x' ≠ 4, 7
OS55b			DC	—	200	MHz	For PBCLK4, PBCLK7
OS56	FREF	Reference Clock Frequency	—	—	50	MHz	For REFCLKI1, 3, 4 and REFCLKO1, 3, 4 pins

TABLE 37-19: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
OS50	FIN	PLL Input Frequency Range	5	—	64	MHz	ECPLL, HSPLL, FRCPLL modes
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	100	µs	—
OS53	DCLK	CLKO Stability(2) (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period
OS54	FVCO	PLL VCO Frequency Range	350	—	700	MHz	—
OS54a	FPLL	PLL Output Frequency Range	10	—	200	MHz	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

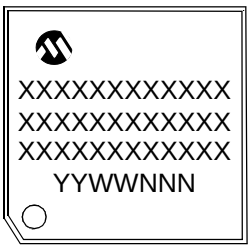
$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{PBCLK2}{CommunicationClock}}}$$

For example, if PBCLK2 = 100 MHz and SPI bit rate = 50 MHz, the effective jitter is as follows:

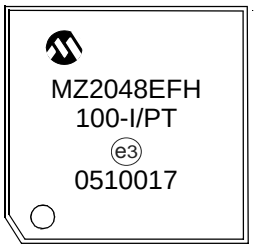
$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{100}{50}}} = \frac{D_{CLK}}{1.41}$$

41.1 Package Marking Information (Continued)

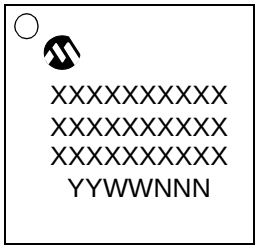
100-Lead TQFP (12x12x1 mm)



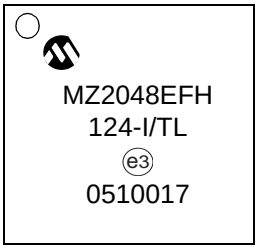
Example



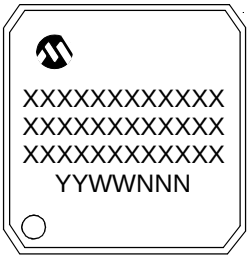
124-Lead VTLA (9x9x0.9 mm)



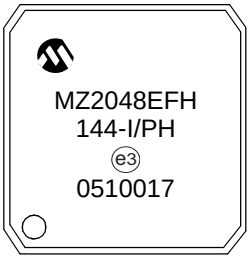
Example



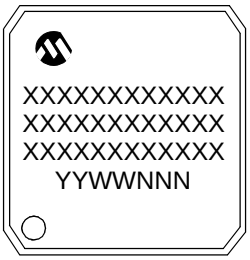
144-Lead TQFP (16x16x1 mm)



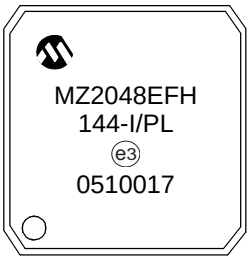
Example



144-Lead LQFP (20x20x1.40 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

A.3 CPU

The CPU in the PIC32MZ EF family of devices has been changed to the MIPS32 M-Class MPU architecture. This CPU includes DSP ASE, internal data and instruction L1 caches, and a TLB-based MMU.

Table A-4 summarizes some of the key differences (indicated by **Bold** type) in the internal CPU registers.

TABLE A-4: CPU DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
L1 Data and Instruction Cache and Prefetch Wait States	
On PIC32MX devices, the cache was included in the prefetch module outside the CPU. PREFEN<1:0> (**CHECON**<5:4>) **11 = Enable predictive prefetch for both cacheable and non-cacheable regions** **10 = Enable predictive prefetch for non-cacheable regions only** **01 = Enable predictive prefetch for cacheable regions only** 00 = Disable predictive prefetch DCSZ<1:0> (CHECON<9:8>) Changing these bits causes all lines to be reinitialized to the "invalid" state. 11 = Enable data caching with a size of 4 lines 10 = Enable data caching with a size of 2 lines 01 = Enable data caching with a size of 1 line 00 = Disable data caching CHECOH (CHECON<16>) 1 = Invalidate all data and instruction lines 0 = Invalidate all data and instruction lines that are not locked	On PIC32MZ EF devices, the CPU has a separate L1 instruction and data cache in the core. The PREFEN<1:0> bits still enable the prefetch module; however, the K0<2:0> bits in the CP0 registers controls the internal L1 cache for the designated regions. PREFEN<1:0> (**PRECON**<5:4>) **11 = Enable predictive prefetch for any address** **10 = Enable predictive prefetch for CPU instructions and CPU data** **01 = Enable predictive prefetch for CPU instructions only** 00 = Disable predictive prefetch **K0<2:0> (CP0 Reg 16, Select 0)** **011 = Cacheable, non-coherent, write-back, write allocate** **010 = Uncached** **001 = Cacheable, non-coherent, write-through, write allocate** **000 = Cacheable, non-coherent, write-through, no write allocate**
PFMWS<2:0> (**CHECON**<2:0>) 111 = Seven Wait states 110 = Six Wait states 101 = Five Wait states 100 = Four Wait states 011 = Three Wait states 010 = Two Wait states **(61-80 MHz)** 001 = One Wait state **(31-60 MHz)** 000 = Zero Wait state **(0-30 MHz)**	The Program Flash Memory read wait state frequency points have changed in PIC32MZ EF devices. The register for accessing the PFMWS field has changed from CHECON to PRECON. PFMWS<2:0> (**PRECON**<2:0>) 111 = Seven Wait states • • • 100 = Four Wait states **(200-252 MHz)** 011 = Reserved 010 = Two Wait states **(133-200 MHz)** 001 = One Wait state **(66-133 MHz)** 000 = Zero Wait states **(0-66 MHz)** **Note:** Wait states listed are for ECC enabled.
Core Instruction Execution	
On PIC32MX devices, the CPU can execute MIPS16e instructions and uses a 16-bit instruction set, which reduces memory size. **MIPS16e®**	On PIC32MZ EF devices, the CPU can operate a mode called microMIPS. microMIPS mode is an enhanced MIPS32® instruction set that uses both 16-bit and 32-bit opcodes. This mode of operation reduces memory size with minimum performance impact. **microMIPS™** The BOOTISA (DEVCFG0<6>) Configuration bit controls the MIPS32 and microMIPS modes for boot and exception code. 1 = Boot code and Exception code is MIPS32® (ISAONEXC bit is set to '0' and the ISA<1:0> bits are set to '10' in the CP0 Config3 register) 0 = Boot code and Exception code is microMIPS™ (ISAONEXC bit is set to '1' and the ISA<1:0> bits are set to '11' in the CP0 Config3 register)