Microchip Technology - PIC32MZ0512EFE124-E/TL Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	97
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512efe124-e-tl

1.0 DEVICE OVERVIEW

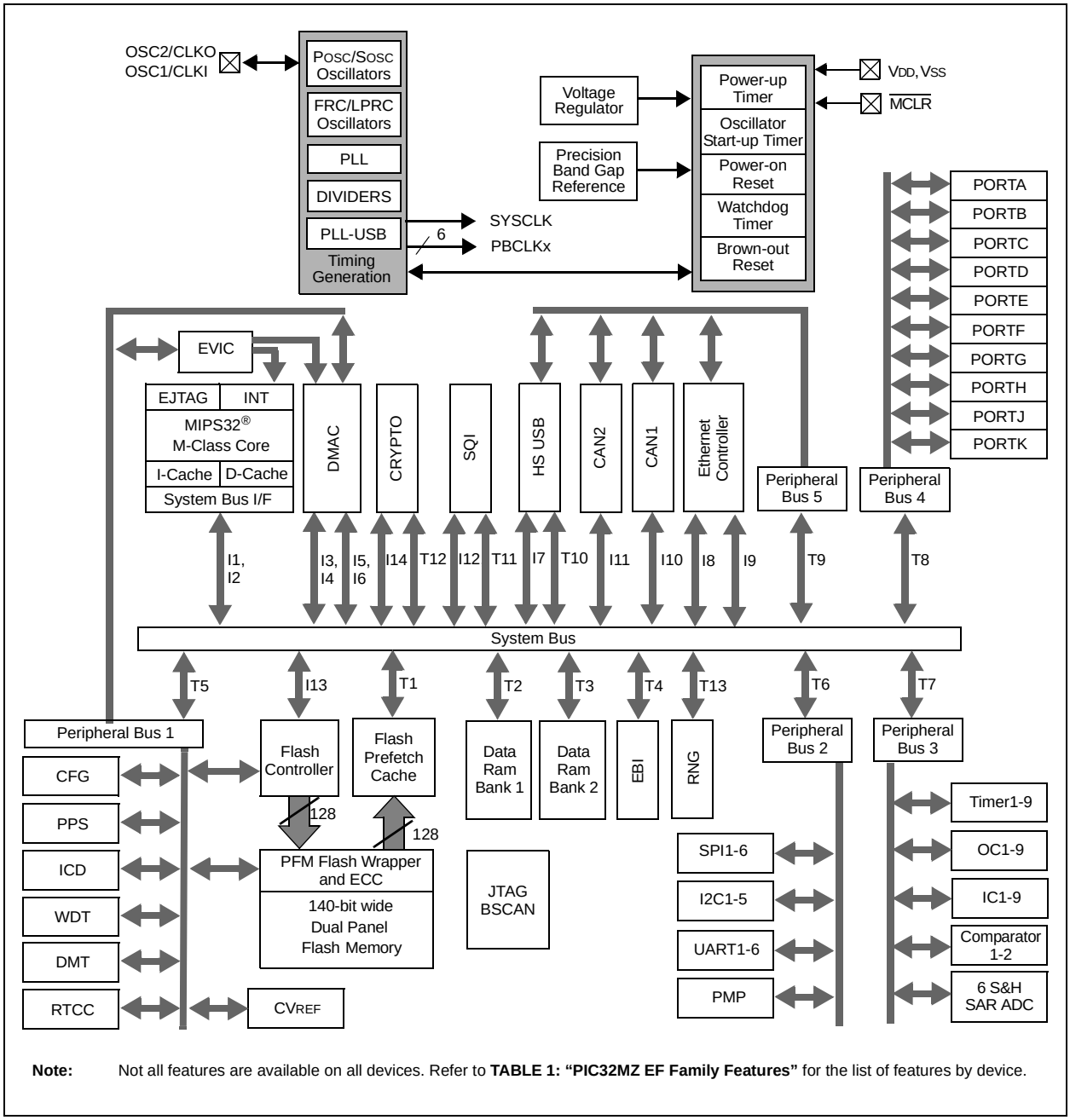
Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This data sheet contains device-specific information for PIC32MZ EF devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MZ EF family of devices.

Table 1-21 through Table 1-22 list the pinout I/O descriptions for the pins shown in the device pin tables (see Table 2 through Table 5).

FIGURE 1-1: PIC32MZ EF FAMILY BLOCK DIAGRAM



Note: Not all features are available on all devices. Refer to **TABLE 1: "PIC32MZ EF Family Features"** for the list of features by device.

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTA							
RA0	—	17	A11	22	I/O	ST	PORTA is a bidirectional I/O port
RA1	—	38	B21	56	I/O	ST	
RA2	—	59	A41	85	I/O	ST	
RA3	—	60	B34	86	I/O	ST	
RA4	—	61	A42	87	I/O	ST	
RA5	—	2	B1	2	I/O	ST	
RA6	—	89	A61	129	I/O	ST	
RA7	—	90	B51	130	I/O	ST	
RA9	—	28	B15	39	I/O	ST	
RA10	—	29	A20	40	I/O	ST	
RA14	—	66	B37	95	I/O	ST	
RA15	—	67	A45	96	I/O	ST	
PORTB							
RB0	16	25	A18	36	I/O	ST	PORTB is a bidirectional I/O port
RB1	15	24	A17	35	I/O	ST	
RB2	14	23	A16	34	I/O	ST	
RB3	13	22	A14	31	I/O	ST	
RB4	12	21	A13	26	I/O	ST	
RB5	11	20	B11	25	I/O	ST	
RB6	17	26	B14	37	I/O	ST	
RB7	18	27	A19	38	I/O	ST	
RB8	21	32	B18	47	I/O	ST	
RB9	22	33	A23	48	I/O	ST	
RB10	23	34	B19	49	I/O	ST	
RB11	24	35	A24	50	I/O	ST	
RB12	27	41	A27	59	I/O	ST	
RB13	28	42	B23	60	I/O	ST	
RB14	29	43	A28	61	I/O	ST	
RB15	30	44	B24	62	I/O	ST	
PORTC							
RC1	—	6	B3	6	I/O	ST	PORTC is a bidirectional I/O port
RC2	—	7	A6	11	I/O	ST	
RC3	—	8	B5	12	I/O	ST	
RC4	—	9	A7	13	I/O	ST	
RC12	31	49	B28	71	I/O	ST	
RC13	47	72	B41	105	I/O	ST	
RC14	48	73	A49	106	I/O	ST	
RC15	32	50	A33	72	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

TABLE 1-10: I2C1 THROUGH I2C5 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Inter-Integrated Circuit 1							
SCL1	44	66	B37	95	I/O	ST	I2C1 Synchronous Serial Clock Input/Output
SDA1	43	67	A45	96	I/O	ST	I2C1 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 2							
SCL2	—	59	A41	85	I/O	ST	I2C2 Synchronous Serial Clock Input/Output
SDA2	—	60	B34	86	I/O	ST	I2C2 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 3							
SCL3	51	58	A39	80	I/O	ST	I2C3 Synchronous Serial Clock Input/Output
SDA3	50	57	B31	79	I/O	ST	I2C3 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 4							
SCL4	6	12	B7	16	I/O	ST	I2C4 Synchronous Serial Clock Input/Output
SDA4	5	11	A8	15	I/O	ST	I2C4 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 5							
SCL5	42	65	A44	91	I/O	ST	I2C5 Synchronous Serial Clock Input/Output
SDA5	41	64	B36	90	I/O	ST	I2C5 Synchronous Serial Data Input/Output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-11: COMPARATOR 1, COMPARATOR 2 AND CVREF PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Comparator Voltage Reference							
CVREF+	16	29	A20	40	I	Analog	Comparator Voltage Reference (High) Input
CVREF-	15	28	B15	39	I	Analog	Comparator Voltage Reference (Low) Input
CVREFOUT	23	34	B19	49	O	Analog	Comparator Voltage Reference Output
Comparator 1							
C1INA	11	20	B11	25	I	Analog	Comparator 1 Positive Input
C1INB	12	21	A13	26	I	Analog	Comparator 1 Selectable Negative Input
C1INC	5	11	A8	15	I	Analog	
C1IND	4	10	B6	14	I	Analog	
C1OUT	PPS	PPS	PPS	PPS	O	—	Comparator 1 Output
Comparator 2							
C2INA	13	22	A14	31	I	Analog	Comparator 2 Positive Input
C2INB	14	23	A16	34	I	Analog	Comparator 2 Selectable Negative Input
C2INC	10	16	B9	21	I	Analog	
C2IND	6	12	B7	16	I	Analog	
C2OUT	PPS	PPS	PPS	PPS	O	—	Comparator 2 Output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

3.7 M-Class Core Configuration

Register 3-1 through Register 3-4 show the default configuration of the M-Class core, which is included on the PIC32MZ EF family of devices.

REGISTER 3-1: CONFIG: CONFIGURATION REGISTER; CP0 REGISTER 16, SELECT 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	ISP
23:16	R-0	R-0	R-1	R-0	U-0	R-1	R-0	R-0
	DSP	UDI	SB	MDU	—	MM<1:0>		BM
15:8	R-0	R-0	R-0	R-0	R-0	R-1	R-0	R-0
	BE	AT<1:0>		AR<2:0>			MT<2:1>	
7:0	R-1	U-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-0
	MT<0>	—	—	—	—	K0<2:0>		

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to '1' to indicate the presence of the Config1 register.

bit 30-25 **Unimplemented:** Read as '0'

bit 24 **ISP:** Instruction Scratch Pad RAM bit
0 = Instruction Scratch Pad RAM is not implemented

bit 23 **DSP:** Data Scratch Pad RAM bit
0 = Data Scratch Pad RAM is not implemented

bit 22 **UDI:** User-defined bit
0 = CorExtend User-Defined Instructions are not implemented

bit 21 **SB:** SimpleBE bit
1 = Only Simple Byte Enables are allowed on the internal bus interface

bit 20 **MDU:** Multiply/Divide Unit bit
0 = Fast, high-performance MDU

bit 19 **Unimplemented:** Read as '0'

bit 18-17 **MM<1:0>:** Merge Mode bits
10 = Merging is allowed

bit 16 **BM:** Burst Mode bit
0 = Burst order is sequential

bit 15 **BE:** Endian Mode bit
0 = Little-endian

bit 14-13 **AT<1:0>:** Architecture Type bits
00 = MIPS32

bit 12-10 **AR<2:0>:** Architecture Revision Level bits
001 = MIPS32 Release 2

bit 9-7 **MT<2:0>:** MMU Type bits
001 = M-Class MPU Microprocessor core uses a TLB-based MMU

bit 6-3 **Unimplemented:** Read as '0'

bit 2-0 **K0<2:0>:** Kseg0 Coherency Algorithm bits
011 = Cacheable, non-coherent, write-back, write allocate
010 = Uncached
001 = Cacheable, non-coherent, write-through, write allocate
000 = Cacheable, non-coherent, write-through, no write allocate
All other values are not used and mapped to other values. 100, 101, and 110 are mapped to 010. 111 is mapped to 010.

REGISTER 3-10: FCSR: FLOATING POINT CONTROL AND STATUS REGISTER; CP1 REGISTER 31

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	FCC<7:1>							FS
23:16	R/W-x	R/W-x	R/W-x	R-0	R-1	R-1	R/W-x	R/W-x
	FCC<0>	FO	FN	MAC2008	ABS2008	NAN2008	CAUSE<5:4>	
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CAUSE<3:0>				ENABLES<4:1>			
					V	Z	O	U
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	ENABLES<0>	FLAGS<4:0>					RM<1:0>	
	I	V	Z	O	U	I		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-25 **FCC<7:1>:** Floating Point Condition Code bits
These bits record the results of floating point compares and are tested for floating point conditional branches and conditional moves.

bit 24 **FS:** Flush to Zero control bit
1 = Denormal input operands are flushed to zero. Tiny results are flushed to either zero or the applied format's smallest normalized number (MinNorm) depending on the rounding mode settings.
0 = Denormal input operands result in an Unimplemented Operation exception.

bit 23 **FCC<0>:** Floating Point Condition Code bits
These bits record the results of floating point compares and are tested for floating point conditional branches and conditional moves.

bit 22 **FO:** Flush Override Control bit
1 = The intermediate result is kept in an internal format, which can be perceived as having the usual mantissa precision but with unlimited exponent precision and without forcing to a specific value or taking an exception.
0 = Handling of Tiny Result values depends on setting of the FS bit.

bit 21 **FN:** Flush to Nearest Control bit
1 = Final result is rounded to either zero or 2E_min (MinNorm), whichever is closest when in Round to Nearest (RN) rounding mode. For other rounding modes, a final result is given as if FS was set to 1.
0 = Handling of Tiny Result values depends on setting of the FS bit.

bit 20 **MAC2008:** Fused Multiply Add mode control bit
0 = Unfused multiply-add. Intermediary multiplication results are rounded to the destination format.

bit 19 **ABS2008:** Absolute value format control bit
1 = ABS.fmt and NEG.fmt instructions compliant with IEEE Standard 754-2008. The ABS and NEG functions accept QNAN inputs without trapping.

bit 18 **NAN2008:** NaN Encoding control bit
1 = Quiet and signaling NaN encodings recommended by the IEEE Standard 754-2008. A quiet NaN is encoded with the first bit of the fraction being 1 and a signaling NaN is encoded with the first bit of the fraction being 0.

bit 17-12 **CAUSE<5:0>:** FPU Exception Cause bits
These bits indicated the exception conditions that arise during execution of an FPU arithmetic instruction.

bit 17 **E:** Unimplemented Operation bit

REGISTER 8-8: CLKSTAT: OSCILLATOR CLOCK STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R-0	R-0	U-0	R-0	R-0	R-0
	—	—	LPRCRDY	SOSCRDY	—	POSCRDY	DIVSPLLRDY	FRCRDY

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5 **LPRCRDY**: Low-Power RC (LPRC) Oscillator Ready Status bit
1 = LPRC is stable and ready
0 = LPRC is disabled or not operating

bit 4 **SOSCRDY:** Secondary Oscillator (SOSC) Ready Status bit
1 = SOSC is stable and ready
0 = SOSC is disabled or not operating

bit 3 **Unimplemented:** Read as '0'

bit 2 **POSCRDY:** Primary Oscillator (POSC) Ready Status bit
1 = POSC is stable and ready
0 = POSC is disabled or not operating

bit 1 **DIVSPLLRDY:** Divided System PLL Ready Status bit
1 = Divided System PLL is ready
0 = Divided System PLL is not ready

bit 0 **FRCRDY:** Fast RC (FRC) Oscillator Ready Status bit
1 = FRC is stable and ready
0 = FRC is disabled for not operating

NOTES:

REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9) (CONTINUED)

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer Clock Source Select bit(1)
1 = External clock from TxCK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

Note 1: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, Timer5, Timer7, and Timer9). All timer functions are set through the even numbered timers.

2: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

3: This bit is available only on even numbered timers (Timer2, Timer4, Timer6, and Timer8).

REGISTER 19-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

bit 4 **DISSDI:** Disable SDI bit(4)
1 = SDI pin is not used by the SPI module (pin is controlled by PORT function)
0 = SDI pin is controlled by the SPI module

bit 3-2 **STXISEL<1:0>:** SPI Transmit Buffer Empty Interrupt Mode bits
11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
10 = Interrupt is generated when the buffer is empty by one-half or more
01 = Interrupt is generated when the buffer is completely empty
00 = Interrupt is generated when the last transfer is shifted out of SPISR and transmit operations are complete

bit 1-0 **SRXISEL<1:0>:** SPI Receive Buffer Full Interrupt Mode bits
11 = Interrupt is generated when the buffer is full
10 = Interrupt is generated when the buffer is full by one-half or more
01 = Interrupt is generated when the buffer is not empty
00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)

Note 1: This bit can only be written when the ON bit = 0. Refer to **Section 37.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: This bit present for legacy compatibility and is superseded by PPS functionality on these devices (see **Section 12.4 "Peripheral Pin Select (PPS)"** for more information).

REGISTER 28-15: ADCCMPx: ADC DIGITAL COMPARATOR 'x' LIMIT VALUE REGISTER ('x' = 1 THROUGH 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPHI<15:8>(1,2,3)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPHI<7:0>(1,2,3)							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPLO<15:8>(1,2,3)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPLO<7:0>(1,2,3)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **DCMPHI<15:0>:** Digital Comparator 'x' High Limit Value bits(1,2,3)

These bits store the high limit value, which is used by digital comparator for comparisons with ADC converted data.

bit 15-0 **DCMPLO<15:0>:** Digital Comparator 'x' Low Limit Value bits(1,2,3)

These bits store the low limit value, which is used by digital comparator for comparisons with ADC converted data.

Note 1: Changing theses bits while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

2: The format of the limit values should match the format of the ADC converted value in terms of sign and fractional settings.

3: For Digital Comparator 0 used in CVD mode, the DCMPHI<15:0> and DCMPLO<15:0> bits must always be specified in signed format, as the CVD output data is differential and is always signed.

REGISTER 28-16: ADCFLTRx: ADC DIGITAL FILTER 'x' REGISTER ('x' = 1 THROUGH 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC
	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	CHNLID<4:0>				
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	FLTRDATA<15:8>							
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	FLTRDATA<7:0>							

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **AFEN:** Digital Filter 'x' Enable bit
1 = Digital filter is enabled
0 = Digital filter is disabled and the AFRDY status bit is cleared

bit 30 **DATA16EN:** Filter Significant Data Length bit
1 = All 16 bits of the filter output data are significant
0 = Only the first 12 bits are significant, followed by four zeros
Note: This bit is significant only if DFMODE = 1 (Averaging Mode) and FRACT (ADCCON1<23>) = 1 (Fractional Output Mode).

bit **DFMODE:** ADC Filter Mode bit
1 = Filter 'x' works in Averaging mode
0 = Filter 'x' works in Oversampling Filter mode (default)

bit 28-26 **OVRSAM<2:0>:** Oversampling Filter Ratio bits
If DFMODE is '0':
111 = 128 samples (shift sum 3 bits to right, output data is in 15.1 format)
110 = 32 samples (shift sum 2 bits to right, output data is in 14.1 format)
101 = 8 samples (shift sum 1 bit to right, output data is in 13.1 format)
100 = 2 samples (shift sum 0 bits to right, output data is in 12.1 format)
011 = 256 samples (shift sum 4 bits to right, output data is 16 bits)
010 = 64 samples (shift sum 3 bits to right, output data is 15 bits)
001 = 16 samples (shift sum 2 bits to right, output data is 14 bits)
000 = 4 samples (shift sum 1 bit to right, output data is 13 bits)

If DFMODE is '1':
111 = 256 samples (256 samples to be averaged)
110 = 128 samples (128 samples to be averaged)
101 = 64 samples (64 samples to be averaged)
100 = 32 samples (32 samples to be averaged)
011 = 16 samples (16 samples to be averaged)
010 = 8 samples (8 samples to be averaged)
001 = 4 samples (4 samples to be averaged)
000 = 2 samples (2 samples to be averaged)

bit 25 **AFGIEN:** Digital Filter 'x' Interrupt Enable bit
1 = Digital filter interrupt is enabled and is generated by the AFRDY status bit
0 = Digital filter is disabled

29.1 CAN Control Registers

Note: The 'i' shown in register names denotes CAN1 or CAN2.

TABLE 29-1: CAN1 REGISTER SUMMARY FOR PIC32MZXXXXECF AND PIC32MZXXXXECH DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	C1CON	31:16	—	—	—	—	ABAT	REQOP<2:0>			OPMOD<2:0>			CANCAP	—	—	—	—	0480
		15:0	ON	—	SIDLE	—	CANBUSY	—	—	—	—	—	—	DNCNT<4:0>					0000
0010	C1CFG	31:16	—	—	—	—	—	—	—	—	—	WAKFIL	—	—	—	SEG2PH<2:0>			0000
		15:0	SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			SJW<1:0>		BRP<5:0>						0000
0020	C1INT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE	0000
		15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF	—	—	—	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF	0000
0030	C1VEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	FILHIT<4:0>					—	ICODE<6:0>							0040
0040	C1TREC	31:16	—	—	—	—	—	—	—	—	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000
		15:0	TERRCNT<7:0>								RERRCNT<7:0>								0000
0050	C1FSTAT	31:16	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16	0000
		15:0	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0	0000
0060	C1RXOVF	31:16	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
		15:0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
0070	C1TMR	31:16	CANTS<15:0>																0000
		15:0	CANTSPRE<15:0>																0000
0080	C1RXM0	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
0090	C1RXM1	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
00A0	C1RXM2	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
00B0	C1RXM3	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
00C0	C1FLTCON0	31:16	FLTEN3	MSEL3<1:0>		FSEL3<4:0>					FLTEN2	MSEL2<1:0>		FSEL2<4:0>					0000
		15:0	FLTEN1	MSEL1<1:0>		FSEL1<4:0>					FLTEN0	MSEL0<1:0>		FSEL0<4:0>					0000
00D0	C1FLTCON1	31:16	FLTEN7	MSEL7<1:0>		FSEL7<4:0>					FLTEN6	MSEL6<1:0>		FSEL6<4:0>					0000
		15:0	FLTEN5	MSEL5<1:0>		FSEL5<4:0>					FLTEN4	MSEL4<1:0>		FSEL4<4:0>					0000
00E0	C1FLTCON2	31:16	FLTEN11	MSEL11<1:0>		FSEL11<4:0>					FLTEN10	MSEL10<1:0>		FSEL10<4:0>					0000
		15:0	FLTEN9	MSEL9<1:0>		FSEL9<4:0>					FLTEN8	MSEL8<1:0>		FSEL8<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 29-10: CiFLTCON0: CAN FILTER CONTROL REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN3	MSEL3<1:0>		FSEL3<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN2	MSEL2<1:0>		FSEL2<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN1	MSEL1<1:0>		FSEL1<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN0	MSEL0<1:0>		FSEL0<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN3:** Filter 3 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL3<1:0>:** Filter 3 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL3<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN2:** Filter 2 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL2<1:0>:** Filter 2 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL2<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 34-6: DEVCFG3/ADEVCFG3: DEVICE CONFIGURATION WORD 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	R/P	R/P	R/P	R/P	r-1	R/P	R/P
	—	FUSBIDIO	IOL1WAY	PMDL1WAY	PGL1WAY	—	FETHIO	FMIIEN
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** Write as '1'

bit 30 **FUSBIDIO:** USB USBID Selection bit
1 = USBID pin is controlled by the USB module
0 = USBID pin is controlled by the port function

If USBMD is '1', USBID reverts to port control.

bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 28 **PMDL1WAY:** Peripheral Module Disable Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 27 **PGL1WAY:** Permission Group Lock One Way Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 26 **Reserved:** Write as '1'

bit 25 **FETHIO:** Ethernet I/O Pin Selection Configuration bit
1 = Default Ethernet I/O pins
0 = Alternate Ethernet I/O pins

This bit is ignored for devices that do not have an alternate Ethernet pin selection.

bit 24 **FMIIEN:** Ethernet MII Enable Configuration bit
1 = MII is enabled
0 = RMII is enabled

bit 23-16 **Reserved:** Write as '1'

bit 15-0 **USERID<15:0>:** This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG

REGISTER 34-9: CFGEBIC: EXTERNAL BUS INTERFACE CONTROL PIN CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0
	EBI RDYINV3	EBI RDYINV2	EBI RDYIN1	—	EBI RDYEN3	EBI RDYEN2	EBI RDYEN1	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	EBIRDYLVL	EBIRPEN
15:8	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	—	EBIWEEN	EBIOEEN	—	—	EBIBSEN1	EBIBSEN0
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	EBICSEN3	EBICSEN2	EBICSEN1	EBICSEN0	—	—	EBIDEN1	EBIDEN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **EBIRDYINV3:** EBIRDY3 Inversion Control bit
1 = Invert EBIRDY3 pin before use
0 = Do not invert EBIRDY3 pin before use

bit 30 **EBIRDYINV2:** EBIRDY2 Inversion Control bit
1 = Invert EBIRDY2 pin before use
0 = Do not invert EBIRDY2 pin before use

bit 29 **EBIRDYINV1:** EBIRDY1 Inversion Control bit
1 = Invert EBIRDY1 pin before use
0 = Do not invert EBIRDY1 pin before use

bit 28 **Unimplemented:** Read as '0'

bit 27 **EBIRDYEN3:** EBIRDY3 Pin Enable bit
1 = EBIRDY3 pin is enabled for use by the EBI module
0 = EBIRDY3 pin is available for general use

bit 26 **EBIRDYEN2:** EBIRDY2 Pin Enable bit
1 = EBIRDY2 pin is enabled for use by the EBI module
0 = EBIRDY2 pin is available for general use

bit 25 **EBIRDYEN1:** EBIRDY1 Pin Enable bit
1 = EBIRDY1 pin is enabled for use by the EBI module
0 = EBIRDY1 pin is available for general use

bit 24-18 **Unimplemented:** Read as '0'

bit 17 **EBIRDYLVL:** EBIRDYx Pin Sensitivity Control bit
1 = Use level detect for EBIRDYx pins
0 = Use edge detect for EBIRDYx pins

bit 16 **EBIRPEN:** $\overline{\text{EBIRP}}$ Pin Sensitivity Control bit
1 = $\overline{\text{EBIRP}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIRP}}$ pin is available for general use

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **EBIWEEN:** $\overline{\text{EBIWE}}$ Pin Enable bit
1 = $\overline{\text{EBIWE}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIWE}}$ pin is available for general use

Note: When EBIMD = 1, the bits in this register are ignored and the pins are available for general use.

TABLE 37-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions(1)**
DO20a	VOH1	**Output High Voltage** I/O Pins: 4x Source Driver Pins - RA3, RA9, RA10, RA14, RA15 RB0-RB2, RB4, RB6-RB7, RB11, RB13 RC12-RC15 RD0, RD6-RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8 RG15 RH0, RH1, RH4-RH6, RH8-RH13 RJ0-RJ2, RJ8, RJ9, RJ11	1.5	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0	—	—	V	IOH ≥ -12 mA, VDD = 3.3V
			3.0	—	—	V	IOH ≥ -7 mA, VDD = 3.3V
		Output High Voltage I/O Pins: 8x Source Driver Pins - RA0-RA2, RA4, RA5 RB3, RB5, RB8-RB10, RB12, RB14, RB15 RC1-RC4 RD1-RD5, RD9, RD10, RD12, RD13, RD15 RE4-RE7 RF0, RF4, RF5, RF12, RF13 RG0, RG1, RG6-RG9 RH2, RH3, RH7, RH14, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	1.5	—	—	V	IOH ≥ -22 mA, VDD = 3.3V
			2.0	—	—	V	IOH ≥ -18 mA, VDD = 3.3V
			3.0	—	—	V	IOH ≥ -10 mA, VDD = 3.3V
		Output High Voltage I/O Pins: 12x Source Driver Pins - RA6, RA7 RE0-RE3 RF1 RG12-RG14	1.5	—	—	V	IOH ≥ -32 mA, VDD = 3.3V
			2.0	—	—	V	IOH ≥ -25 mA, VDD = 3.3V
			3.0	—	—	V	IOH ≥ -14 mA, VDD = 3.3V

Note 1: Parameters are characterized, but not tested.

TABLE 37-33: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	88	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 4)**	2.5	—	12	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	10	—	—	ns	—
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	12.5	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 20 ns.

4: Assumes 30 pF load on all SPIx pins.

FIGURE 40-5: VOH – 12x DRIVER PINS

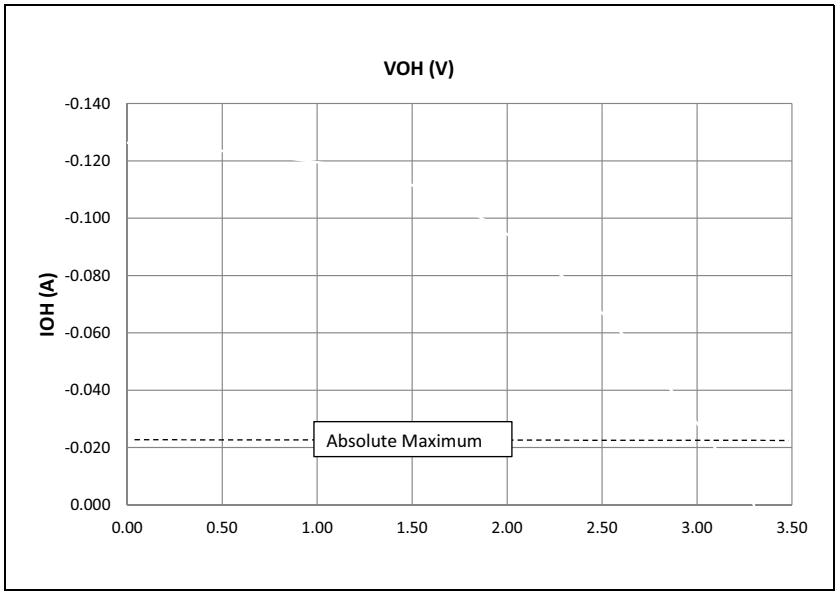


FIGURE 40-6: VOL – 12x DRIVER PINS

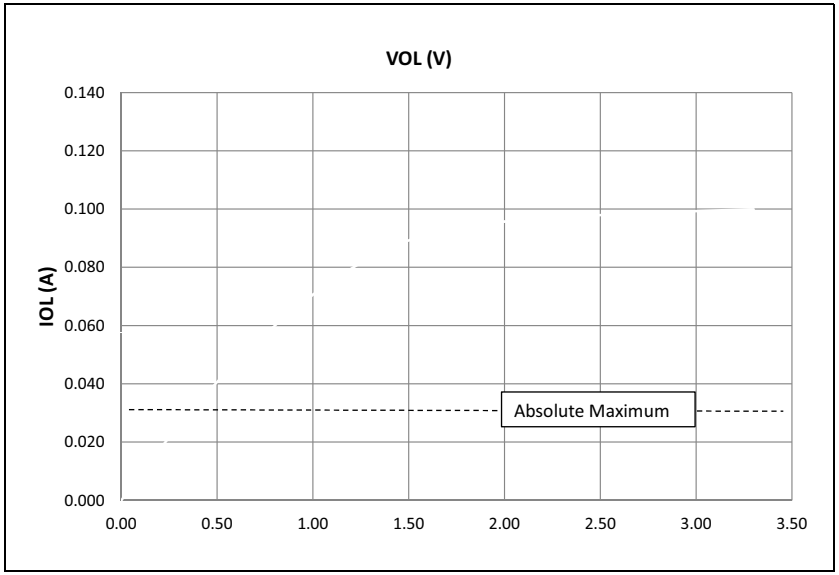


FIGURE 40-7: TYPICAL TEMPERATURE SENSOR VOLTAGE

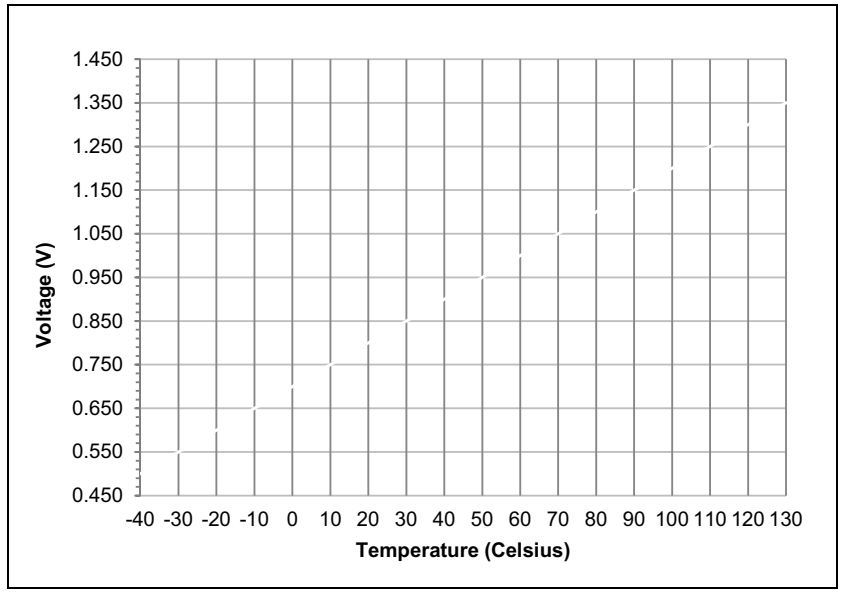


TABLE A-10: PERIPHERAL DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Ethernet	
	On PIC32MZ EF devices, the input clock divider for the Ethernet module has expanded options to accommodate the faster peripheral bus clock.
CLKSEL<3:0> (EMAC1MCFG<5:2>) 1000 = SYSCLK divided by 40 0111 = SYSCLK divided by 28 0110 = SYSCLK divided by 20 0101 = SYSCLK divided by 14 0100 = SYSCLK divided by 10 0011 = SYSCLK divided by 8 0010 = SYSCLK divided by 6 000x = SYSCLK divided by 4	CLKSEL<3:0> (EMAC1MCFG<5:2>) **1010 = PBCLK5 divided by 50** **1001 = PBCLK5 divided by 48** 1000 = PBCLK5 divided by 40 0111 = PBCLK5 divided by 28 0110 = PBCLK5 divided by 20 0101 = PBCLK5 divided by 14 0100 = PBCLK5 divided by 10 0011 = PBCLK5 divided by 8 0010 = PBCLK5 divided by 6 000x = PBCLK5 divided by 4
Comparator/Comparator Voltage Reference	
On PIC32MX devices, it was possible to select the VREF+ pin as the output to the CVREFOUT pin. VREFSEL (CVRCON<10>) 1 = CVREF = VREF+ 0 = CVREF is generated by the resistor network	On PIC32MZ EF devices, the CVREFOUT pin must come from the resistor network. This bit is not available.
On PIC32MX devices, the internal voltage reference (IVREF) could be chosen by the BGSEL<1:0> bits. BGSEL<1:0> (CVRCON<9:8>) 11 = IVREF = VREF+ 10 = Reserved 01 = IVREF = 0.6V (nominal, default) 00 = IVREF = 1.2V (nominal)	On PIC32MZ EF devices, IVREF is fixed and cannot be changed. These bits are not available.
Change Notification	
On PIC32MX devices, Change Notification is controlled by the **CNCON, CNEN, and CNPUE** registers.	On PIC32MZ EF devices, Change Notification functionality has been relocated into each I/O port and is controlled by the **CNPUx, CNPDx, CNCONx, CNENx, and CNSTATx** registers.
System Bus	
On PIC32MX devices, the System Bus registers can be used to configure RAM memory for data and program memory partitions, cacheability of Flash memory, and RAM Wait states. These registers are: **BMXCON, BMXDKPBA, BMXDUDBA, BMXDUPBA, BMXPUPBA, BMXDRMSZ, BMXPFMSZ, and BMXBOOTSZ.**	On PIC32MZ EF devices, a new System Bus is utilized that supports using RAM memory for program or data without the need for special configuration. Therefore, no special registers are associated with the System Bus to configure these features.
On PIC32MX devices, various arbitration modes are used as initiators on the System Bus. These modes can be selected by the **BMXARB<2:0> (BMXCON<2:0>)** bits.	On PIC32MZ EF devices, a new arbitration scheme has been implemented on the System Bus. All initiators use the Least Recently Serviced (LRS) scheme, with the exception of the DMA, CPU, and the Flash Controller. The Flash Controller always has High priority over LRS initiators. The DMA and CPU (when servicing an interrupt) can be selected to have LRS or High priority using the **DMAPRI (CFGCON<25>)** and **CPUPRI (CFGCON<24>)** bits.

Revision C (March 2016)

In this revision, the Preliminary status was removed from the document footer.

The revision also includes the following major changes, which are referenced by their respective chapter in Table C-2. In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE C-2: MAJOR SECTION UPDATES

Section Name	Update Description
2.0 "Guidelines for Getting Started with 32-bit Microcontrollers"	**2.9.1.3 "EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations"** and Figure 2-5 were updated.
4.0 "Memory Organization"	The names of the Boot Flash Words were updated from BFxSEQ0 to BFxSEQ3 (see **4.1.1 "Boot Flash Sequence and Configuration Spaces"**). The ABFxSEQx registers were removed from the Boot Flash Sequence and Configuration tables (see Table 4-2 and Table 4-3).
7.0 "CPU Exceptions and Interrupt Controller"	The Cache Error exception type was removed from the MIPS32 M-Class Microprocessor Core Exception Types (see Table 7-1).
8.0 "Oscillator Configuration"	The PLLODIV<2:0> bit value settings were updated in the SPLLCON register (see Register 8-3).
12.0 "I/O Ports"	The SIDL bit was removed from the CNCONx registers (see Table 12-4 through Table 12-21 and Register 12-3).
20.0 "Serial Quad Interface (SQI)"	The following bits were removed from the SQI1XCON1 register (see Table 20-1 and Register 20-1): DDRDATA, DDRDUMMY, DDRMODE, DDRADDR, and DDRCMD. The DDRMODE bit was removed from the SQI1CON register (see Table 20-1 and Register 20-4).
28.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"	A note was added to the SELRES<1:0> bits in the ADCCON1 and ADCxTIME registers (see Register 28-1 and Register 28-27). The ADCID<2:0 bit values were updated in the ADCFSTAT register (see Register 28-22).
34.0 "Special Features"	The bit value definitions for the POSCGAIN<1:0> and SOSCGAIN<1:0> bits were updated (see Register 34-3). The Device ADC Calibration Word (DEVADCx) register was added (see Table 34-5 and Register 34-13).