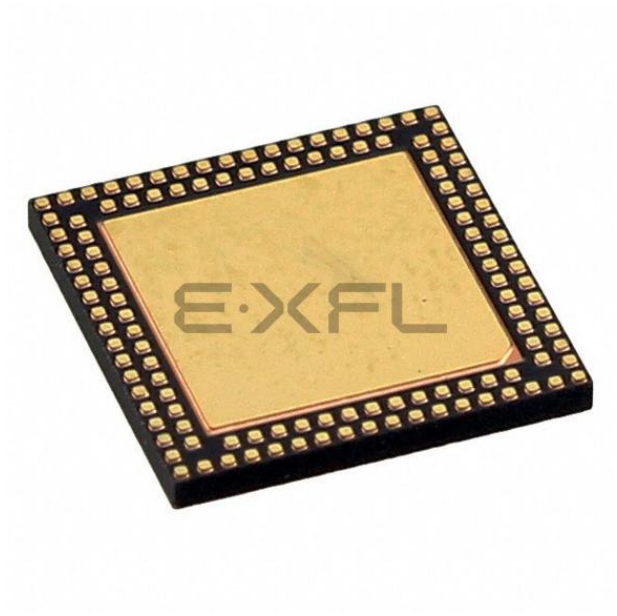
Microchip Technology - PIC32MZ0512EFE124T-I/TL Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	97
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512efe124t-i-tl

REGISTER 3-2: CONFIG1: CONFIGURATION REGISTER 1; CP0 REGISTER 16, SELECT 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	R-0	R-0	R-1	R-1	R-1	R-1	R-0
		MMU Size<5:0>						IS<2>
23:16	R-1	R-0	R-0	R-1	R-1	R-0	R-1	R-1
	IS<1:0>		IL<2:0>			IA<2:0>		
15:8	R-0	R-0	R-0	R-0	R-1	R-1	R-0	R-1
	DS<2:0>			DL<2:0>			DA<2:1>	
7:0	R-1	U-0	U-0	R-1	R-1	R-0	R-1	R-1
	DA<0>			PC	WR	CA	EP	FP

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 31 Reserved: This bit is hardwired to a 1 to indicate the presence of the Config2 register.

bit 30-25 MMU Size<5:0>: Contains the number of TLB entries minus 1
001111 = 16 TLB entries

bit 24-22 IS<2:0>: Instruction Cache Sets bits
010 = Contains 256 instruction cache sets per way

bit 21-19 IL<2:0>: Instruction-Cache Line bits
011 = Contains instruction cache line size of 16 bytes

bit 18-16 IA<2:0: Instruction-Cache Associativity bits
011 = Contains 4-way instruction cache associativity

bit 15-13 DS<2:0>: Data-Cache Sets bits
000 = Contains 64 data cache sets per way

bit 12-10 DL<2:0>: Data-Cache Line bits
011 = Contains data cache line size of 16 bytes

bit 9-7 DA<2:0>: Data-Cache Associativity bits
011 = Contains the 4-way set associativity for the data cache

bit 6-5 Unimplemented: Read as 0

bit 4 PC: Performance Counter bit
1 = The processor core contains Performance Counters

bit 3 WR: Watch Register Presence bit
1 = No Watch registers are present

bit 2 CA: Code Compression Implemented bit
0 = No MIPS16e^{fi} present

bit 1 EP: EJTAG Present bit
1 = Core implements EJTAG

bit 0 FP: Floating Point Unit bit
1 = Floating Point Unit is present

REGISTER 3-4: CONFIG5: CONFIGURATION REGISTER 5; CP0 REGISTER 16, SELECT 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-1
								NF

Legend:	r = Reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 31-1 Unimplemented: Read as 0

bit 0 NF: Nested Fault bit
1 = Nested Fault feature is implemented

REGISTER 3-5: CONFIG7: CONFIGURATION REGISTER 7; CP0 REGISTER 16, SELECT 7

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	WII							
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 31 WII: Wait IE Ignore bit
1 = Indicates that this processor will allow an interrupt to unblock a WAIT instruction

bit 30-0 Unimplemented: Read as 0

REGISTER 3-10: FCSR: FLOATING POINT CONTRO L AND STATUS REGISTER; CP1 REGISTER 31

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	FCC<7:1>							FS
23:16	R/W-x	R/W-x	R/W-x	R-0	R-1	R-1	R/W-x	R/W-x
	FCC<0>	FO	FN	MAC2008	ABS2008	NAN2008	CAUSE<5:4>	
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CAUSE<3:0>				ENABLES<4:1>			
					V	Z	O	U
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	ENABLES<0>	FLAGS<4:0>					RM<1:0>	
	I	V	Z	O	U	I		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 31-25 FCC<7:1>: Floating Point Condition Code bits
These bits record the results of floating point compares and are tested for floating point conditional branches and conditional moves.

bit 24 FS: Flush to Zero control bit
1 = Denormal input operands are flushed to zero. Tiny results are flushed to either zero or the applied format's smallest normalized number (MinNorm) depending on the rounding mode settings.
0 = Denormal input operands result in an Unimplemented Operation exception.

bit 23 FCC<0>: Floating Point Condition Code bits
These bits record the results of floating point compares and are tested for floating point conditional branches and conditional moves.

bit 22 FO: Flush Override Control bit
1 = The intermediate result is kept in an internal format, which can be perceived as having the usual mantissa precision but with unlimited exponent precision and without forcing to a specific value or taking an exception.
0 = Handling of Tiny Result values depends on setting of the FS bit.

bit 21 FN: Flush to Nearest Control bit
1 = Final result is rounded to either zero or 2E_min (MinNorm), whichever is closest when in Round to Nearest (RN) rounding mode. For other rounding modes, a final result is given as if FS was set to 1.
0 = Handling of Tiny Result values depends on setting of the FS bit.

bit 20 MAC2008: Fused Multiply Add mode control bit
0 = Unfused multiply-add. Intermediary multiplication results are rounded to the destination format.

bit 19 ABS2008: Absolute value format control bit
1 = ABS.fmt and NEG.fmt instructions compliant with IEEE Standard 754-2008. The ABS and NEG functions accept QNAN inputs without trapping.

bit 18 NAN2008: NaN Encoding control bit
1 = Quiet and signaling NaN encodings recommended by the IEEE Standard 754-2008. A quiet NaN is encoded with the first bit of the fraction being 1 and a signaling NaN is encoded with the first bit of the fraction being 0.

bit 17-12 CAUSE<5:0>: FPU Exception Cause bits
These bits indicated the exception conditions that arise during execution of an FPU arithmetic instruction.

bit 17 E: Unimplemented Operation bit

TABLE 4-16: SYSTEM BUS TARGET 8 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A020	SBT8ELOG1	31:16	MULTI				CODE<3:0>												0000
		15:0	INITID<7:0>								REGION<3:0>					CMD<2:0>			0000
A024	SBT8ELOG2	31:16																	0000
		15:0															GROUP<1:0>		0000
A028	SBT8ECON	31:16								ERRP									0000
		15:0																	0000
A030	SBT8ECLRS	31:16																	0000
		15:0																CLEAR	0000
A038	SBT8ECLRM	31:16																	0000
		15:0																CLEAR	0000
A040	SBT8REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI		SIZE<4:0>								xxxx
A050	SBT8RD0	31:16																	xxxx
		15:0													GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A058	SBT8WR0	31:16																	xxxx
		15:0													GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A060	SBT8REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI		SIZE<4:0>								xxxx
A070	SBT8RD1	31:16																	xxxx
		15:0													GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A078	SBT8WR1	31:16																	xxxx
		15:0													GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; = unimplemented, read as 0. Reset values are shown in hexadecimal.
Note: For reset values listed as xxxx, please refer to Table 4-6 for the actual reset values.

REGISTER 5-1: NVMCON: FLASH PROGRAM MING CONTROL REGISTER (CONTINUED)

bit 6 BFSWAP: Boot Flash Bank Alias Swap Control bit

This bit is only writable when WREN = 0 and the unlock sequence has been performed.

1 = Boot Flash Bank 2 is mapped to the lower boot alias and boot Flash Bank 1 is mapped to the upper boot alias

0 = Boot Flash Bank 1 is mapped to the lower boot alias and boot Flash Bank 2 is mapped to the upper boot alias

bit 5-4 Unimplemented: Read as 0

bit 3-0 NVMOP<3:0>: NVM Operation bits

These bits are only writable when WREN = 0.

1111 = Reserved

1000 = Reserved

0111 = Program erase operation: erase all of program Flash memory (all pages must be unprotected, PWP<23:0> = 0x000000)

0110 = Upper program Flash memory erase operation: erases only the upper mapped region of program Flash (all pages in that region must be unprotected)

0101 = Lower program Flash memory erase operation: erases only the lower mapped region of program Flash (all pages in that region must be unprotected)

0100 = Page erase operation: erases page selected by NVMADDR, if it is not write-protected

0011 = Row program operation: programs row selected by NVMADDR, if it is not write-protected

0010 = Quad Word (128-bit) program operation: programs the 128-bit Flash word selected by NVMADDR, if it is not write-protected

0001 = Word program operation: programs word selected by NVMADDR, if it is not write-protected(2)

0000 = No operation

Note 1: These bits are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

2: This operation results in a no operation (NOP) when the Dynamic Flash ECC Configuration bits = 00 (FECCCON<1:0> (DVCFG0<9:8>)), which enables ECC at all times. For all other FECCCON<1:0> bit settings, this command will execute, but will not write the ECC bits for the word and can cause DED errors if dynamic Flash ECC is enabled (FECCCON<1:0> = 01). Refer to Section 52. Flash Program Memory with Support for Live Update (DS60001193) for information regarding ECC and Flash programming.

7.2 Interrupts

The PIC32MZ EF family uses variable offsets for vector spacing. This allows the interrupt vector spacing to be configured according to application needs. A unique interrupt vector offset can be set for each vector using its associated OFFx register.

For details on the Variable Offset feature, refer to 8.5.2 Variable Offset in Section 8. Interrupt Controller (DS60001108) of the *"PIC32 Family Reference Manual"*.

Table 7-2 provides the Interrupt IRQ, vector and bit location information.

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION

Interrupt Source (1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Highest Natural Order Priority								
Core Timer Interrupt	_CORE_TIMER_VECTOR	0	OFF000<17:1>	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
Core Software Interrupt 0	_CORE_SOFTWARE_0_VECTOR	1	OFF001<17:1>	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
Core Software Interrupt 1	_CORE_SOFTWARE_1_VECTOR	2	OFF002<17:1>	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
External Interrupt 0	_EXTERNAL_0_VECTOR	3	OFF003<17:1>	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
Timer1	_TIMER_1_VECTOR	4	OFF004<17:1>	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
Input Capture 1 Error	_INPUT_CAPTURE_1_ERROR_VECTOR	5	OFF005<17:1>	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes
Input Capture 1	_INPUT_CAPTURE_1_VECTOR	6	OFF006<17:1>	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>	Yes
Output Compare 1	_OUTPUT_COMPARE_1_VECTOR	7	OFF007<17:1>	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>	No
External Interrupt 1	_EXTERNAL_1_VECTOR	8	OFF008<17:1>	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>	No
Timer2	_TIMER_2_VECTOR	9	OFF009<17:1>	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>	No
Input Capture 2 Error	_INPUT_CAPTURE_2_ERROR_VECTOR	10	OFF010<17:1>	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>	Yes
Input Capture 2	_INPUT_CAPTURE_2_VECTOR	11	OFF011<17:1>	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>	Yes
Output Compare 2	_OUTPUT_COMPARE_2_VECTOR	12	OFF012<17:1>	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>	No
External Interrupt 2	_EXTERNAL_2_VECTOR	13	OFF013<17:1>	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>	No
Timer3	_TIMER_3_VECTOR	14	OFF014<17:1>	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>	No
Input Capture 3 Error	_INPUT_CAPTURE_3_ERROR_VECTOR	15	OFF015<17:1>	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>	Yes
Input Capture 3	_INPUT_CAPTURE_3_VECTOR	16	OFF016<17:1>	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>	Yes
Output Compare 3	_OUTPUT_COMPARE_3_VECTOR	17	OFF017<17:1>	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>	No
External Interrupt 3	_EXTERNAL_3_VECTOR	18	OFF018<17:1>	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>	No
Timer4	_TIMER_4_VECTOR	19	OFF019<17:1>	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>	No
Input Capture 4 Error	_INPUT_CAPTURE_4_ERROR_VECTOR	20	OFF020<17:1>	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>	Yes
Input Capture 4	_INPUT_CAPTURE_4_VECTOR	21	OFF021<17:1>	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: PIC32MZ EF Family Features for the list of available peripherals.
2: This interrupt source is not available on 64-pin devices.
3: This interrupt source is not available on 100-pin devices.
4: This interrupt source is not available on 124-pin devices.

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION (CONTINUED)

Interrupt Source (1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Output Compare 4	_OUTPUT_COMPARE_4_VECTOR	22	OFF022<17:1>	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>	No
External Interrupt 4	_EXTERNAL_4_VECTOR	23	OFF023<17:1>	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>	No
Timer5	_TIMER_5_VECTOR	24	OFF024<17:1>	IFS0<24>	IEC0<24>	IPC6<4:2>	IPC6<1:0>	No
Input Capture 5 Error	_INPUT_CAPTURE_5_ERROR_VECTOR	25	OFF025<17:1>	IFS0<25>	IEC0<25>	IPC6<12:10>	IPC6<9:8>	Yes
Input Capture 5	_INPUT_CAPTURE_5_VECTOR	26	OFF026<17:1>	IFS0<26>	IEC0<26>	IPC6<20:18>	IPC6<17:16>	Yes
Output Compare 5	_OUTPUT_COMPARE_5_VECTOR	27	OFF027<17:1>	IFS0<27>	IEC0<27>	IPC6<28:26>	IPC6<25:24>	No
Timer6	_TIMER_6_VECTOR	28	OFF028<17:1>	IFS0<28>	IEC0<28>	IPC7<4:2>	IPC7<1:0>	No
Input Capture 6 Error	_INPUT_CAPTURE_6_ERROR_VECTOR	29	OFF029<17:1>	IFS0<29>	IEC0<29>	IPC7<12:10>	IPC7<9:8>	Yes
Input Capture 6	_INPUT_CAPTURE_6_VECTOR	30	OFF030<17:1>	IFS0<30>	IEC0<30>	IPC7<20:18>	IPC7<17:16>	Yes
Output Compare 6	_OUTPUT_COMPARE_6_VECTOR	31	OFF031<17:1>	IFS0<31>	IEC0<31>	IPC7<28:26>	IPC7<25:24>	No
Timer7	_TIMER_7_VECTOR	32	OFF032<17:1>	IFS1<0>	IEC1<0>	IPC8<4:2>	IPC8<1:0>	No
Input Capture 7 Error	_INPUT_CAPTURE_7_ERROR_VECTOR	33	OFF033<17:1>	IFS1<1>	IEC1<1>	IPC8<12:10>	IPC8<9:8>	Yes
Input Capture 7	_INPUT_CAPTURE_7_VECTOR	34	OFF034<17:1>	IFS1<2>	IEC1<2>	IPC8<20:18>	IPC8<17:16>	Yes
Output Compare 7	_OUTPUT_COMPARE_7_VECTOR	35	OFF035<17:1>	IFS1<3>	IEC1<3>	IPC8<28:26>	IPC8<25:24>	No
Timer8	_TIMER_8_VECTOR	36	OFF036<17:1>	IFS1<4>	IEC1<4>	IPC9<4:2>	IPC9<1:0>	No
Input Capture 8 Error	_INPUT_CAPTURE_8_ERROR_VECTOR	37	OFF037<17:1>	IFS1<5>	IEC1<5>	IPC9<12:10>	IPC9<9:8>	Yes
Input Capture 8	_INPUT_CAPTURE_8_VECTOR	38	OFF038<17:1>	IFS1<6>	IEC1<6>	IPC9<20:18>	IPC9<17:16>	Yes
Output Compare 8	_OUTPUT_COMPARE_8_VECTOR	39	OFF039<17:1>	IFS1<7>	IEC1<7>	IPC9<28:26>	IPC9<25:24>	No
Timer9	_TIMER_9_VECTOR	40	OFF040<17:1>	IFS1<8>	IEC1<8>	IPC10<4:2>	IPC10<1:0>	No
Input Capture 9 Error	_INPUT_CAPTURE_9_ERROR_VECTOR	41	OFF041<17:1>	IFS1<9>	IEC1<9>	IPC10<12:10>	IPC10<9:8>	Yes
Input Capture 9	_INPUT_CAPTURE_9_VECTOR	42	OFF042<17:1>	IFS1<10>	IEC1<10>	IPC10<20:18>	IPC10<17:16>	Yes
Output Compare 9	_OUTPUT_COMPARE_9_VECTOR	43	OFF043<17:1>	IFS1<11>	IEC1<11>	IPC10<28:26>	IPC10<25:24>	No
ADC Global Interrupt	_ADC_VECTOR	44	OFF044<17:1>	IFS1<12>	IEC1<12>	IPC11<4:2>	IPC11<1:0>	Yes
ADC FIFO Data Ready Interrupt	_ADC_FIFO_VECTOR	45	OFF045<17:1>	IFS1<13>	IEC1<13>	IPC11<12:10>	IPC11<9:8>	Yes
ADC Digital Comparator 1	_ADC_DC1_VECTOR	46	OFF046<17:1>	IFS1<14>	IEC1<14>	IPC11<20:18>	IPC11<17:16>	Yes
ADC Digital Comparator 2	_ADC_DC2_VECTOR	47	OFF047<17:1>	IFS1<15>	IEC1<15>	IPC11<28:26>	IPC11<25:24>	Yes
ADC Digital Comparator 3	_ADC_DC3_VECTOR	48	OFF048<17:1>	IFS1<16>	IEC1<16>	IPC12<4:2>	IPC12<1:0>	Yes
ADC Digital Comparator 4	_ADC_DC4_VECTOR	49	OFF049<17:1>	IFS1<17>	IEC1<17>	IPC12<12:10>	IPC12<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: PIC32MZ EF Family Features for the list of available peripherals.
2: This interrupt source is not available on 64-pin devices.
3: This interrupt source is not available on 100-pin devices.
4: This interrupt source is not available on 124-pin devices.

REGISTER 7-8: OFFx: INTERRUPT VECTOR ADDRESS OFFSET REGISTER (x = 0-190)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
							VOFF<17:16>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VOFF<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	VOFF<7:1>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as 0

bit 17-1 VOFF<17:1>: Interrupt Vector x Address Offset bits

bit 0 Unimplemented: Read as 0

REGISTER 9-1: PRECON: PREFETCH MODULE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
						PFMSECEN		
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
			PREFEN<1:0>			PFMWS<2:0> (1)		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 31-27 Unimplemented: Read as 0

bit 26 PFMSECEN: Flash SEC Interrupt Enable bit
1 = Generate an interrupt when the PFMSEC bit (PRESTAT<26>) is set
0 = Do not generate an interrupt when the PFMSEC bit is set

bit 25-6 Unimplemented: Read as 0

bit 5-4 PREFEN<1:0>: Predictive Prefetch Enable bits
11 = Enable predictive prefetch for any address
10 = Enable predictive prefetch for CPU instructions and CPU data
01 = Enable predictive prefetch for CPU instructions only
00 = Disable predictive prefetch

bit 3 Unimplemented: Read as 0

bit 2-0 PFMWS<2:0>: PFM Access Time Defined in Terms of SYSCLK Wait States bits(1)
111 = Seven Wait states

010 = Two Wait states
001 = One Wait state
000 = Zero Wait states

Note 1: For the Wait states to SYSCLK relationship, refer to Table 37-13 in Section37.0 Electrical Characteristics .

REGISTER 11-8: USBIENCSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 1-7) (CONTINUED)

bit 15-11 MULT<4:0>: Multiplier Control bits

For Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints, multiplies TXMAXP by MULT+1 for the payload size.

For Bulk endpoints, MULT can be up to 32 and defines the number of USB packets of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. The data packet is required to be an exact multiple of the payload specified by TXMAXP.

For Isochronous/Interrupts endpoints operating in Hi-Speed mode, MULT may be either 2 or 3 and specifies the maximum number of such transactions that can take place in a single microframe.

bit 10-0 TXMAXP<10:0>: Maximum TX Payload per transaction Control bits

This field sets the maximum payload (in bytes) transmitted in a single transaction. The value is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-Speed and Hi-Speed operations.

TXMAXP must be set to an even number of bytes for proper interrupt generation in DMA Mode 1.

REGISTER 11-17: USBEOFRST: USB END-OF -FRAME/SOFT RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
							NRSTX	NRST
23:16	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R.W-0	R/W-1	R/W-0
	LSEOF<7:0>							
15:8	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R.W-1	R/W-1	R/W-1
	FSEOF<7:0>							
7:0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R.W-0	R/W-0	R/W-0
	HSEOF<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 31-26 Unimplemented: Read as 0

bit 25 NRSTX: Reset of XCLK Domain bit
1 = Reset the XCLK domain, which is clock recovered from the received data by the PHY
0 = Normal operation

bit 24 NRST: Reset of CLK Domain bit
1 = Reset the CLK domain, which is clock recovered from the peripheral bus
0 = Normal operation

bit 23-16 LSEOF<7:0>: Low-Speed EOF bits
These bits set the Low-Speed transaction in units of 1.067 µs (default setting is 121.6 µs) prior to the EOF to stop new transactions from beginning.

bit 15-8 FSEOF<7:0>: Full-Speed EOF bits
These bits set the Full-Speed transaction in units of 533.3 µs (default setting is 63.46 µs) prior to the EOF to stop new transactions from beginning.

bit 7-0 HSEOF<7:0>: Hi-Speed EOF bits
These bits set the Hi-Speed transaction in units of 133.3 µs (default setting is 17.07µs) prior to the EOF to stop new transactions from beginning.

TABLE 12-23: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1620	RPE8R(1)	31:16																	0000
		15:0													RPE8R<3:0>				0000
1624	RPE9R(1)	31:16																	0000
		15:0													RPE9R<3:0>				0000
1640	RPF0R	31:16																	0000
		15:0													RPF0R<3:0>				0000
1644	RPF1R	31:16																	0000
		15:0													RPF1R<3:0>				0000
1648	RPF2R(1)	31:16																	0000
		15:0													RPF2R<3:0>				0000
164C	RPF3R	31:16																	0000
		15:0													RPF3R<3:0>				0000
1650	RPF4R	31:16																	0000
		15:0													RPF4R<3:0>				0000
1654	RPF5R	31:16																	0000
		15:0													RPF5R<3:0>				0000
1660	RPF8R(1)	31:16																	0000
		15:0													RPF8R<3:0>				0000
1670	RPF12R(1)	31:16																	0000
		15:0													RPG12R<3:0>				0000
1674	RPF13R(1)	31:16																	0000
		15:0													RPG0R<3:0>				0000
1680	RPG0R(1)	31:16																	0000
		15:0													RPG1R<3:0>				0000
1684	RPG1R(1)	31:16																	0000
		15:0													RPG1R<3:0>				0000
1698	RPG6R	31:16																	0000
		15:0													RPG6R<3:0>				0000
169C	RPG7R	31:16																	0000
		15:0													RPG7R<3:0>				0000
16A0	RPG8R	31:16																	0000
		15:0													RPG8R<3:0>				0000
16A4	RPG9R	31:16																	0000
		15:0													RPG9R<3:0>				0000

Legend: x = unknown value on Reset; = unimplemented, read as 0 . Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

2: This register is not available on 64-pin and 100-pin devices.

REGISTER 28-11: ADCCSS2: ADC COMMON SCAN SELECT REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				CSS44	CSS43	CSS42 (2)	CSS41(2)	CSS40(2)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS39(2)	CSS38(2)	CSS37(2)	CSS36(2)	CSS35(2)	CSS34(1)	CSS33(1)	CSS32(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 31-13 Unimplemented: Read as 0

bit 12-0 CSS44:CSS32: Analog Common Scan Select bits
Analog inputs 44 to 32 are always Class 3, as there are only 32 triggers available.
1 = Select AN*x* for input scan
0 = Skip AN*x* for input scan

Note 1: This bit is not available on 64-pin devices.
2: This bit is not available on 64-pin and 100-pin devices.

REGISTER 28-18: ADCTRG2: AD C TRIGGER SOURCE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				TRGSRC7<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				TRGSRC6<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				TRGSRC5<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				TRGSRC4<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 31-29 Unimplemented: Read as 0

bit 28-24 TRGSRC7<4:0>: Trigger Source for Conversion of Analog Input AN7 Select bits
11111 = Reserved

01101 = Reserved
01100 = Comparator 2 (COUT)
01011 = Comparator 1 (COUT)
01010 = OCMP5
01001 = OCMP3
01000 = OCMP1
00111 = TMR5 match
00110 = TMR3 match
00101 = TMR1 match
00100 = INT0 External interrupt
00011 = STRIG
00010 = Global level software trigger (GLSWTRG)
00001 = Global software edge Trigger (GSWTRG)
00000 = No Trigger

For STRIG, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSS*x* registers.

bit 23-21 Unimplemented: Read as 0

bit 20-16 TRGSRC6<4:0>: Trigger Source for Conversion of Analog Input AN6 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 Unimplemented: Read as 0

bit 12-8 TRGSRC5<4:0>: Trigger Source for Conversion of Analog Input AN5 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 Unimplemented: Read as 0

bit 4-0 TRGSRC4<4:0>: Trigger Source for Conversion of Analog Input AN4 Select bits
See bits 28-24 for bit value definitions.

REGISTER 29-4: CiVEC: CAN INTERRUPT CODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
				FILHIT<4:0>				
7:0	U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
		ICODE<6:0> (1)						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 31-13 Unimplemented: Read as 0

bit 12-8 FILHIT<4:0>: Filter Hit Number bit
11111 = Filter 31
11110 = Filter 30

00001 = Filter 1
00000 = Filter 0

bit 7 Unimplemented: Read as 0

bit 6-0 ICODE<6:0>: Interrupt Flag Code bits(1)
1001000-1111111 = Reserved
1001000 = Invalid message received (IVRIF)
1000111 = CAN module mode change (MODIF)
1000110 = CAN timestamp timer (CTMRIF)
1000101 = Bus bandwidth error (SERRIF)
1000100 = Address error interrupt (SERRIF)
1000011 = Receive FIFO overflow interrupt (RBOVIF)
1000010 = Wake-up interrupt (WAKIF)
1000001 = Error Interrupt (CERRIF)
1000000 = No interrupt
0100000-0111111 = Reserved
0011111 = FIFO31 Interrupt (CiFSTAT<31> set)
0011110 = FIFO30 Interrupt (CiFSTAT<30> set)

0000001 = FIFO1 Interrupt (CiFSTAT<1> set)
0000000 = FIFO0 Interrupt (CiFSTAT<0> set)

Note 1: These bits are only updated for enabled interrupts.

REGISTER 29-10: CiFLTCON0: CAN FILTER CONTROL REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN3	MSEL3<1:0>		FSEL3<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN2	MSEL2<1:0>		FSEL2<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN1	MSEL1<1:0>		FSEL1<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN0	MSEL0<1:0>		FSEL0<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 31 FLTEN3: Filter 3 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 MSEL3<1:0>: Filter 3 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 FSEL3<4:0>: FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30

00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 FLTEN2: Filter 2 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 MSEL2<1:0>: Filter 2 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 FSEL2<4:0>: FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30

00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is 0 .

REGISTER 30-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HTEN	MPEN		NOTPM	PMMODE<3:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CRCERREN	CRCOKEN	RUNTERREN	RUNTEN	UCEN	NOTMEEN	MCEN	BCEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as 0

bit 15 HTEN: Enable Hash Table Filtering bit
1 = Enable Hash Table Filtering
0 = Disable Hash Table Filtering

bit 14 MPEN: Magic Packet Enable bit
1 = Enable Magic Packet Filtering
0 = Disable Magic Packet Filtering

bit 13 Unimplemented: Read as 0

bit 12 NOTPM: Pattern Match Inversion bit
1 = The Pattern Match Checksum must not match for a successful Pattern Match to occur
0 = The Pattern Match Checksum must match for a successful Pattern Match to occur
This bit determines whether Pattern Match Checksum must match in order for a successful Pattern Match to occur.

bit 11-8 PMMODE<3:0>: Pattern Match Mode bits
1001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Packet = Magic Packet)(1,3)
1000 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Hash Table Filter match)(1,1)
0111 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)(1)
0110 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)(1)
0101 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)(1)
0100 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)(1)
0011 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)(1)
0010 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)(1)
0001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches)(1)
0000 = Pattern Match is disabled; pattern match is always unsuccessful

Note 1: XOR = True when either one or the other conditions are true, but not both.
2: This Hash Table Filter match is active regardless of the value of the HTEN bit.
3: This Magic Packet Filter match is active regardless of the value of the MPEN bit.

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

NOTES:

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