Microchip Technology - PIC32MZ0512EFE144T-E/JWX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TFBGA
Supplier Device Package	144-TFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512efe144t-e-jwx

TABLE 1-10: I2C1 THROUGH I2C5 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Inter-Integrated Circuit 1							
SCL1	44	66	B37	95	I/O	ST	I2C1 Synchronous Serial Clock Input/Output
SDA1	43	67	A45	96	I/O	ST	I2C1 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 2							
SCL2	—	59	A41	85	I/O	ST	I2C2 Synchronous Serial Clock Input/Output
SDA2	—	60	B34	86	I/O	ST	I2C2 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 3							
SCL3	51	58	A39	80	I/O	ST	I2C3 Synchronous Serial Clock Input/Output
SDA3	50	57	B31	79	I/O	ST	I2C3 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 4							
SCL4	6	12	B7	16	I/O	ST	I2C4 Synchronous Serial Clock Input/Output
SDA4	5	11	A8	15	I/O	ST	I2C4 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 5							
SCL5	42	65	A44	91	I/O	ST	I2C5 Synchronous Serial Clock Input/Output
SDA5	41	64	B36	90	I/O	ST	I2C5 Synchronous Serial Data Input/Output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-11: COMPARATOR 1, COMPARATOR 2 AND CVREF PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Comparator Voltage Reference							
CVREF+	16	29	A20	40	I	Analog	Comparator Voltage Reference (High) Input
CVREF-	15	28	B15	39	I	Analog	Comparator Voltage Reference (Low) Input
CVREFOUT	23	34	B19	49	O	Analog	Comparator Voltage Reference Output
Comparator 1							
C1INA	11	20	B11	25	I	Analog	Comparator 1 Positive Input
C1INB	12	21	A13	26	I	Analog	Comparator 1 Selectable Negative Input
C1INC	5	11	A8	15	I	Analog	
C1IND	4	10	B6	14	I	Analog	
C1OUT	PPS	PPS	PPS	PPS	O	—	Comparator 1 Output
Comparator 2							
C2INA	13	22	A14	31	I	Analog	Comparator 2 Positive Input
C2INB	14	23	A16	34	I	Analog	Comparator 2 Selectable Negative Input
C2INC	10	16	B9	21	I	Analog	
C2IND	6	12	B7	16	I	Analog	
C2OUT	PPS	PPS	PPS	PPS	O	—	Comparator 2 Output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

REGISTER 3-2: CONFIG1: CONFIGURATION REGISTER 1; CP0 REGISTER 16, SELECT 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	R-0	R-0	R-1	R-1	R-1	R-1	R-0
	—	MMU Size<5:0>						IS<2>
23:16	R-1	R-0	R-0	R-1	R-1	R-0	R-1	R-1
	IS<1:0>		IL<2:0>			IA<2:0>		
15:8	R-0	R-0	R-0	R-0	R-1	R-1	R-0	R-1
	DS<2:0>			DL<2:0>			DA<2:1>	
7:0	R-1	U-0	U-0	R-1	R-1	R-0	R-1	R-1
	DA<0>	—	—	PC	WR	CA	EP	FP

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to a '1' to indicate the presence of the Config2 register.

bit 30-25 **MMU Size<5:0>:** Contains the number of TLB entries minus 1
001111 = 16 TLB entries

bit 24-22 **IS<2:0>:** Instruction Cache Sets bits
010 = Contains 256 instruction cache sets per way

bit 21-19 **IL<2:0>:** Instruction-Cache Line bits
011 = Contains instruction cache line size of 16 bytes

bit 18-16 **IA<2:0:** Instruction-Cache Associativity bits
011 = Contains 4-way instruction cache associativity

bit 15-13 **DS<2:0>:** Data-Cache Sets bits
000 = Contains 64 data cache sets per way

bit 12-10 **DL<2:0>:** Data-Cache Line bits
011 = Contains data cache line size of 16 bytes

bit 9-7 **DA<2:0>:** Data-Cache Associativity bits
011 = Contains the 4-way set associativity for the data cache

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **PC:** Performance Counter bit
1 = The processor core contains Performance Counters

bit 3 **WR:** Watch Register Presence bit
1 = No Watch registers are present

bit 2 **CA:** Code Compression Implemented bit
0 = No MIPS16e® present

bit 1 **EP:** EJTAG Present bit
1 = Core implements EJTAG

bit 0 **FP:** Floating Point Unit bit
1 = Floating Point Unit is present

REGISTER 3-4: CONFIG5: CONFIGURATION REGISTER 5; CP0 REGISTER 16, SELECT 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-1
	—	—	—	—	—	—	—	NF

Legend:	r = Reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **NF:** Nested Fault bit
1 = Nested Fault feature is implemented

REGISTER 3-5: CONFIG7: CONFIGURATION REGISTER 7; CP0 REGISTER 16, SELECT 7

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	WII	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **WII:** Wait IE Ignore bit
1 = Indicates that this processor will allow an interrupt to unblock a WAIT instruction

bit 30-0 **Unimplemented:** Read as '0'

REGISTER 3-10: FCSR: FLOATING POINT CONTROL AND STATUS REGISTER; CP1 REGISTER 31

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	FCC<7:1>							FS
23:16	R/W-x	R/W-x	R/W-x	R-0	R-1	R-1	R/W-x	R/W-x
	FCC<0>	FO	FN	MAC2008	ABS2008	NAN2008	CAUSE<5:4>	
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CAUSE<3:0>				ENABLES<4:1>			
					V	Z	O	U
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	ENABLES<0>	FLAGS<4:0>					RM<1:0>	
	I	V	Z	O	U	I		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-25 **FCC<7:1>:** Floating Point Condition Code bits
These bits record the results of floating point compares and are tested for floating point conditional branches and conditional moves.

bit 24 **FS:** Flush to Zero control bit
1 = Denormal input operands are flushed to zero. Tiny results are flushed to either zero or the applied format's smallest normalized number (MinNorm) depending on the rounding mode settings.
0 = Denormal input operands result in an Unimplemented Operation exception.

bit 23 **FCC<0>:** Floating Point Condition Code bits
These bits record the results of floating point compares and are tested for floating point conditional branches and conditional moves.

bit 22 **FO:** Flush Override Control bit
1 = The intermediate result is kept in an internal format, which can be perceived as having the usual mantissa precision but with unlimited exponent precision and without forcing to a specific value or taking an exception.
0 = Handling of Tiny Result values depends on setting of the FS bit.

bit 21 **FN:** Flush to Nearest Control bit
1 = Final result is rounded to either zero or 2E_min (MinNorm), whichever is closest when in Round to Nearest (RN) rounding mode. For other rounding modes, a final result is given as if FS was set to 1.
0 = Handling of Tiny Result values depends on setting of the FS bit.

bit 20 **MAC2008:** Fused Multiply Add mode control bit
0 = Unfused multiply-add. Intermediary multiplication results are rounded to the destination format.

bit 19 **ABS2008:** Absolute value format control bit
1 = ABS.fmt and NEG.fmt instructions compliant with IEEE Standard 754-2008. The ABS and NEG functions accept QNAN inputs without trapping.

bit 18 **NAN2008:** NaN Encoding control bit
1 = Quiet and signaling NaN encodings recommended by the IEEE Standard 754-2008. A quiet NaN is encoded with the first bit of the fraction being 1 and a signaling NaN is encoded with the first bit of the fraction being 0.

bit 17-12 **CAUSE<5:0>:** FPU Exception Cause bits
These bits indicated the exception conditions that arise during execution of an FPU arithmetic instruction.

bit 17 **E:** Unimplemented Operation bit

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
05FC	OFF047	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0600	OFF048	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0604	OFF049	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0608	OFF050	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
060C	OFF051	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0610	OFF052	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0614	OFF053	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0618	OFF054	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
061C	OFF055	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0620	OFF056	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0624	OFF057	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0628	OFF058	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
062C	OFF059	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0630	OFF060	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0634	OFF061	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

REGISTER 10-8: DCHxECON: DMA CHANNEL x EVENT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHAIRQ<7:0>(1)							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHSIRQ<7:0>(1)							
7:0	S-0	S-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—

Legend:	S = Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>:** Channel Transfer Abort IRQ bits(1)

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag
•
•
•
00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag
00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>:** Channel Transfer Start IRQ bits(1)

11111111 = Interrupt 255 will initiate a DMA transfer
•
•
•
00000001 = Interrupt 1 will initiate a DMA transfer
00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE:** DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a '1'
0 = This bit always reads '0'

bit 6 **CABORT:** DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a '1'
0 = This bit always reads '0'

bit 5 **PATEN:** Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match
0 = Pattern match is disabled

bit 4 **SIRQEN:** Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs
0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN:** Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs
0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

Note 1: See **Table 7-2: "Interrupt IRQ, Vector, and Bit Location"** for the list of available interrupt IRQ sources.

11.1 USB OTG Control Registers

TABLE 11-1: USB REGISTER MAP 1

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	USBCSR0	31:16	—	—	—	—	—	—	—	—	EP7TXIF	EP6TXIF	EP5TXIF	EP4TXIF	EP3TXIF	EP2TXIF	EP1TXIF	EP0IF	0000
		15:0	ISOUPD(1)	SOFT CONN(1)	HSEN	HSMODE	RESET	RESUME	SUSP MODE	SUSPEN	—	FUNC<6:0>(1)							2000
			—(2)	—(2)								—(2)	—(2)	—(2)	—(2)	—(2)	—(2)	—(2)	
3004	USBCSR1	31:16	—	—	—	—	—	—	—	—	EP7TXIE	EP6TXIE	EP5TXIE	EP4TXIE	EP3TXIE	EP2TXIE	EP1TXIE	EP0IE	00FF
		15:0	—	—	—	—	—	—	—	—	EP7RXIF	EP6RXIF	EP5RXIF	EP4RXIF	EP3RXIF	EP2RXIF	EP1RXIF	—	0000
3008	USBCSR2	31:16	VBUSERRIE	SESSRQIE	DISCONIE	CONNIE	SOFIE	RESETIE	RESUMEIE	SUSPIE	VBUSERRIF	SESSREQIF	DISCONIF	CONNIF	SOFIF	RESETIF	RESUMEIF	SUSPIF	0600
		15:0	—	—	—	—	—	—	—	—	EP7RXIE	EP6RXIE	EP5RXIE	EP4RXIE	EP3RXIE	EP2RXIE	EP1RXIE	—	00FE
300C	USBCSR3	31:16	FORCEHST	FIFOACC	FORCEFS	FORCEHS	PACKET	TESTK	TESTJ	NAK	—	—	—	—	ENDPOINT<3:0>				0000
		15:0	—	—	—	—	—	RFRMNUM<10:0>											0000
3010	USB IE0CSR0(3)	31:16	—	—	—	—	—(1)	—(1)	—(1)	FLSHFIFO	SVC SETEND(1)	SVCRPR(1)	SEND STALL(1)	SETUP END(1)	DATAEND(1)	SENT STALL(1)	TXPKT RDY	RXPKT RDY	0000
							DISPING(2)	DTWREN(2)	DATA TGGL(2)		NAK TMOUT(2)	STATPKT(2)	REQPKT(2)	ERROR(2)	SETUP PKT(2)	RXSTALL(2)			0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
3018	USB IE0CSR2(3)	31:16	—	—	—	NAKLIM<4:0>(2)					SPEED<1:0>(2)		—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	RXCNT<6:0>							0000
301C	USB IE0CSR3(3)	31:16	MPRXEN	MPTXEN	BIGEND	HBRXEN	HBTXEN	DYNFIFOS	SOFTCONE	UTMIDWID	—	—	—	—	—	—	—	—	xx00
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
3010	USB IENCSR0(4)	31:16	AUTOSET	ISO(1)	MODE	DMA REQEN	FRC DATTG	DMA REQMD	—(1)	—(1)	INCOMP TX(1)	CLRDT	SENT STALL(1)	SEND STALL(1)	FLUSH	UNDER RUN(1)	FIFONE	TXPKT RDY	0000
				—					DTWREN(2)	DATA TGGL(2)	NAK TMOUT(2)		RXSTALL(2)	SETUPPKT(2)		ERROR(2)			0000
		15:0	MULT<4:0>					TXMAXP<10:0>											0000
3014	USB IENCSR1(4)	31:16	AUTOCLR	ISO(1)	DMA REQEN	DISNYET(1)	DMA REQMD	—(1)	—(1)	INCOM PRX	CLRDT	SENTSTALL(1)	SENDSTALL(1)	FLUSH	DATAERR(1)	OVERRUN(1)	FIFOFULL	RXPKT RDY	0000
				AUTORQ(2)		PIDERR(2)		DATA TWEN(2)	DATA TGGL(2)			RXSTALL(2)	REQPKT(2)		DERR-NAKT(1)	ERROR(2)			0000
		15:0	MULT<4:0>					RXMAXP<10:0>											0000
3018	USB IENCSR2(4)	31:16	TXINTERV<7:0>(2)								SPEED<1:0>(2)		PROTOCOL<1:0>		TEP<3:0>				0000
		15:0	—	—	RXCNT<13:0>														0000
301C	USB IENCSR3(1,3)	31:16	RXFIFOSZ<3:0>				TXFIFOSZ<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	RXINTERV<7:0>								SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>				0000
3020	USB FIFO0	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3024	USB FIFO1	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3128	USB E2CSR2	31:16	Indexed by the same bits in USBIE2CSR2																0000
		15:0																	0000
312C	USB E2CSR3	31:16	Indexed by the same bits in USBIE2CSR3																0000
		15:0																	0000
3130	USB E3CSR0	31:16	Indexed by the same bits in USBIE3CSR0																0000
		15:0																	0000
3134	USB E3CSR1	31:16	Indexed by the same bits in USBIE3CSR1																0000
		15:0																	0000
3138	USB E3CSR2	31:16	Indexed by the same bits in USBIE3CSR2																0000
		15:0																	0000
313C	USB E3CSR3	31:16	Indexed by the same bits in USBIE3CSR3																0000
		15:0																	0000
3140	USB E4CSR0	31:16	Indexed by the same bits in USBIE4CSR0																0000
		15:0																	0000
3144	USB E4CSR1	31:16	Indexed by the same bits in USBIE4CSR1																0000
		15:0																	0000
3148	USB E4CSR2	31:16	Indexed by the same bits in USBIE4CSR2																0000
		15:0																	0000
314C	USB E4CSR3	31:16	Indexed by the same bits in USBIE4CSR3																0000
		15:0																	0000
3150	USB E5CSR0	31:16	Indexed by the same bits in USBIE5CSR0																0000
		15:0																	0000
3154	USB E5CSR1	31:16	Indexed by the same bits in USBIE5CSR1																0000
		15:0																	0000
3158	USB E5CSR2	31:16	Indexed by the same bits in USBIE5CSR2																0000
		15:0																	0000
315C	USB E5CSR3	31:16	Indexed by the same bits in USBIE5CSR3																0000
		15:0																	0000
3160	USB E6CSR0	31:16	Indexed by the same bits in USBIE6CSR0																0000
		15:0																	0000
3164	USB E6CSR1	31:16	Indexed by the same bits in USBIE6CSR1																0000
		15:0																	0000
3168	USB E6CSR2	31:16	Indexed by the same bits in USBIE6CSR2																0000
		15:0																	0000
316C	USB E6CSR3	31:16	Indexed by the same bits in USBIE6CSR3																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

REGISTER 11-3: USBCSR2: USB CONTROL STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0
	VBUSERRIE	SESSRQIE	DISCONIE	CONNIE	SOFIE	RESETIE	RESUMEIE	SUSPIE
23:16	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS
	VBUSERRIF	SESSRQIF	DISCONIF	CONNIF	SOFIF	RESETIF	RESUMEIF	SUSPIF
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	U-0
	EP7RXIE	EP6RXIE	EP5RXIE	EP4RXIE	EP3RXIE	EP2RXIE	EP1RXIE	—

Legend:	HS = Hardware Set		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **VBUSERRIE:** VBUS Error Interrupt Enable bit
1 = VBUS error interrupt is enabled
0 = VBUS error interrupt is disabled

bit 30 **SESSRQIE:** Session Request Interrupt Enable bit
1 = Session request interrupt is enabled
0 = Session request interrupt is disabled

bit 29 **DISCONIE:** Device Disconnect Interrupt Enable bit
1 = Device disconnect interrupt is enabled
0 = Device disconnect interrupt is disabled

bit 28 **CONNIE:** Device Connection Interrupt Enable bit
1 = Device connection interrupt is enabled
0 = Device connection interrupt is disabled

bit 27 **SOFIE:** Start of Frame Interrupt Enable bit
1 = Start of Frame event interrupt is enabled
0 = Start of Frame event interrupt is disabled

bit 26 **RESETIE:** Reset/Babble Interrupt Enable bit
1 = Interrupt when reset (*Device mode*) or Babble (*Host mode*) is enabled
0 = Reset/Babble interrupt is disabled

bit 25 **RESUMEIE:** Resume Interrupt Enable bit
1 = Resume signaling interrupt is enabled
0 = Resume signaling interrupt is disabled

bit 24 **SUSPIE:** Suspend Interrupt Enable bit
1 = Suspend signaling interrupt is enabled
0 = Suspend signaling interrupt is disabled

bit 23 **VBUSERRIF:** VBUS Error Interrupt bit
1 = VBUS has dropped below the VBUS valid threshold during a session
0 = No interrupt

bit 22 **SESSRQIF:** Session Request Interrupt bit
1 = Session request signaling has been detected
0 = No session request detected

bit 21 **DISCONIF:** Device Disconnect Interrupt bit
1 = In *Host mode*, indicates when a device disconnect is detected. In *Device mode*, indicates when a session ends.
0 = No device disconnect detected

bit 20 **CONNIF:** Device Connection Interrupt bit
1 = In *Host mode*, indicates when a device connection is detected
0 = No device connection detected

REGISTER 11-21: USBDMAxC: USB DMA CHANNEL 'x' CONTROL REGISTER ('x' = 1-8)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	DMABRSTM<1:0>		DMAERR
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-9 **DMABRSTM<1:0>:** DMA Burst Mode Selection bit

11 = Burst Mode 3: INCR16, INCR8, INCR4 or unspecified length
10 = Burst Mode 2: INCR8, INCR4 or unspecified length
01 = Burst Mode 1: INCR4 or unspecified length
00 = Burst Mode 0: Bursts of unspecified length

bit 8 **DMAERR:** Bus Error bit

1 = A bus error has been observed on the input
0 = The software writes this to clear the error

bit 7-4 **DMAEP<3:0>:** DMA Endpoint Assignment bits

These bits hold the endpoint that the DMA channel is assigned to. Valid values are 0-7.

bit 3 **DMAIE:** DMA Interrupt Enable bit

1 = Interrupt is enabled for this channel
0 = Interrupt is disabled for this channel

bit 2 **DMAMODE:** DMA Transfer Mode bit

1 = DMA Mode1 Transfers
0 = DMA Mode0 Transfers

bit 1 **DMADIR:** DMA Transfer Direction bit

1 = DMA Read (TX endpoint)
0 = DMA Write (RX endpoint)

bit 0 **DMAEN:** DMA Enable bit

1 = Enable the DMA transfer and start the transfer
0 = Disable the DMA transfer

REGISTER 11-30: USBCRCON: USB CLOCK/RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R/W-1, HS
	—	—	—	—	—	USBIF	USBRF	USBWKUP
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	r-1	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	USB IDOVEN	USB IDVAL
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PHYIDEN	VBUS MONEN	ASVAL MONEN	BSVAL MONEN	SEND MONEN	USBIE	USBRIE	USB WKUPEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **USBIF:** USB General Interrupt Flag bit
1 = An event on the USB Bus has occurred
0 = No interrupt from USB module or interrupts have not been enabled

bit 25 **USBRF:** USB Resume Flag bit
1 = Resume from Suspend state. Device wake-up activity can be started.
0 = No Resume activity detected during Suspend, or not in Suspend state

bit 24 **USBWK:** USB Activity Status bit
1 = Connect, disconnect, or other activity on USB detected since last cleared
0 = No activity detected on USB

Note: This bit should be cleared just prior to entering sleep, but it should be checked that no activity has already occurred on USB before actually entering sleep.

bit 23-14 **Unimplemented:** Read as '0'

bit 15 **Reserved:** Read as '1'

bit 14-10 **Unimplemented:** Read as '0'

bit 9 **USBIDOVEN:** USB ID Override Enable bit
1 = Enable use of USBIDVAL bit
0 = Disable use of USBIDVAL and instead use the PHY value

bit 8 **USBIDVAL:** USB ID Value bit
1 = ID override value is 1
0 = ID override value is 0

bit 7 **PHYIDEN:** PHY ID Monitoring Enable bit
1 = Enable monitoring of the ID bit from the USB PHY
0 = Disable monitoring of the ID bit from the USB PHY

bit 6 **VBUSMONEN:** VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in VBUS Valid range (between 4.4V and 4.75V)
0 = Disable monitoring for VBUS in VBUS Valid range

bit 5 **ASVALMONEN:** A-Device VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in Session Valid range for A-device (between 0.8V and 2.0V)
0 = Disable monitoring for VBUS in Session Valid range for A-device

bit 4 **BSVALMONEN:** B-Device VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in Session Valid range for B-device (between 0.8V and 4.0V)
0 = Disable monitoring for VBUS in Session Valid range for B-device

12.4.3 CONTROLLING PPS

PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

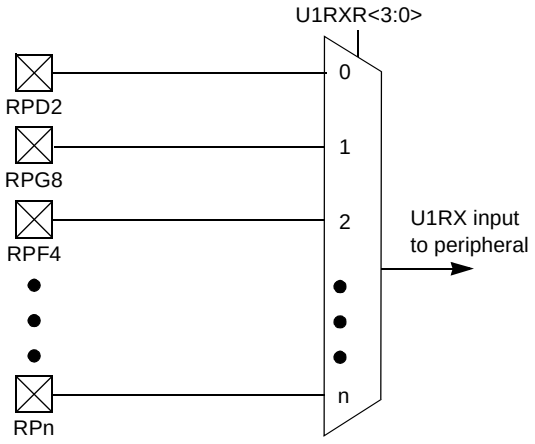
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

12.4.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [*pin name*]R registers, where [*pin name*] refers to the peripheral pins listed in Table 12-2, are used to configure peripheral input mapping (see Register 12-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 12-2.

For example, Figure 12-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 12-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

FIGURE 26-2: FORMAT OF BD_CTRL

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	DESC_EN	—	CRY_MODE<2:0>			—	—	—
23-16	—	SA_ FETCH_EN	—	—	LAST_BD	LIFM	PKT_ INT_EN	CBD_ INT_EN
15-8	BD_BUFLEN<15:8>							
7-0	BD_BUFLEN<7:0>							

bit 31 **DESC_EN**: Descriptor Enable
1 = The descriptor is owned by hardware. After processing the BD, hardware resets this bit to '0'.
0 = The descriptor is owned by software

bit 30 **Unimplemented:** Must be written as '0'

bit 29-27 **CRY_MODE<2:0>:** Crypto Mode
111 = Reserved
110 = Reserved
101 = Reserved
100 = Reserved
011 = CEK operation
010 = KEK operation
001 = Preboot authentication
000 = Normal operation

bit 22 **SA_FETCH_EN:** Fetch Security Association From External Memory
1 = Fetch SA from the SA pointer. This bit needs to be set to '1' for every new packet.
0 = Use current fetched SA or the internal SA

bit 21-20 **Unimplemented:** Must be written as '0'

bit 19 **LAST_BD:** Last Buffer Descriptors
1 = Last Buffer Descriptor in the chain
0 = More Buffer Descriptors in the chain
After the last BD, the CEBDADDR goes to the base address in CEBDPADDR.

bit 18 **LIFM:** Last In Frame
In case of Receive Packets (from H/W-> Host), this field is filled by the Hardware to indicate whether the packet goes across multiple buffer descriptors. In case of transmit packets (from Host -> H/W), this field indicates whether this BD is the last in the frame.

bit 17 **PKT_INT_EN:** Packet Interrupt Enable
Generate an interrupt after processing the current buffer descriptor, if it is the end of the packet.

bit 16 **CBD_INT_EN:** CBD Interrupt Enable
Generate an interrupt after processing the current buffer descriptor.

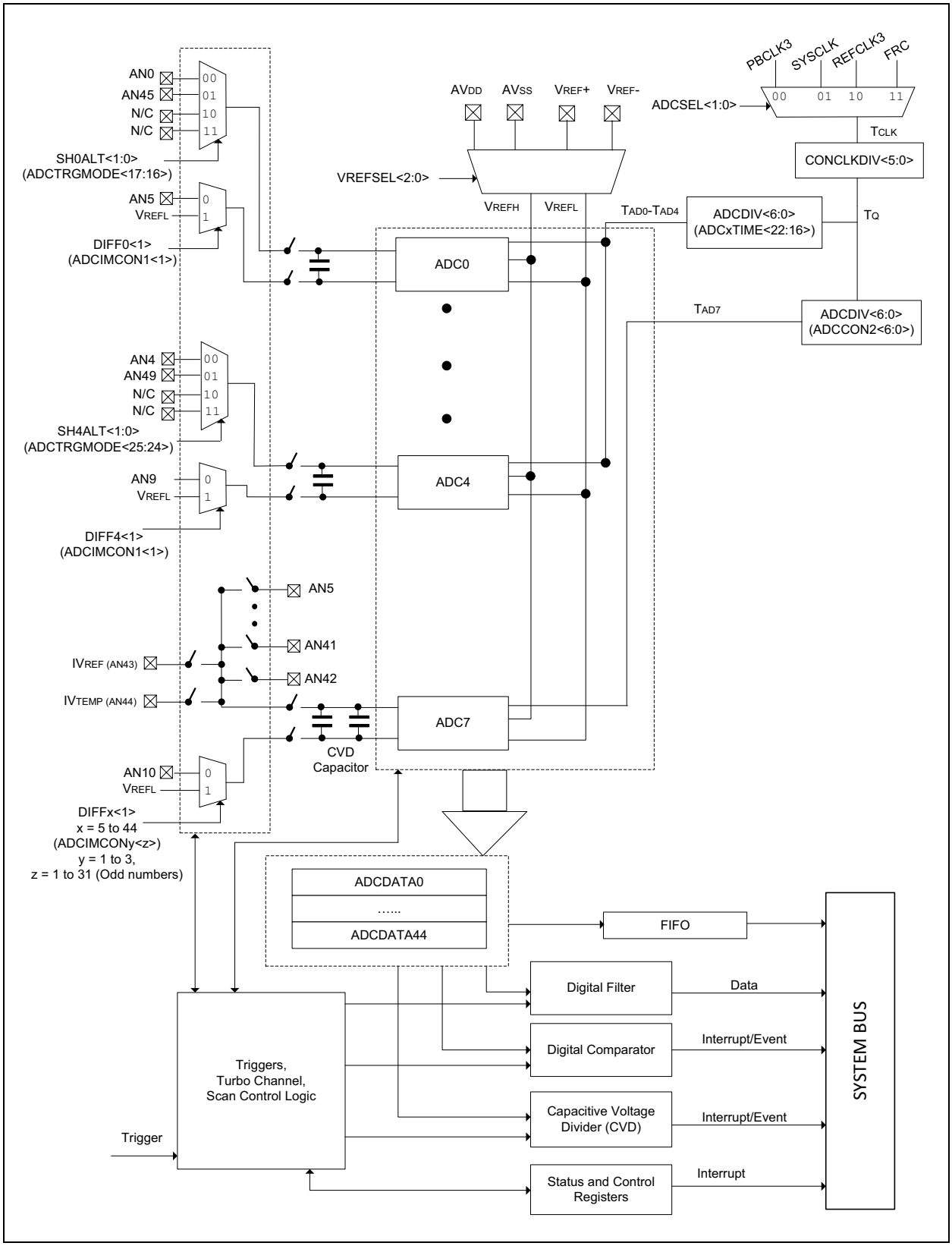
bit 15-0 **BD_BUFLEN<15:0>:** Buffer Descriptor Length
This field contains the length of the buffer and is updated with the actual length filled by the receiver.

FIGURE 26-3: FORMAT OF BD_SADDR

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	BD_SAADDR<31:24>							
23-16	BD_SAADDR<23:16>							
15-8	BD_SAADDR<15:8>							
7-0	BD_SAADDR<7:0>							

bit 31-0 **BD_SAADDR<31:0>:** Security Association IP Session Address
The sessions' SA pointer has the keys and IV values.

FIGURE 28-1: ADC BLOCK DIAGRAM



REGISTER 28-12: ADCDSTAT1: ADC DATA READY STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ARDY31(1)	ARDY30(1)	ARDY29(1)	ARDY28(1)	ARDY27(1)	ARDY26(1)	ARDY25(1)	ARDY24(1)
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ARDY23(1)	ARDY22(1)	ARDY21(1)	ARDY20(1)	ARDY19(1)	ARDY18	ARDY17	ARDY16
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ARDY15	ARDY14	ARDY13	ARDY12	ARDY11	ARDY10	ARDY9	ARDY8
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ARDY7	ARDY6	ARDY5	ARDY4	ARDY3	ARDY2	ARDY1	ARDY0

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **ARDY31:ARDY0:** Conversion Data Ready for Corresponding Analog Input Ready bits
1 = This bit is set when converted data is ready in the data register
0 = This bit is cleared when the associated data register is read

Note 1: This bit is not available on 64-pin devices.

REGISTER 28-13: ADCDSTAT2: ADC DATA READY STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	ARDY44	ARDY43	ARDY42(2)	ARDY41(2)	ARDY40(2)
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ARDY39(2)	ARDY38(2)	ARDY37(2)	ARDY36(2)	ARDY35(2)	ARDY34(1)	ARDY33(1)	ARDY32(1)

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-0 **ARDY44:ARDY32:** Conversion Data Ready for Corresponding Analog Input Ready bits
1 = This bit is set when converted data is ready in the data register
0 = This bit is cleared when the associated data register is read

Note 1: This bit is not available on 64-pin devices.
2: This bit is not available on 64 -pin and 100-pin devices.

REGISTER 28-22: ADCFSTAT: ADC FIFO STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FEN	—	—	ADC4EN	ADC3EN	ADC2EN	ADC1EN	ADC0EN
23:16	R/W-0	R-0, HS, HC	R-0, HS, HC	U-0	U-0	U-0	U-0	U-0
	FIEN	FRDY	FWROVERR	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FCNT<7:0>							
7:0	R-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	FSIGN	—	—	—	—	ADCID<2:0>		

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FEN:** FIFO Enable bit
1 = FIFO is enabled
0 = FIFO is disabled; no data is being saved into the FIFO

bit 30-29 **Unimplemented:** Read as '0'

bit 28-24 **ADC4EN:ADC0EN:** ADCx Enable bits ('x' = 0 through 4)
1 = Converted output data of ADCx is stored in the FIFO
0 = Converted output data of ADCx is not stored in the FIFO

Note: While using FIFO, the output data is additionally stored in the respective output data register (ADCDATAx).

bit 23 **FIEN:** FIFO Interrupt Enable bit
1 = FIFO interrupts are enabled; an interrupt is generated once the FRDY bit is set
0 = FIFO interrupts are disabled

bit 22 **FRDY:** FIFO Data Ready Interrupt Status bit
1 = FIFO has data to be read
0 = No data is available in the FIFO

Note: This bit is cleared when the FIFO output data in ADCFIFO has been read and there is no additional data ready in the FIFO (that is, the FIFO is empty).

bit 21 **FWROVERR:** FIFO Write Overflow Error Status bit
1 = A write overflow error in the FIFO has occurred (circular FIFO)
0 = A write overflow error in the FIFO has not occurred

Note: This bit is cleared after ADCFSTAT<23:16> are read by software.

bit 15-8 **FCNT<7:0>:** FIFO Data Entry Count Status bit
The value in these bits indicates the number of data entries in the FIFO.

bit 7 **FSIGN:** FIFO Sign Setting bit
This bit reflects the sign of data stored in the ADCFIFO register.

bit 6-3 **Unimplemented:** Read as '0'

bit 2-0 **ADCID<2:0>:** ADCx Identifier bits ('x' = 0 through 4)
These bits specify the ADC module whose data is stored in the FIFO.
111 = Reserved
110 = Reserved
101 = Reserved
100 = Converted data of ADC4 is stored in FIFO
•
•
•
000 = Converted data of ADC0 is stored in FIFO

REGISTER 30-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HTEN	MPEN	—	NOTPM	PMMODE<3:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CRCERREN	CRCOKEN	RUNTERREN	RUNTEN	UCEN	NOTMEEN	MCEN	BCEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **HTEN:** Enable Hash Table Filtering bit
1 = Enable Hash Table Filtering
0 = Disable Hash Table Filtering

bit 14 **MPEN:** Magic Packet™ Enable bit
1 = Enable Magic Packet Filtering
0 = Disable Magic Packet Filtering

bit 13 **Unimplemented:** Read as '0'

bit 12 **NOTPM:** Pattern Match Inversion bit
1 = The Pattern Match Checksum must not match for a successful Pattern Match to occur
0 = The Pattern Match Checksum must match for a successful Pattern Match to occur
This bit determines whether Pattern Match Checksum must match in order for a successful Pattern Match to occur.

bit 11-8 **PMMODE<3:0>:** Pattern Match Mode bits
1001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Packet = Magic Packet)**(1,3)**
1000 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Hash Table Filter match)**(1,1)**
0111 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)**(1)**
0110 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)**(1)**
0101 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)**(1)**
0100 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)**(1)**
0011 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)**(1)**
0010 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)**(1)**
0001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches)**(1)**
0000 = Pattern Match is disabled; pattern match is always unsuccessful

Note 1: XOR = True when either one or the other conditions are true, but not both.
2: This Hash Table Filter match is active regardless of the value of the HTEN bit.
3: This Magic Packet Filter match is active regardless of the value of the MPEN bit.

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

36.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

36.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

36.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

36.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

FIGURE 37-2: EXTERNAL CLOCK TIMING

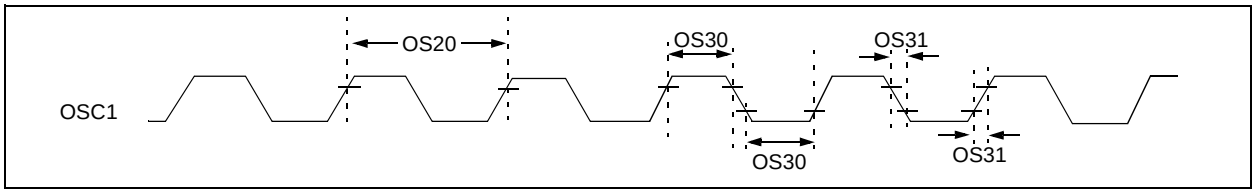


TABLE 37-17: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Minimum**	**Typical(1)**	**Maximum**	**Units**	**Conditions**
OS10	FOSC	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	64	MHz	EC **(Note 2,3)**
OS13		Oscillator Crystal Frequency	4	—	32	MHz	HS **(Note 2,3)**
OS15			32	32.768	100	kHz	SOSC **(Note 2)**
OS20	TOSC	TOSC = 1/FOSC	—	—	—	—	See parameter OS10 for FOSC value
OS30	TOSL, TOSH	External Clock In (OSC1) High or Low Time	0.375 x TOSC	—	—	ns	EC **(Note 2)**
OS31	TOSR, TOSF	External Clock In (OSC1) Rise or Fall Time	—	—	7.5	ns	EC **(Note 2)**
OS40	TOST	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, and SOSC Clock Oscillator modes)	—	1024	—	TOSC	**(Note 2)**
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	**(Note 2)**
OS42	GM	External Oscillator Transconductance	—	400	—	µA/V	VDD = 3.3V, TA = +25°C, HS **(Note 2)**

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are characterized but are not tested.

2: This parameter is characterized, but not tested in manufacturing.

3: See parameter OS50 for PLL input frequency limitations.

APPENDIX B: MIGRATING FROM PIC32MZ EC TO PIC32MZ EF

This appendix provides an overview of considerations for migrating from PIC32MZ EC devices to the PIC32MZ EF family of devices. The code developed for PIC32MZ EC devices can be ported to PIC32MZ EF devices after making the appropriate changes outlined in the following sections.

The PIC32MZ EF devices are similar to PIC32MZ EC devices, with many feature improvements and new capabilities.

B.1 Oscillator and PLL Configuration

A number of new features have been added to the oscillator and PLL to enhance their ability to work with crystals and to change frequencies.

Table B-1 summarizes the differences (indicated by **Bold** type) between the family differences for the oscillator.

TABLE B-1: OSCILLATOR DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
Primary Oscillator Crystal Power	
On PIC32MZ EC devices, the crystal HS POSC mode is only functional with crystals that have certain characteristics, such as very low ESR.	On PIC32MZ EF devices, some DEVCFG0 bits have been added to allow control over the strength of the oscillator and to add a kick start boost. POSCBOOST (DEVCFG0<21>) 1 = Boost the kick start of the oscillator 0 = Normal start of the oscillator POSCGAIN<1:0> (DEVCFG0<20:19>) 11 = 2x gain setting 10 = 1.5x gain setting 01 = 0.5x gain setting 00 = 1x gain setting Note that the default for POSCGAIN (2x gain setting) may overdrive crystals and shorten their life. It is the responsibility of the designer to ensure crystals are operated properly.
Secondary Oscillator Crystal Power	
On PIC32MZ EC devices, the Secondary Oscillator (SOSC) is not functional.	On PIC32MZ EF devices, the Secondary Oscillator is now functional, and provides similar strength and kick start boost features as the POSC. SOSCBOOST (DEVCFG0<18>) 1 = Boost the kick start of the oscillator 0 = Normal start of the oscillator SOSCGAIN<1:0> (DEVCFG0<17:16>) 11 = 2x gain setting 10 = 1.5x gain setting 01 = 0.5x gain setting 00 = 1x gain setting Note that the default for SOSCGAIN (2x gain setting) may overdrive crystals and shorten their life. It is the responsibility of the designer to ensure crystals are operated properly.
Clock Status Bits	
On PIC32MZ EC devices, the SOSCRDY bit (OSCCON<22>) indicates when the Secondary Oscillator is ready. There are no indications of other oscillator status.	A new register, CLKSTAT, has been added, which includes the SOSCRDY bit (CLKSTAT<4>). In addition, new status bits are available: • LPRCRDY (CLKSTAT<5>) • POSCRDY (CLKSTAT<2>) • DIVSPLLRDY (CLKSTAT<1>) • FRCRDY (CLKSTAT<0>)
Clock Switching	
On PIC32MZ EC devices, clock switches occur as soon as the switch command is issued. Also, the only clock sources that can be divided are the output of the PLL, and the FRC.	To reduce power spikes during clock switches, PIC32MZ EF devices add a clock slewing feature, so that clock switches can be controlled in their rate and size. The SLEWCON register controls this feature. The SLEWCON register also features a SYSCLK divider, so that all of the possible clock sources may be divided further as needed.