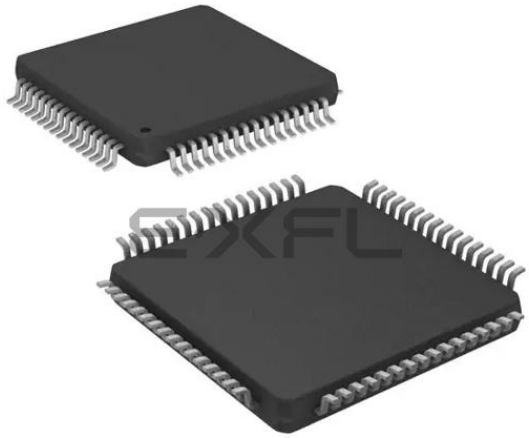
Microchip Technology - PIC32MZ0512EFF064T-I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	46
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512eff064t-i-pt

TABLE 1-22: JTAG, TRACE, AND PROGRAMMING/DEBUGGING PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
JTAG							
TCK	27	38	B21	56	I	ST	JTAG Test Clock Input Pin
TDI	28	39	A26	57	I	ST	JTAG Test Data Input Pin
TDO	24	40	B22	58	O	—	JTAG Test Data Output Pin
TMS	23	17	A11	22	I	ST	JTAG Test Mode Select Pin
Trace							
TRCLK	57	89	A61	129	O	—	Trace Clock
TRD0	58	97	B55	141	O	—	Trace Data bits 0-3
TRD1	61	96	A65	140	O	—	
TRD2	62	95	B54	139	O	—	
TRD3	63	90	B51	130	O	—	
Programming/Debugging							
PGED1	16	25	A18	36	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1
PGEC1	15	24	A17	35	I	ST	Clock input pin for Programming/Debugging Communication Channel 1
PGED2	18	27	A19	38	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2
PGEC2	17	26	B14	37	I	ST	Clock input pin for Programming/Debugging Communication Channel 2
$\overline{MCLR}$	9	15	A10	20	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER (CONTINUED)

bit 15-12 **PRI3SS<3:0>:** Interrupt with Priority Level 3 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 3 uses Shadow Set 0)
0111 = Interrupt with a priority level of 3 uses Shadow Set 7
0110 = Interrupt with a priority level of 3 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 3 uses Shadow Set 1
0000 = Interrupt with a priority level of 3 uses Shadow Set 0

bit 11-8 **PRI2SS<3:0>:** Interrupt with Priority Level 2 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 2 uses Shadow Set 0)
0111 = Interrupt with a priority level of 2 uses Shadow Set 7
0110 = Interrupt with a priority level of 2 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 2 uses Shadow Set 1
0000 = Interrupt with a priority level of 2 uses Shadow Set 0

bit 7-4 **PRI1SS<3:0>:** Interrupt with Priority Level 1 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 1 uses Shadow Set 0)
0111 = Interrupt with a priority level of 1 uses Shadow Set 7
0110 = Interrupt with a priority level of 1 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 1 uses Shadow Set 1
0000 = Interrupt with a priority level of 1 uses Shadow Set 0

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **SS0:** Single Vector Shadow Register Set bit
1 = Single vector is presented with a shadow set
0 = Single vector is not presented with a shadow set

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

10.1 DMA Control Registers

TABLE 10-1: DMA GLOBAL REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	DMACON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	SUSPEND	DMABUSY	—	—	—	—	—	—	—	—	—	—	—	0000
1010	DMASTAT	31:16	RDWR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	DMACH<2:0>			0000
1020	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

TABLE 10-2: DMA CRC REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1030	DCRCCON	31:16	—	—	BYTO<1:0>		WBO	—	—	BITO	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PLEN<4:0>					CRCEN	CRCAPP	CRCTYP	—	—	CRCCH<2:0>			0000
1040	DCRCDATA	31:16	DCRCDATA<31:0>																0000
		15:0																	0000
1050	DCRCXOR	31:16	DCRCXOR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RXDPB	RXFIFOSZ<3:0>			
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TXDPB	TXFIFOSZ<3:0>			
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	TXEDMA	RXEDMA
7:0	R-1	R-0	R-0	R-0	R-0	R-0	R/W-0, HC	R/W-0
	BDEV	FSDEV	LSDEV	VBUS<1:0>		HOSTMODE	HOSTREQ	SESSION

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **RXDPB:** RX Endpoint Double-packet Buffering Control bit
1 = Double-packet buffer is supported. This doubles the size set in RXFIFOSZ.
0 = Double-packet buffer is not supported

bit 27-24 **RXFIFOSZ<3:0>:** RX Endpoint FIFO Packet Size bits

The maximum packet size to allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)

1111 = Reserved
•
•
•
1010 = Reserved
1001 = 4096 bytes
1000 = 2048 bytes
0111 = 1024 bytes
0110 = 512 bytes
0101 = 256 bytes
0100 = 128 bytes
0011 = 64 bytes
0010 = 32 bytes
0001 = 16 bytes
0000 = 8 bytes

bit 23-21 **Unimplemented:** Read as '0'

bit 20 **TXDPB:** TX Endpoint Double-packet Buffering Control bit
1 = Double-packet buffer is supported. This doubles the size set in TXFIFOSZ.
0 = Double-packet buffer is not supported

TABLE 12-7: PORTC REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	—	—	—	—	—	F000
0220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUC15	CNPUC14	CNPUC13	CNPUC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
0260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDC15	CNPDC14	CNPDC13	CNPDC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
0270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0280	CNENC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNENC15	CNENC14	CNENC13	CNENC12													0000
0290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATC15	CNSTATC14	CNSTATC13	CNSTATC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
02A0	CNNEC	31:16	—	—		—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEC15	CNNEC14	CNNEC13	CNNEC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
02B0	CNFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFC15	CNFC14	CNFC13	CNFC12	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

14.0 TIMER2/3, TIMER4/5, TIMER6/7, AND TIMER8/9

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32MZ EF family of devices features eight synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events.

The following modes are supported:

- Synchronous internal 16-bit timer
- Synchronous internal 16-bit gated timer
- Synchronous external 16-bit timer

Four 32-bit synchronous timers are available by combining Timer2 with Timer3, Timer4 with Timer5, Timer6 with Timer7, and Timer8 with Timer9.

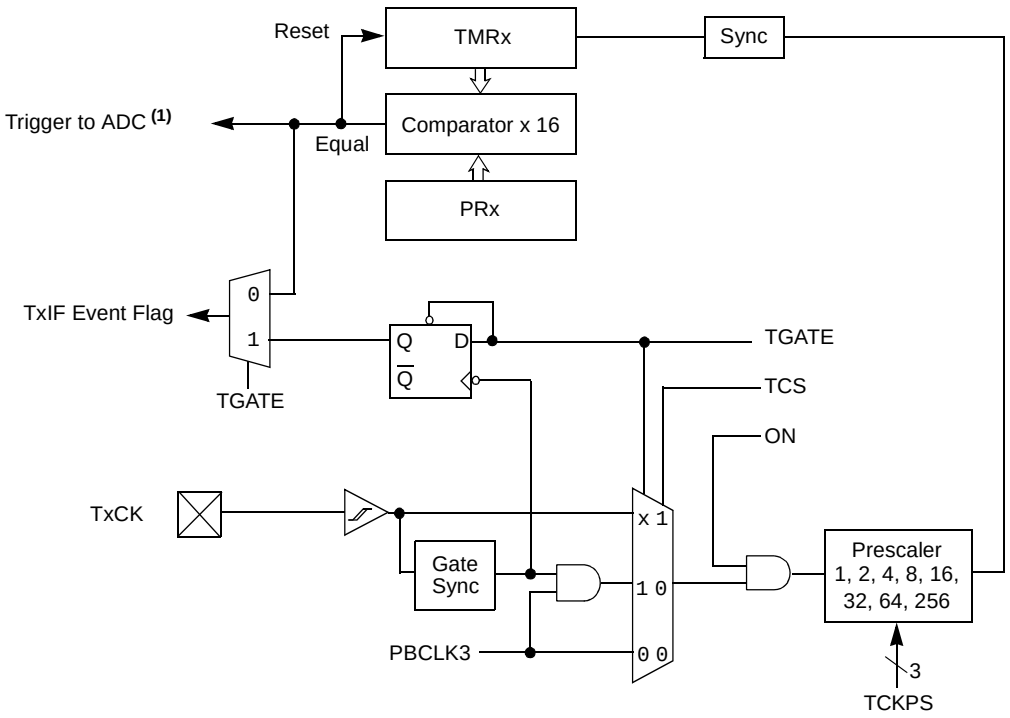
The 32-bit timers can operate in one of three modes:

- Synchronous internal 32-bit timer
- Synchronous internal 32-bit gated timer
- Synchronous external 32-bit timer

14.1 Additional Supported Features

- Selectable clock prescaler
- Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (Timer2 through Timer7 only)
- ADC event trigger (Timer3 and Timer5 only)
- Fast bit manipulation using CLR, SET, and INV registers

FIGURE 14-1: TIMER2 THROUGH TIMER9 BLOCK DIAGRAM (16-BIT)



Note 1: The ADC event trigger is available on Timer3 and Timer5 only.

NOTES:

17.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin.

Capture events are caused by the following:

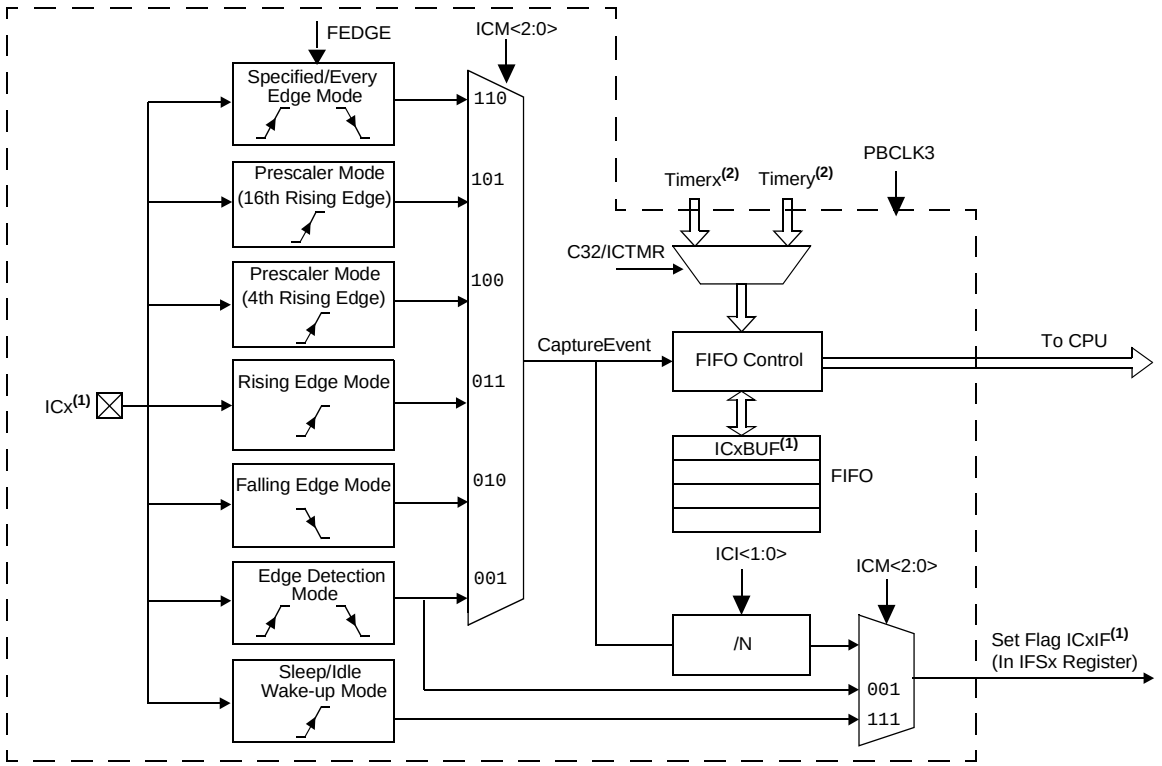
- Capture timer value on every edge (rising and falling), specified edge first
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of six 16-bit timers for the time base, or two of six 16-bit timers together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values; Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

FIGURE 17-1: INPUT CAPTURE BLOCK DIAGRAM



Note 1: An 'x' in a signal, register or bit name denotes the number of the capture channel.

2: See Table 17-1 for Timerx and Timery selections.

REGISTER 23-7: PMSTAT: PARALLEL PORT STATUS REGISTER (SLAVE MODES ONLY)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0, HS, SC	U-0	U-0	R-0	R-0	R-0	R-0
	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7:0	R-1	R/W-0, HS, SC	U-0	U-0	R-1	R-1	R-1	R-1
	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E

Legend:	HS = Hardware Set	SC = Software Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **IBF:** Input Buffer Full Status bit
- 1 = All writable input buffer registers are full
- 0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
- 1 = A write attempt to a full input byte buffer is occurred (must be cleared in software)
- 0 = No overflow is occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer x Status Full bits
- 1 = Input Buffer contains data that has not been read (reading buffer will clear this bit)
- 0 = Input Buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
- 1 = All readable output buffer registers are empty
- 0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
- 1 = A read occurred from an empty output byte buffer (must be cleared in software)
- 0 = No underflow is occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer x Status Empty bits
- 1 = Output buffer is empty (writing data to the buffer will clear this bit)
- 0 = Output buffer contains data that has not been transmitted

REGISTER 26-3: CEBDADDR: CRYPTO ENGINE BUFFER DESCRIPTOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BDPADDR<31:0>:** Current Buffer Descriptor Process Address Status bits

These bits contain the current descriptor address that is being processed by the Buffer Descriptor Processor (BDP).

REGISTER 26-4: CEBDPADDR: CRYPTO ENGINE BUFFER DESCRIPTOR PROCESSOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BASEADDR<31:0>:** Buffer Descriptor Base Address bits

These bits contain the physical address of the first Buffer Descriptor in the Buffer Descriptor chain. When enabled, the Crypto DMA begins fetching Buffer Descriptors from this address.

REGISTER 28-2: ADCCON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BGVRRDY	REFFLT	EOSRDY	CVDCPL<2:0>			SAMC<9:8>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SAMC<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	BGVRIEN	REFFLTIEN	EOSIEN	ADCEIOVR	—	ADCEIS<2:0>		
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	ADCDIV<6:0>						

Legend:	HC = Hardware Set	HS = Hardware Cleared	r = Reserved
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **BGVRRDY:** Band Gap Voltage/ADC Reference Voltage Status bit

1 = Both band gap voltage and ADC reference voltages (V_{REF}) are ready
0 = Either or both band gap voltage and ADC reference voltages (V_{REF}) are not ready

Data processing is valid only after BGVRRDY is set by hardware, so the application code must check that the BGVRRDY bit is set to ensure data validity. This bit set to '0' when ON (ADCCON1<15>) = 0.

bit 30 **REFFLT:** Band Gap/V_{REF}/AV_{DD} BOR Fault Status bit

1 = Fault in band gap or the V_{REF} voltage while the ON bit (ADCCON1<15>) was set. Most likely a band gap or V_{REF} fault will be caused by a BOR of the analog V_{DD} supply.
0 = Band gap and V_{REF} voltage are working properly

This bit is cleared when the ON bit (ADCCON1<15>) = 0 and the BGVRRDY bit = 1.

bit 29 **EOSRDY:** End of Scan Interrupt Status bit

1 = All analog inputs are considered for scanning through the scan trigger (all analog inputs specified in the ADCCSS1 and ADCCSS2 registers) have completed scanning
0 = Scanning has not completed

This bit is cleared when ADCCON2<31:24> are read in software.

bit 28-26 **CVDCPL<2:0>:** Capacitor Voltage Divider (CVD) Setting bit

111 = 7 * 2.5 pF = 17.5 pF
110 = 6 * 2.5 pF = 15 pF
101 = 5 * 2.5 pF = 12.5 pF
100 = 4 * 2.5 pF = 10 pF
011 = 3 * 2.5 pF = 7.5 pF
010 = 2 * 2.5 pF = 5 pF
001 = 1 * 2.5 pF = 2.5 pF
000 = 0 * 2.5 pF = 0 pF

bit 25-16 **SAMC<9:0>:** Sample Time for the Shared ADC (ADC7) bits

1111111111 = 1025 T_{AD7}
•
•
•
0000000001 = 3 T_{AD7}
0000000000 = 2 T_{AD7}

Where T_{AD7} = period of the ADC conversion clock for the Shared ADC (ADC7) controlled by the ADCDIV<6:0> bits.

bit 15 **BGVRIEN:** Band Gap/V_{REF} Voltage Ready Interrupt Enable bit

1 = Interrupt will be generated when the BGVRDDY bit is set
0 = No interrupt is generated when the BGVRRDY bit is set

REGISTER 29-5: CiTREC: CAN TRANSMIT/RECEIVE ERROR COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	TERRCNT<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RERRCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21 **TXBO:** Transmitter in Error State Bus OFF (TERRCNT ≥ 256)

bit 20 **TXBP:** Transmitter in Error State Bus Passive (TERRCNT ≥ 128)

bit 19 **RXBP:** Receiver in Error State Bus Passive (RERRCNT ≥ 128)

bit 18 **TXWARN:** Transmitter in Error State Warning (128 > TERRCNT ≥ 96)

bit 17 **RXWARN:** Receiver in Error State Warning (128 > RERRCNT ≥ 96)

bit 16 **EWARN:** Transmitter or Receiver is in Error State Warning

bit 15-8 **TERRCNT<7:0>:** Transmit Error Counter

bit 7-0 **RERRCNT<7:0>:** Receive Error Counter

REGISTER 29-6: CiFSTAT: CAN FIFO STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **FIFOIP<31:0>:** FIFOx Interrupt Pending bits

1 = One or more enabled FIFO interrupts are pending

0 = No FIFO interrupts are pending

REGISTER 29-10: CiFLTCON0: CAN FILTER CONTROL REGISTER 0 (CONTINUED)

bit 15 **FLTEN1:** Filter 1 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL1<1:0>:** Filter 1 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL1<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN0:** Filter 0 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL0<1:0>:** Filter 0 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL0<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-1: ETHCON1: ETHERNET CONTROLLER CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTV<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTV<7:0>							
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	—	—	—	TXRTS	RXEN(1)
7:0	R/W-0	U-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0
	AUTOFC	—	—	MANFC	—	—	—	BUFCDEC

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **PTV<15:0>:** PAUSE Timer Value bits

PAUSE Timer Value used for Flow Control.
This register should only be written when RXEN (ETHCON1<8>) is not set.

These bits are only used for Flow Control operations.

bit 15 **ON:** Ethernet ON bit

1 = Ethernet module is enabled
0 = Ethernet module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Ethernet Stop in Idle Mode bit

1 = Ethernet module transfers are paused during Idle mode
0 = Ethernet module transfers continue during Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **TXRTS:** Transmit Request to Send bit

1 = Activate the TX logic and send the packet(s) defined in the TX EDT
0 = Stop transmit (when cleared by software) or transmit done (when cleared by hardware)

After the bit is written with a '1', it will clear to a '0' whenever the transmit logic has finished transmitting the requested packets in the Ethernet Descriptor Table (EDT). If a '0' is written by the CPU, the transmit logic finishes the current packet's transmission and then stops any further.

This bit only affects TX operations.

bit 8 **RXEN:** Receive Enable bit(1)

1 = Enable RX logic, packets are received and stored in the RX buffer as controlled by the filter configuration
0 = Disable RX logic, no packets are received in the RX buffer

This bit only affects RX operations.

Note 1: It is not recommended to clear the RXEN bit and then make changes to any RX related field/register. The Ethernet Controller must be reinitialized (ON cleared to '0'), and then the RX changes applied.

REGISTER 34-4: DEVCFG1/ADEVCFG1: DEVICE CONFIGURATION WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FDMTEN	DMTCNT<4:0>					FWDTWINSZ<1:0>	
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>				
15:8	R/P	R/P	r-1	r-1	r-1	R/P	R/P	R/P
	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	IESO	FSOSCEN	DMTINTV<2:0>			FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FDMTEN:** Deadman Timer enable bit
1 = Deadman Timer is enabled and *cannot* be disabled by software
0 = Deadman Timer is disabled and *can* be enabled by software

bit 30-26 **DMTCNT<4:0>:** Deadman Timer Count Select bits
11111 = Reserved
•
•
•
11000 = Reserved
10111 = 2^{31} (2147483648)
10110 = 2^{30} (1073741824)
10101 = 2^{29} (536870912)
10100 = 2^{28} (268435456)
•
•
•
00001 = 2^{9} (512)
00000 = 2^{8} (256)

bit 25-24 **FWDTWINSZ<1:0>:** Watchdog Timer Window Size bits
11 = Window size is 25%
10 = Window size is 37.5%
01 = Window size is 50%
00 = Window size is 75%

bit 23 **FWDTEN:** Watchdog Timer Enable bit
1 = Watchdog Timer is enabled and cannot be disabled by software
0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS:** Watchdog Timer Window Enable bit
1 = Watchdog Timer is in non-Window mode
0 = Watchdog Timer is in Window mode

bit 21 **WDTSPGM:** Watchdog Timer Stop During Flash Programming bit
1 = Watchdog Timer stops during Flash programming
0 = Watchdog Timer runs during Flash programming (for read/execute while programming Flash applications)

TABLE 37-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions(1)**
DO20	VOH	**Output High Voltage** I/O Pins: 4x Source Driver Pins - RA3, RA9, RA10, RA14, RA15 RB0-RB2, RB4, RB6-RB7, RB11, RB13 RC12-RC15 RD0, RD6-RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8 RG15 RH0, RH1, RH4-RH6, RH8-RH13 RJ0-RJ2, RJ8, RJ9, RJ11	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V
		Output High Voltage I/O Pins: 8x Source Driver Pins - RA0-RA2, RA4, RA5 RB3, RB5, RB8-RB10, RB12, RB14, RB15 RC1-RC4 RD1-RD5, RD9, RD10, RD12, RD13, RD15 RE4-RE7 RF0, RF4, RF5, RF12, RF13 RG0, RG1, RG6-RG9 RH2, RH3, RH7, RH14, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	2.4	—	—	V	IOH ≥ -15 mA, VDD = 3.3V
		Output High Voltage I/O Pins: 12x Source Driver Pins - RA6, RA7 RE0-RE3 RF1 RG12-RG14	2.4	—	—	V	IOH ≥ -20 mA, VDD = 3.3V

Note 1: Parameters are characterized, but not tested.

TABLE 37-14: COMPARATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	—	±10	—	mV	AVDD = VDD, AVSS = VSS
D301	VICM	Input Common Mode Voltage	0	—	VDD	V	AVDD = VDD, AVSS = VSS **(Note 2)**
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	Max VICM = (VDD – 1)V **(Note 2, 4)**
D303	TRESP	Response Time	—	150	—	ns	AVDD = VDD, AVSS = VSS **(Notes 1, 2)**
D304	ON2OV	Comparator Enabled to Output Valid	—	—	10	µs	Comparator module is configured before setting the comparator ON bit **(Note 2)**
D305	IVREF	Internal Voltage Reference	1.194	1.2	1.206	V	—

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

2: These parameters are characterized but not tested.

3: The Comparator module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

4: CMRR measurement characterized with a 1 MΩ resistor in parallel with a 25 pF capacitor to VSS.

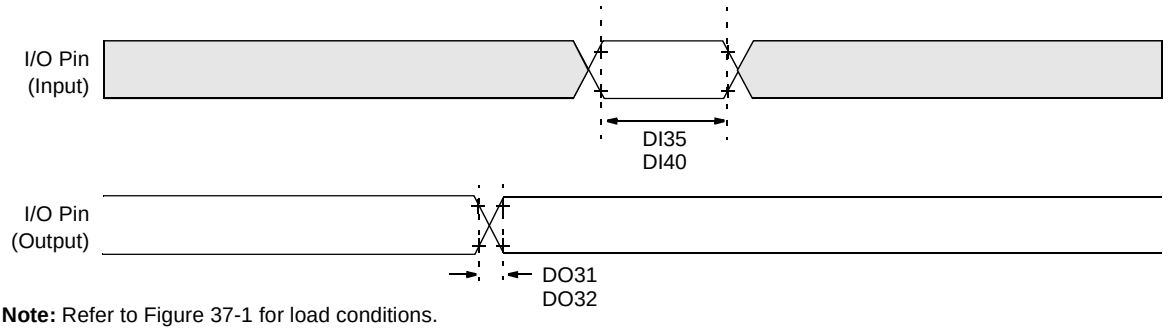
TABLE 37-15: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time	—	—	10	µs	See **Note 1**
D313	DACREFH	CVREF Input Voltage Reference Range	AVSS	—	AVDD	V	CVRSRC with CVRSS = 0
			VREF-	—	VREF+	V	CVRSRC with CVRSS = 1
D314	DVREF	CVREF Programmable Output Range	0	—	0.625 x DACREFH	V	0 to 0.625 DACREFH with DACREFH/24 step size
			0.25 x DACREFH	—	0.719 x DACREFH	V	0.25 x DACREFH to 0.719 DACREFH with DACREFH/32 step size
D315	DACRES	Resolution	—	—	DACREFH/24		CVRCON<CVRR> = 1
			—	—	DACREFH/32		CVRCON<CVRR> = 0
D316	DACACC	Absolute Accuracy(2)	—	—	1/4	LSB	DACREFH/24, CVRCON<CVRR> = 1
			—	—	1/2	LSB	DACREFH/32, CVRCON<CVRR> = 0

Note 1: Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

2: These parameters are characterized but not tested.

FIGURE 37-3: I/O TIMING CHARACTERISTICS



Note: Refer to Figure 37-1 for load conditions.

FIGURE 37-26: TRANSMIT SIGNAL TIMING RELATIONSHIPS AT THE MII

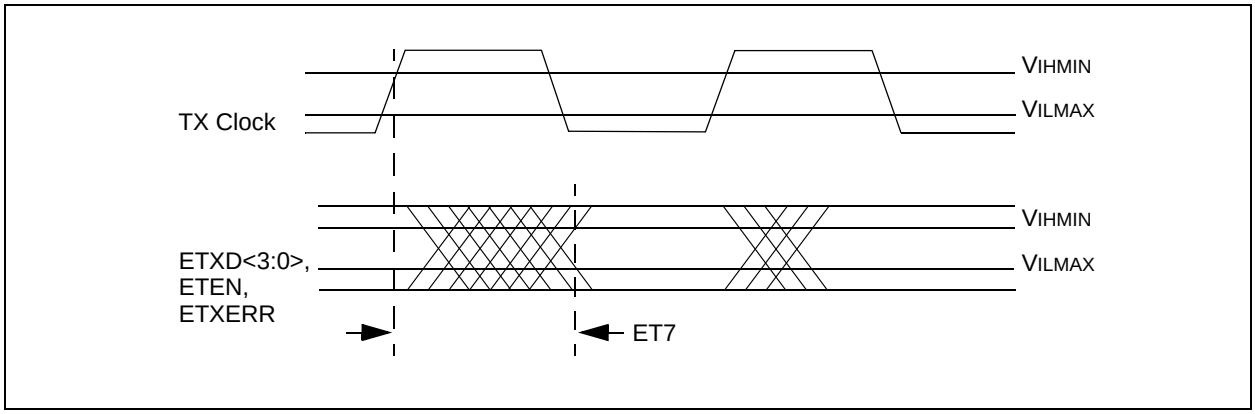
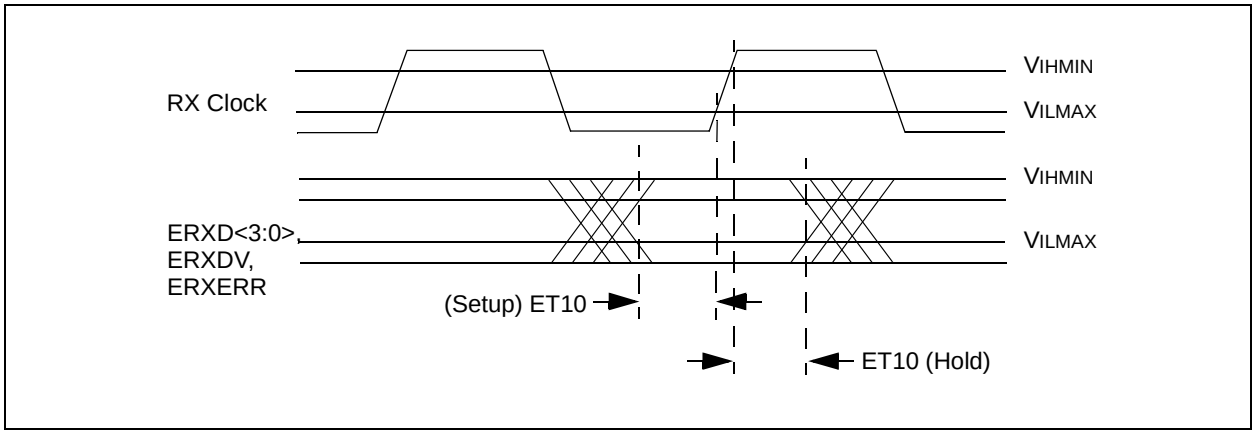


FIGURE 37-27: RECEIVE SIGNAL TIMING RELATIONSHIPS AT THE MII



B.2 Analog-to-Digital Converter (ADC)

The PIC32MZ EC family features a Pipelined ADC module, while the PIC32MZ EF family of devices has an entirely new 12-bit High-Speed SAR ADC module. Nearly all registers in this new ADC module differ from the registers in PIC32MZ EC devices. Due to this difference, code will not port from PIC32MZ EC devices to PIC32MZ EF devices. Table B-2 lists some of the differences in registers to note to adapt code as quickly as possible.

TABLE B-2: ADC DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
Clock Selection and Operating Frequency (TAD)	
On PIC32MZ EC devices, there are three possible sources of the ADC clock: FRC, REFCLKO3, and SYSCLK.	On PIC32MZ EF devices, there are four sources for the ADC clock. In addition to the ones for PIC32MZ EC, PBCLK4 is added as a source. Also, the clock source selection is in a different register.
ADCSEL<1:0> (AD1CON1<9:8>) 11 = FRC 10 = REFCLKO3 01 = SYSCLK 00 = Reserved	ADCSEL<1:0> (ADCCON3<31:30>) 11 = FRC 10 = REFCLKO3 01 = SYSCLK **00 = PBCLK4**
Scan Trigger Sources	
On PIC32MZ EC devices, there are 10 available trigger sources for starting ADC sampling and conversion.	On PIC32MZ EF devices, two new sources have been added. One is a shared trigger source (STRIG). The other is a Global Level Software Trigger (GLSWTRG). With the GLSWTRG, the conversions continue until the bit is cleared in software.
STRGSRC<4:0> (AD1CON1<26:22>) 11111 = Reserved • • • 01101 = Reserved 01100 = Comparator 2 COUT 01011 = Comparator 1 COUT 01010 = OCMP5 01001 = OCMP3 01000 = OCMP1 00111 = TMR5 match 00110 = TMR3 match 00101 = TMR1 match 00100 = INT0 **00011 = Reserved** **00010 = Reserved** 00001 = Global Software Trigger (GSWTRG) 00000 = No trigger	TRGSRC<4:0> (ADCTRGx<y:z>) 11111 = Reserved • • • 01101 = Reserved 01100 = Comparator 2 COUT 01011 = Comparator 1 COUT 01010 = OCMP5 01001 = OCMP3 01000 = OCMP1 00111 = TMR5 match 00110 = TMR3 match 00101 = TMR1 match 00100 = INT0 **00011 = STRIG** **00010 = Global Level Software Trigger (GLSWTRG)** 00001 = Global Software Trigger (GSWTRG) 00000 = No trigger
Debug Mode	
On PIC32MZ EC devices, the ADC module continues operating when stopping on a breakpoint during debugging.	On PIC32MZ EF devices, the ADC module will stop during debugging when stopping on a breakpoint.
Electrical Specifications and Timing Requirements	
Refer to the **"Electrical Characteristics"** chapter in the PIC32MZ EC data sheet for ADC module specifications and timing requirements.	On PIC32MZ EF devices, the ADC module sampling and conversion time and other specifications have changed. Refer to **37.0 "Electrical Characteristics"** for more information.
ADC Calibration	
PIC32MZ EC devices require calibration values be copied into the AD1CALx registers before turning on the ADC. These values come from the DEVADCx registers.	PIC32MZ EF devices also require ADC calibration values, but the destination registers are named ADCxCAL.