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Applications of "Embedded - Microcontrollers"

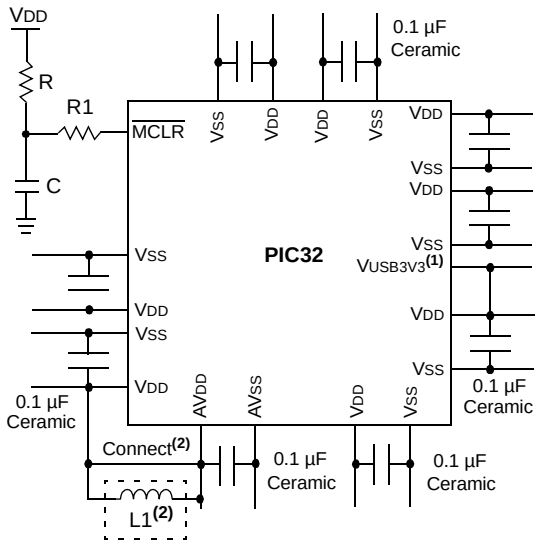
Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512eff100-e-pf

TABLE 1: PIC32MZ EF FAMILY FEATURES

Device	Program Memory (KB)	Data Memory (KB)	Pins	Packages	Boot Flash Memory (KB)	Remappable Peripherals						Crypto	RNG	DMA Channels (Programmable/ Dedicated)	ADC (Channels)	Analog Comparators	USB 2.0 HS OTG	I^2C	PMP	EBI	SQI	RTCC	Ethernet	I/O Pins	JTAG	Trace
						Remappable Pins	Timers/ Capture/ Compare[(1)]	UART	SPI/I^2S	External Interrupts[(2)]	CAN 2.0B															
PIC32MZ0512EFE064	512	128	64	TQFP, QFN	160	34	9/9/9	6	4	5	0	N	Y	8/12	24	2	Y	4	Y	N	Y	Y	Y	46	Y	Y
PIC32MZ0512EFF064											2	N	Y	8/16												
PIC32MZ0512EFK064											2	Y	Y	8/18												
PIC32MZ1024EFE064	1024	256									0	N	Y	8/12												
PIC32MZ1024EFF064											2	N	Y	8/16												
PIC32MZ1024EFK064											2	Y	Y	8/18												
PIC32MZ0512EFE100	512	128	100	TQFP	160	51	9/9/9	6	6	5	0	N	Y	8/12	40	2	Y	5	Y	Y	Y	Y	Y	78	Y	Y
PIC32MZ0512EFF100											2	N	Y	8/16												
PIC32MZ0512EFK100											2	Y	Y	8/18												
PIC32MZ1024EFE100	1024	256									0	N	Y	8/12												
PIC32MZ1024EFF100											2	N	Y	8/16												
PIC32MZ1024EFK100											2	Y	Y	8/18												
PIC32MZ0512EFE124	512	128	124	VTLA	160	53	9/9/9	6	6	5	0	N	Y	8/12	48	2	Y	5	Y	Y	Y	Y	Y	97	Y	Y
PIC32MZ0512EFF124											2	N	Y	8/16												
PIC32MZ0512EFK124											2	Y	Y	8/18												
PIC32MZ1024EFE124	1024	256									0	N	Y	8/12												
PIC32MZ1024EFF124											2	N	Y	8/16												
PIC32MZ1024EFK124											2	Y	Y	8/18												
PIC32MZ0512EFE144	512	128	144	LQFP, TQFP	160	53	9/9/9	6	6	5	0	N	Y	8/12	48	2	Y	5	Y	Y	Y	Y	Y	120	Y	Y
PIC32MZ0512EFF144											2	N	Y	8/16												
PIC32MZ0512EFK144											2	Y	Y	8/18												
PIC32MZ1024EFE144	1024	256									0	N	Y	8/12												
PIC32MZ1024EFF144											2	N	Y	8/16												
PIC32MZ1024EFK144											2	Y	Y	8/18												

Note 1: Eight out of nine timers are remappable.
2: Four out of five external interrupts are remappable.
3: This device is available with a 252 MHz speed rating.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: If the USB module is not used, this pin must be connected to VSS.

2: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{FCNV}{2} \quad \text{(i.e., ADC conversion rate/2)}$$

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

2.3 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

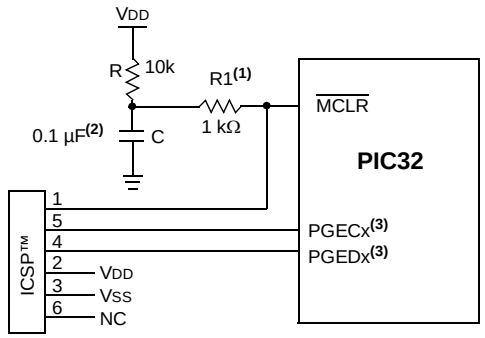
- Device Reset
- Device programming and debugging

Pulling The MCLR pin low generates either a device Reset or a POR, depending on the setting of the SMCLR bit (DEVCFG0<15>). Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Note 1: 470Ω ≤ R1 ≤ 1kΩ will limit any current flowing into MCLR from the external capacitor C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met without interfering with the Debug/Programmer tools.

2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

3: No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

A block diagram of the PIC32MZ EF family processor core is shown in Figure 3-1.

FIGURE 3-1: PIC32MZ EF FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM

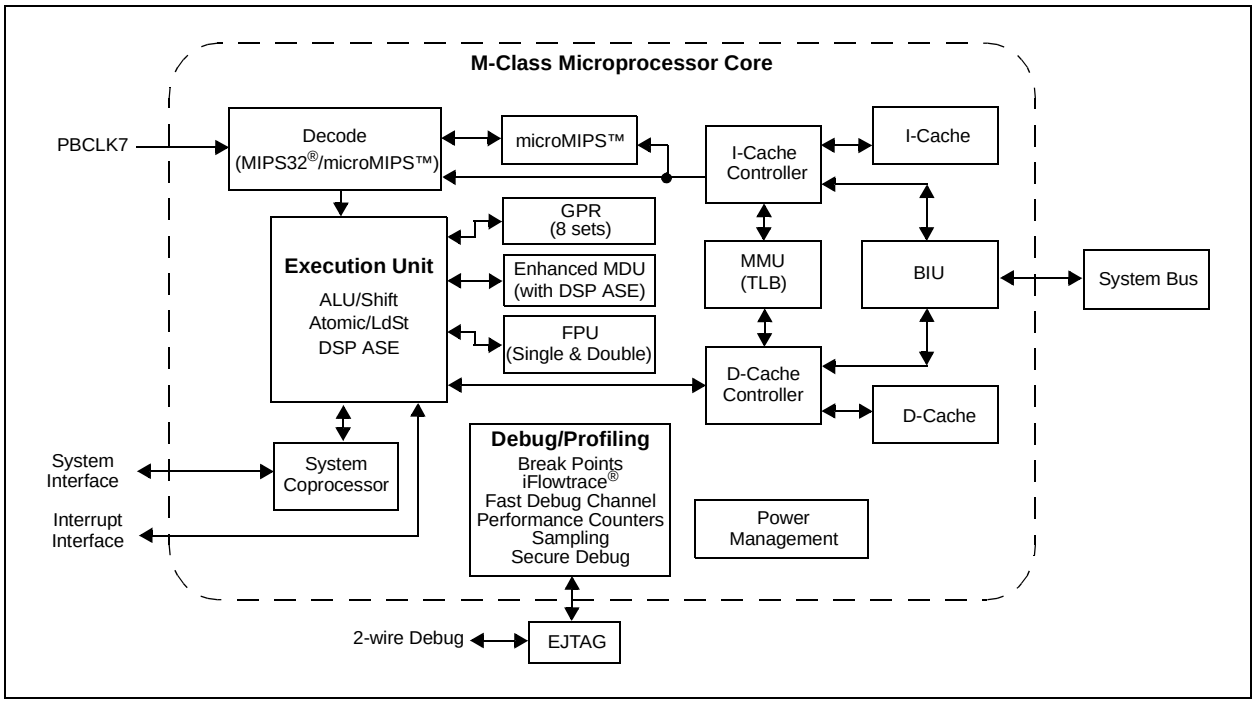


TABLE 4-3: BOOT FLASH 2 SEQUENCE AND CONFIGURATION WORDS SUMMARY

Virtual Address (BFC6_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FF40	ABF2DEVCFG3	31:0	**Note:** See Table 34-2 for the bit descriptions.																xxxx
FF44	ABF2DEVCFG2	31:0																	xxxx
FF48	ABF2DEVCFG1	31:0																	xxxx
FF4C	ABF2DEVCFG0	31:0																	xxxx
FF50	ABF2DEVCP3	31:0																	xxxx
FF54	ABF2DEVCP2	31:0																	xxxx
FF58	ABF2DEVCP1	31:0																	xxxx
FF5C	ABF2DEVCP0	31:0																	xxxx
FF60	ABF2DEVSIGN3	31:0																	xxxx
FF64	ABF2DEVSIGN2	31:0																	xxxx
FF68	ABF2DEVSIGN1	31:0																	xxxx
FF6C	ABF2DEVSIGN0	31:0																	xxxx
FFC0	BF2DEVCFG3	31:0	**Note:** See Table 34-1 for the bit descriptions.																xxxx
FFC4	BF2DEVCFG2	31:0																	xxxx
FFC8	BF2DEVCFG1	31:0																	xxxx
FFCC	BF2DEVCFG0	31:0																	xxxx
FFD0	BF2DEVCP3	31:0																	xxxx
FFD4	BF2DEVCP2	31:0																	xxxx
FFD8	BF2DEVCP1	31:0																	xxxx
FFDC	BF2DEVCP0	31:0																	xxxx
FFE0	BF2DEVSIGN3	31:0																	xxxx
FFE4	BF2DEVSIGN2	31:0																	xxxx
FFE8	BF2DEVSIGN1	31:0																	xxxx
FFEC	BF2DEVSIGN0	31:0																	xxxx
FFF0	BF2SEQ3	31:16	CSEQ<15:0>																xxxx
		15:0	TSEQ<15:0>																xxxx
FFF4	BF2SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFF8	BF2SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFFC	BF2SEQ0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
07E0	OFF168	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E4	OFF169	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E8	OFF170	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07EC	OFF171	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F0	OFF172	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F4	OFF173	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F8	OFF174	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07FC	OFF175	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0800	OFF176(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0804	OFF177(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0808	OFF178(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
080C	OFF179	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0810	OFF180	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0814	OFF181	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0818	OFF182	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

REGISTER 11-3: USBCSR2: USB CONTROL STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0
	VBUSERRIE	SESSRQIE	DISCONIE	CONNIE	SOFIE	RESETIE	RESUMEIE	SUSPIE
23:16	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS
	VBUSERRIF	SESSRQIF	DISCONIF	CONNIF	SOFIF	RESETIF	RESUMEIF	SUSPIF
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	U-0
	EP7RXIE	EP6RXIE	EP5RXIE	EP4RXIE	EP3RXIE	EP2RXIE	EP1RXIE	—

Legend:	HS = Hardware Set		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **VBUSERRIE:** VBUS Error Interrupt Enable bit
1 = VBUS error interrupt is enabled
0 = VBUS error interrupt is disabled

bit 30 **SESSRQIE:** Session Request Interrupt Enable bit
1 = Session request interrupt is enabled
0 = Session request interrupt is disabled

bit 29 **DISCONIE:** Device Disconnect Interrupt Enable bit
1 = Device disconnect interrupt is enabled
0 = Device disconnect interrupt is disabled

bit 28 **CONNIE:** Device Connection Interrupt Enable bit
1 = Device connection interrupt is enabled
0 = Device connection interrupt is disabled

bit 27 **SOFIE:** Start of Frame Interrupt Enable bit
1 = Start of Frame event interrupt is enabled
0 = Start of Frame event interrupt is disabled

bit 26 **RESETIE:** Reset/Babble Interrupt Enable bit
1 = Interrupt when reset (*Device mode*) or Babble (*Host mode*) is enabled
0 = Reset/Babble interrupt is disabled

bit 25 **RESUMEIE:** Resume Interrupt Enable bit
1 = Resume signaling interrupt is enabled
0 = Resume signaling interrupt is disabled

bit 24 **SUSPIE:** Suspend Interrupt Enable bit
1 = Suspend signaling interrupt is enabled
0 = Suspend signaling interrupt is disabled

bit 23 **VBUSERRIF:** VBUS Error Interrupt bit
1 = VBUS has dropped below the VBUS valid threshold during a session
0 = No interrupt

bit 22 **SESSRQIF:** Session Request Interrupt bit
1 = Session request signaling has been detected
0 = No session request detected

bit 21 **DISCONIF:** Device Disconnect Interrupt bit
1 = In *Host mode*, indicates when a device disconnect is detected. In *Device mode*, indicates when a session ends.
0 = No device disconnect detected

bit 20 **CONNIF:** Device Connection Interrupt bit
1 = In *Host mode*, indicates when a device connection is detected
0 = No device connection detected

REGISTER 11-15: USBHWVER: USB HARDWARE VERSION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-1	R-0	R-0	R-0
	RC	VERMAJOR<4:0>					VERMINOR<9:8>	
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERMINOR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **RC:** Release Candidate bit
1 = USB module was created using a release candidate
0 = USB module was created using a full release

bit 14-10 **VERMAJOR<4:0>:** USB Module Major Version number bits
This read-only number is the Major version number for the USB module.

bit 9-0 **VERMINOR<9:0>:** USB Module Minor Version number bits
This read-only number is the Minor version number for the USB module.

TABLE 12-10: PORTD REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	TRISD11	TRISD10	TRISD9	—	—	—	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	0E3F
0320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	RD11	RD10	RD9	—	—	—	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
0330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LATD11	LATD10	LATD9	—	—	—	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
0340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ODCD11	ODCD10	ODCD9	—	—	—	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
0350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNPUD11	CNPUD10	CNPUD9	—	—	—	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
0360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNPDD11	CNPDD10	CNPDD9	—	—	—	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
0370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNEND11	CNEND10	CNEND9				CNEND5	CNEND4	CNEND3	CNEND2	CNEND1	CNEND0	0000
0390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CN STATD11	CN STATD10	CN STATD9	—	—	—	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	CN STATD0	0000
03A0	CNNED	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNNED11	CNNED10	CNNED9	—	—	—	CNNED5	CNNED4	CNNED3	CNNED2	CNNED1	CNNED0	0000
03B0	CNFD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNFD11	CNFD10	CNFD9	—	—	—	CNFD5	CNFD4	CNFD3	CNFD2	CNFD1	CNFD0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

17.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin.

Capture events are caused by the following:

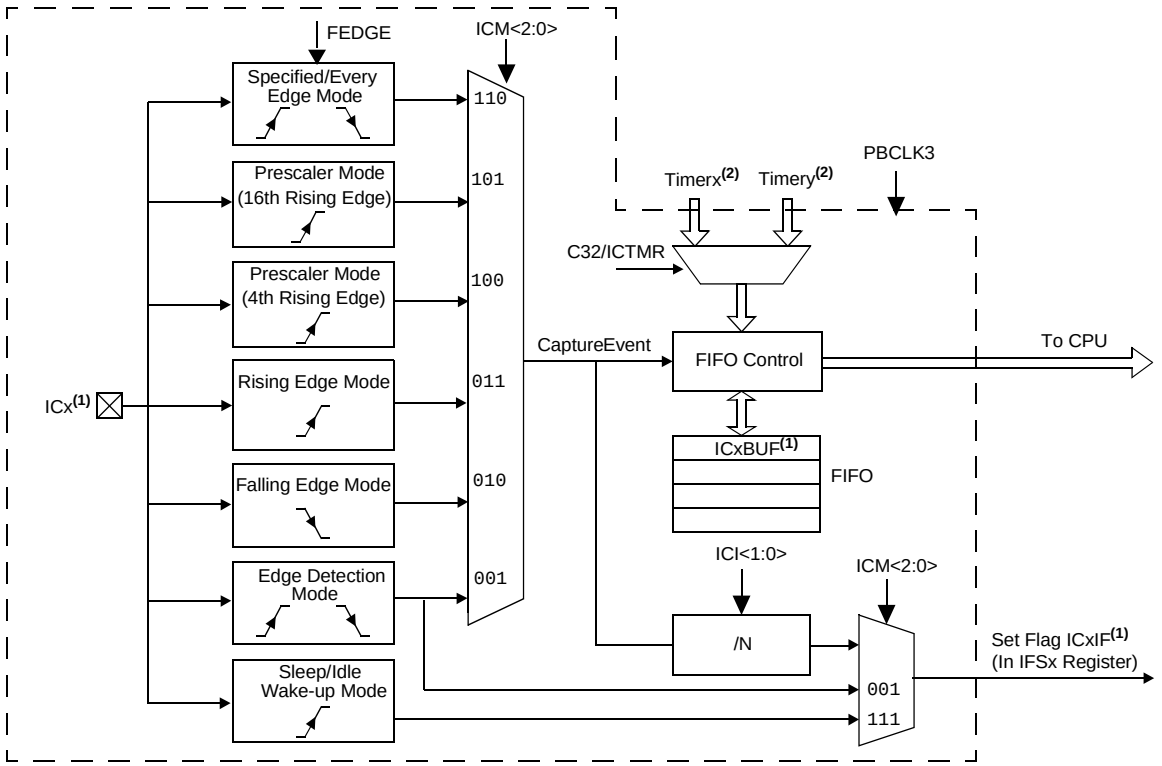
- Capture timer value on every edge (rising and falling), specified edge first
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of six 16-bit timers for the time base, or two of six 16-bit timers together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values; Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

FIGURE 17-1: INPUT CAPTURE BLOCK DIAGRAM



Note 1: An 'x' in a signal, register or bit name denotes the number of the capture channel.

2: See Table 17-1 for Timerx and Timery selections.

The timer source for each Input Capture module depends on the setting of the ICACLK bit in the CFGCON register. The available configurations are shown in Table 17-1.

TABLE 17-1: TIMER SOURCE CONFIGURATIONS

Input Capture Module	Timerx	Timery
ICACLK (CFGCON<17>) = 0		
IC1 • • • IC9	Timer2 • • • Timer2	Timer3 • • • Timer3
ICACLK (CFGCON<17>) = 1		
IC1	Timer4	Timer5
IC2	Timer4	Timer5
IC3	Timer4	Timer5
IC4	Timer2	Timer3
IC5	Timer2	Timer3
IC6	Timer2	Timer3
IC7	Timer6	Timer7
IC8	Timer6	Timer7
IC9	Timer6	Timer7

NOTES:

REGISTER 24-2: EBIMSKx: EXTERNAL BUS INTERFACE ADDRESS MASK REGISTER ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	REGSEL<2:0>		
7:0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MEMTYPE<2:0>			MEMSIZE<4:0>(1)				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **REGSEL<2:0>:** Timing Register Set for Chip Select 'x' bits
111 = Reserved
•
•
•
011 = Reserved
010 = Use EBISMT2
001 = Use EBISMT1
000 = Use EBISMT0

bit 7-5 **MEMTYPE<2:0>:** Select Memory Type for Chip Select 'x' bits
111 = Reserved
•
•
•
011 = Reserved
010 = NOR-Flash
001 = SRAM
000 = Reserved

bit 4-0 **MEMSIZE<4:0>:** Select Memory Size for Chip Select 'x' bits(1)
11111 = Reserved
•
•
•
01010 = Reserved
01001 = 16 MB
01000 = 8 MB
00111 = 4 MB
00110 = 2 MB
00101 = 1 MB
00100 = 512 KB
00011 = 256 KB
00010 = 128 KB
00001 = 64 KB (smaller memories alias within this range)
00000 = Chip Select is not used

Note 1: The specified value for these bits depends on the number of available address lines. Refer to the specific device pin table (Table 2 through Table 5) for the available address lines.

REGISTER 29-1: CiCON: CAN MODULE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	S/HC-0	R/W-1	R/W-0	R/W-0
	—	—	—	—	ABAT	REQOP<2:0>		
23:16	R-1	R-0	R-0	R/W-0	U-0	U-0	U-0	U-0
	OPMOD<2:0>			CANCAP	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R-0	U-0	U-0	U-0
	ON(1)	—	SIDLE	—	CANBUSY	—	—	—
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DNCNT<4:0>				

Legend:	HC = Hardware Clear	S = Settable bit	
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-28 **Unimplemented:** Read as ‘0’

bit 27 **ABAT:** Abort All Pending Transmissions bit
1 = Signal all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions aborted

bit 26-24 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved - Do not use
101 = Reserved - Do not use
100 = Set Configuration mode
011 = Set Listen Only mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode

bit 23-21 **OPMOD<2:0>:** Operation Mode Status bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 20 **CANCAP:** CAN Message Receive Time Stamp Timer Capture Enable bit
1 = CANTMR value is stored on valid message reception and is stored with the message
0 = Disable CAN message receive time stamp timer capture and stop CANTMR to conserve power

bit 19-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** CAN On bit(1)
1 = CAN module is enabled
0 = CAN module is disabled

bit 14 **Unimplemented:** Read as ‘0’

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

TABLE 34-5: DEVICE ADC CALIBRATION SUMMARY

Virtual Address (BFC5_#)	Register Name	Bit Range	Bits															All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4000	DEVADC0	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
4004	DEVADC1	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
4008	DEVADC2	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
400C	DEVADC3	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
4010	DEVADC4	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
401C	DEVADC7	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx

Legend: x = unknown value on Reset.
Note 1: Reset values are dependent on the device variant.

REGISTER 34-5: DEVCFG2/ADEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	R/P	r-1	r-1	r-1	r-1	r-1	r-1
	—	UPLLFSEL	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P
	—	—	—	—	—	FPLLODIV<2:0>		
15:8	r-1	R/P	R/P	R/P	R/P	R/P	R/P	R/P
		FPLLMULT<6:0>						
7:0	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FPLLICLK	FPLLRNG<2:0>			—	FPLLIDIV<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** Write as '1'

bit 30 **UPLLFSEL:** USB PLL Input Frequency Select bit
1 = UPLL input clock is 24 MHz
0 = UPLL input clock is 12 MHz

bit 29-19 **Reserved:** Write as '1'

bit 18-16 **FPLLODIV<2:0>:** Default System PLL Output Divisor bits
111 = PLL output divided by 32
110 = PLL output divided by 32
101 = PLL output divided by 32
100 = PLL output divided by 16
011 = PLL output divided by 8
010 = PLL output divided by 4
001 = PLL output divided by 2
000 = PLL output divided by 2

bit 15 **Reserved:** Write as '1'

bit 14-8 **FPLLMULT<6:0>:** System PLL Feedback Divider bits
1111111 = Multiply by 128
1111110 = Multiply by 127
1111101 = Multiply by 126
1111100 = Multiply by 125
•
•
•
0000000 = Multiply by 1

bit 7 **FPLLICLK:** System PLL Input Clock Select bit
1 = FRC is selected as input to the System PLL
0 = POSC is selected as input to the System PLL

bit 6-4 **FPLLRNG<2:0>:** System PLL Divided Input Clock Frequency Range bits
111 = Reserved
110 = Reserved
101 = 34-64 MHz
100 = 21-42 MHz
011 = 13-26 MHz
010 = 8-16 MHz
001 = 5-10 MHz
000 = Bypass

37.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MZ EF electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MZ EF devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Specifications for Extended Temperature devices (-40ºC to +125ºC) that are different from the specifications in this section are provided in **38.0 "Extended Temperature Electrical Characteristics"**.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias ..... -40°C to +85°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to V_{SS} **(Note 3)** ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 2.1V$ **(Note 3)** ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} < 2.1V$ **(Note 3)** ..... -0.3V to +3.6V
Voltage on D+ or D- pin with respect to V_{USB3V3} ..... -0.3V to (V_{USB3V3} + 0.3V)
Voltage on V_{BUS} with respect to V_{SS} ..... -0.3V to +5.5V
Maximum current out of V_{SS} pin(s) ..... 200 mA
Maximum current into V_{DD} pin(s) **(Note 2)** ..... 200 mA
Maximum current sunk/sourced by any 4x I/O pin **(Note 4)** ..... 15 mA
Maximum current sunk/sourced by any 8x I/O pin **(Note 4)** ..... 25 mA
Maximum current sunk/sourced by any 12x I/O pin **(Note 4)** ..... 33 mA
Maximum current sunk by all ports ..... 150 mA
Maximum current sourced by all ports **(Note 2)** ..... 150 mA

Note 1: Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 37-2).

3: See the pin name tables (Table 2 through Table 4) for the 5V tolerant pins.

4: Characterized, but not tested. Refer to parameters DO10, DO20, and DO20a for the 4x, 8x, and 12x I/O pin lists.

FIGURE 37-2: EXTERNAL CLOCK TIMING

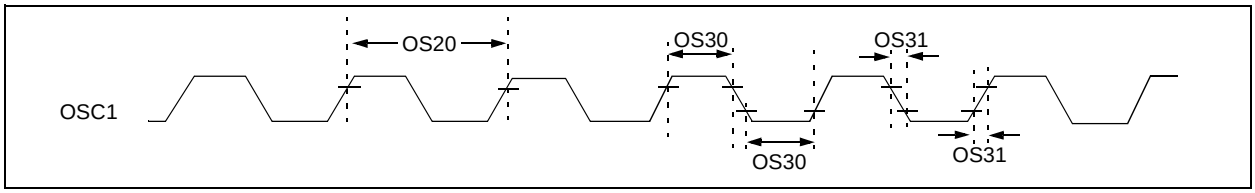


TABLE 37-17: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Minimum**	**Typical(1)**	**Maximum**	**Units**	**Conditions**
OS10	FOSC	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	64	MHz	EC **(Note 2,3)**
OS13		Oscillator Crystal Frequency	4	—	32	MHz	HS **(Note 2,3)**
OS15			32	32.768	100	kHz	SOSC **(Note 2)**
OS20	TOSC	TOSC = 1/FOSC	—	—	—	—	See parameter OS10 for FOSC value
OS30	TOSL, TOSH	External Clock In (OSC1) High or Low Time	0.375 x TOSC	—	—	ns	EC **(Note 2)**
OS31	TOSR, TOSF	External Clock In (OSC1) Rise or Fall Time	—	—	7.5	ns	EC **(Note 2)**
OS40	TOST	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, and SOSC Clock Oscillator modes)	—	1024	—	TOSC	**(Note 2)**
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	**(Note 2)**
OS42	GM	External Oscillator Transconductance	—	400	—	µA/V	VDD = 3.3V, TA = +25°C, HS **(Note 2)**

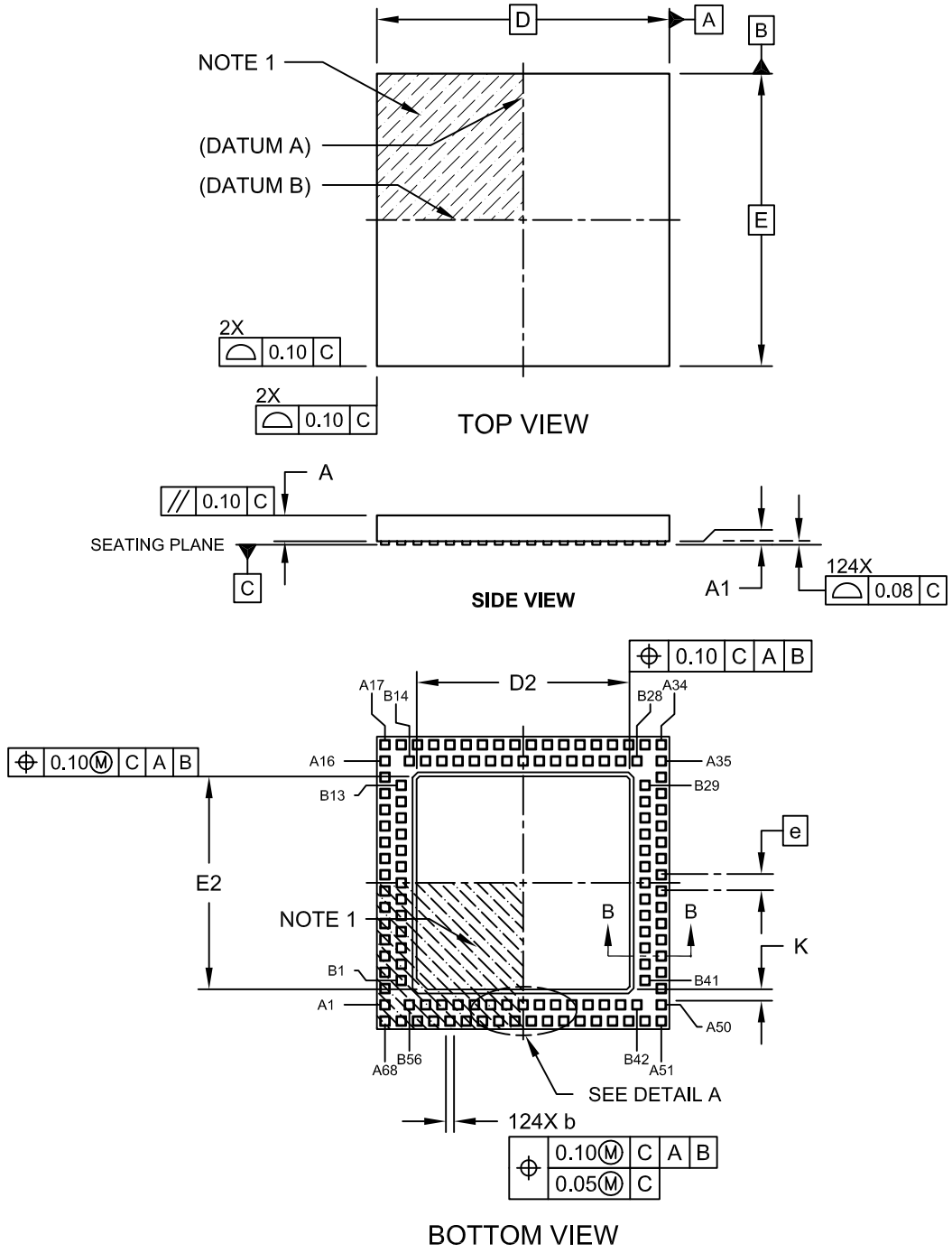
Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are characterized but are not tested.

2: This parameter is characterized, but not tested in manufacturing.

3: See parameter OS50 for PLL input frequency limitations.

124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

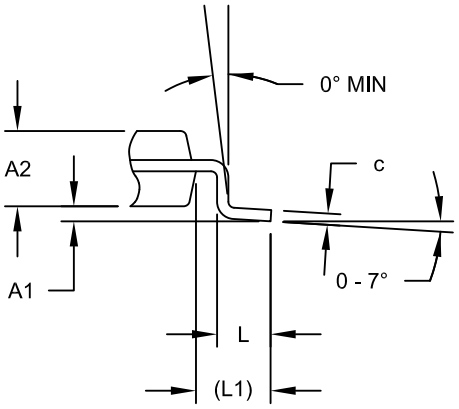
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

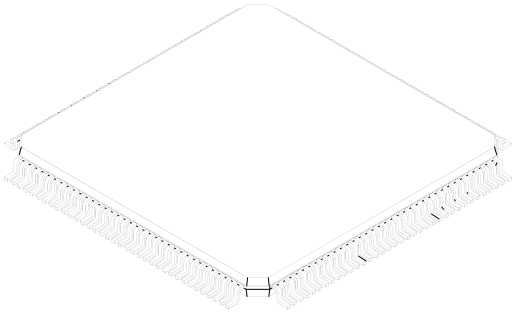


Microchip Technology Drawing C04-193A Sheet 1 of 2

144-Lead Plastic Thin Quad Flatpack (PH) - 16x16x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		144	
Lead Pitch	e		0.40 BSC	
Overall Height	A	-	-	1.20
Molded PackageThickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Overall Width	D		18.00 BSC	
Overall Length	E		18.00 BSC	
Molded Body Width	D1		16.00 BSC	
Molded Body Length	E1		16.00 BSC	
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.13	-	0.23

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

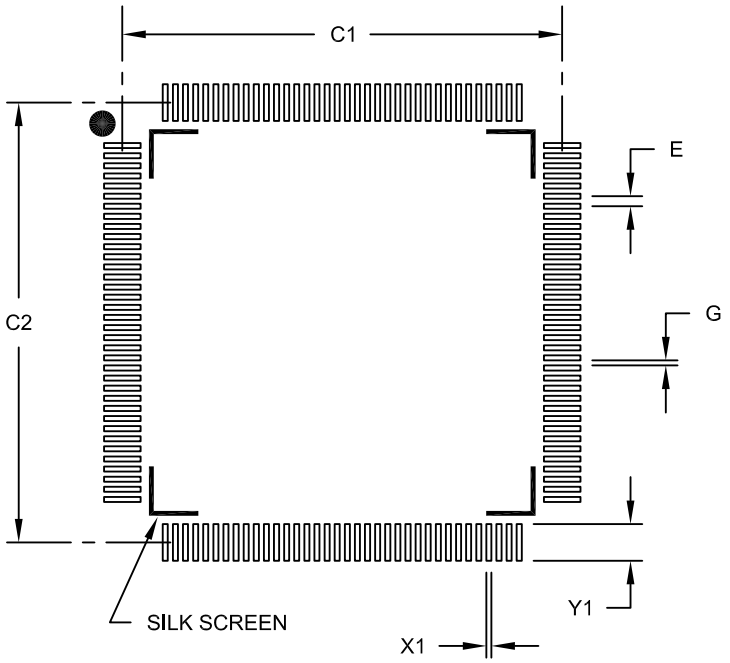
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-155B Sheet 2 of 2

144-Lead Plastic Thin Quad Flat Pack (PH) - 16x16 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		17.40	
Contact Pad Spacing	C2		17.40	
Contact Pad Width (X144)	X1			0.20
Contact Pad Length (X144)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2155B