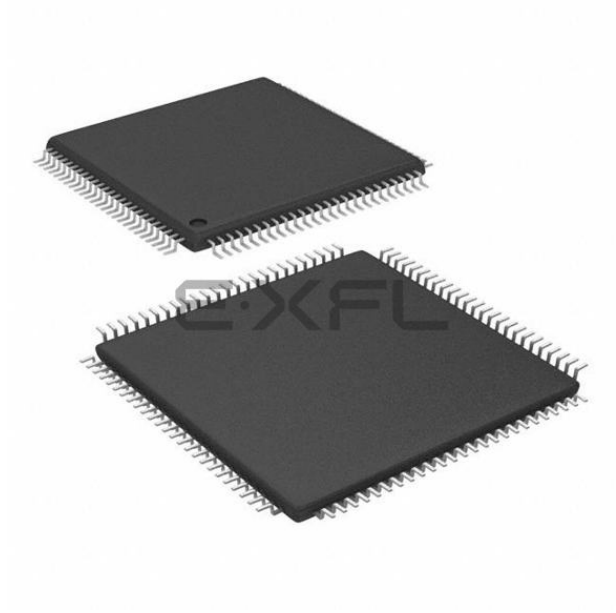
Microchip Technology - PIC32MZ0512EFF100T-I/PF Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512eff100t-i-pf

TABLE 4-2: BOOT FLASH 1 SEQUENCE AND CONFIGURATION WORDS SUMMARY

Virtual Address (BFC4_#)	Register Name	Bit Range	Bits															All Reset
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FF40	ABF1DEVCFG3	31:0	**Note:** See Table 34-2 for the bit descriptions.																xxxx
FF44	ABF1DEVCFG2	31:0																	xxxx
FF48	ABF1DEVCFG1	31:0																	xxxx
FF4C	ABF1DEVCFG0	31:0																	xxxx
FF50	ABF1DEVCP3	31:0																	xxxx
FF54	ABF1DEVCP2	31:0																	xxxx
FF58	ABF1DEVCP1	31:0																	xxxx
FF5C	ABF1DEVCP0	31:0																	xxxx
FF60	ABF1DEVSIGN3	31:0																	xxxx
FF64	ABF1DEVSIGN2	31:0																	xxxx
FF68	ABF1DEVSIGN1	31:0																	xxxx
FF6C	ABF1DEVSIGN0	31:0																	xxxx
FFC0	BF1DEVCFG3	31:0	**Note:** See Table 34-1 for the bit descriptions.																xxxx
FFC4	BF1DEVCFG2	31:0																	xxxx
FFC8	BF1DEVCFG1	31:0																	xxxx
FFCC	BF1DEVCFG0	31:0																	xxxx
FFD0	BF1DEVCP3	31:0																	xxxx
FFD4	BF1DEVCP2	31:0																	xxxx
FFD8	BF1DEVCP1	31:0																	xxxx
FFDC	BF1DEVCP0	31:0																	xxxx
FFE0	BF1DEVSIGN3	31:0																	xxxx
FFE4	BF1DEVSIGN2	31:0																	xxxx
FFE8	BF1DEVSIGN1	31:0																	xxxx
FFEC	BF1DEVSIGN0	31:0																	xxxx
FFF0	BF1SEQ3	31:16	CSEQ<15:0>																xxxx
		15:0	TSEQ<15:0>																xxxx
FFF4	BF1SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFF8	BF1SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFFC	BF1SEQ0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

TABLE 4-20: SYSTEM BUS TARGET 12 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B020	SBT12ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
B024	SBT12ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
B028	SBT12ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
B030	SBT12ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
B038	SBT12ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
B040	SBT12REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
B050	SBT12RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
B058	SBT12WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION (CONTINUED)

Interrupt Source[1]	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Data 19[2]	_ADC_DATA19_VECTOR	78	OFF078<17:1>	IFS2<14>	IEC2<14>	IPC19<20:18>	IPC19<17:16>	Yes
ADC Data 20[2]	_ADC_DATA20_VECTOR	79	OFF079<17:1>	IFS2<15>	IEC2<15>	IPC19<28:26>	IPC19<25:24>	Yes
ADC Data 21[2]	_ADC_DATA21_VECTOR	80	OFF080<17:1>	IFS2<16>	IEC2<16>	IPC20<4:2>	IPC20<1:0>	Yes
ADC Data 22[2]	_ADC_DATA22_VECTOR	81	OFF081<17:1>	IFS2<17>	IEC2<17>	IPC20<12:10>	IPC20<9:8>	Yes
ADC Data 23[2]	_ADC_DATA23_VECTOR	82	OFF082<17:1>	IFS2<18>	IEC2<18>	IPC20<20:18>	IPC20<17:16>	Yes
ADC Data 24[2]	_ADC_DATA24_VECTOR	83	OFF083<17:1>	IFS2<19>	IEC2<19>	IPC20<28:26>	IPC20<25:24>	Yes
ADC Data 25[2]	_ADC_DATA25_VECTOR	84	OFF084<17:1>	IFS2<20>	IEC2<20>	IPC21<4:2>	IPC21<1:0>	Yes
ADC Data 26[2]	_ADC_DATA26_VECTOR	85	OFF085<17:1>	IFS2<21>	IEC2<21>	IPC21<12:10>	IPC21<9:8>	Yes
ADC Data 27[2]	_ADC_DATA27_VECTOR	86	OFF086<17:1>	IFS2<22>	IEC2<22>	IPC21<20:18>	IPC21<17:16>	Yes
ADC Data 28[2]	_ADC_DATA28_VECTOR	87	OFF087<17:1>	IFS2<23>	IEC2<23>	IPC21<28:26>	IPC21<25:24>	Yes
ADC Data 29[2]	_ADC_DATA29_VECTOR	88	OFF088<17:1>	IFS2<24>	IEC2<24>	IPC22<4:2>	IPC22<1:0>	Yes
ADC Data 30[2]	_ADC_DATA30_VECTOR	89	OFF089<17:1>	IFS2<25>	IEC2<25>	IPC22<12:10>	IPC22<9:8>	Yes
ADC Data 31[2]	_ADC_DATA31_VECTOR	90	OFF090<17:1>	IFS2<26>	IEC2<26>	IPC22<20:18>	IPC22<17:16>	Yes
ADC Data 32[2]	_ADC_DATA32_VECTOR	91	OFF091<17:1>	IFS2<27>	IEC2<27>	IPC22<28:26>	IPC22<25:24>	Yes
ADC Data 33[2]	_ADC_DATA33_VECTOR	92	OFF092<17:1>	IFS2<28>	IEC2<28>	IPC23<4:2>	IPC23<1:0>	Yes
ADC Data 34[2]	_ADC_DATA34_VECTOR	93	OFF093<17:1>	IFS2<29>	IEC2<29>	IPC23<12:10>	IPC23<9:8>	Yes
ADC Data 35[2,3]	_ADC_DATA35_VECTOR	94	OFF094<17:1>	IFS2<30>	IEC2<30>	IPC23<20:18>	IPC23<17:16>	Yes
ADC Data 36[2,3]	_ADC_DATA36_VECTOR	95	OFF095<17:1>	IFS2<31>	IEC2<31>	IPC23<28:26>	IPC23<25:24>	Yes
ADC Data 37[2,3]	_ADC_DATA37_VECTOR	96	OFF096<17:1>	IFS3<0>	IEC3<0>	IPC24<4:2>	IPC24<1:0>	Yes
ADC Data 38[2,3]	_ADC_DATA38_VECTOR	97	OFF097<17:1>	IFS3<1>	IEC3<1>	IPC24<12:10>	IPC24<9:8>	Yes
ADC Data 39[2,3]	_ADC_DATA39_VECTOR	98	OFF098<17:1>	IFS3<2>	IEC3<2>	IPC24<20:18>	IPC24<17:16>	Yes
ADC Data 40[2,3]	_ADC_DATA40_VECTOR	99	OFF099<17:1>	IFS3<3>	IEC3<3>	IPC24<28:26>	IPC24<25:24>	Yes
ADC Data 41[2,3]	_ADC_DATA41_VECTOR	100	OFF100<17:1>	IFS3<4>	IEC3<4>	IPC25<4:2>	IPC25<1:0>	Yes
ADC Data 42[2,3]	_ADC_DATA42_VECTOR	101	OFF101<17:1>	IFS3<5>	IEC3<5>	IPC25<12:10>	IPC25<9:8>	Yes
ADC Data 43	_ADC_DATA43_VECTOR	102	OFF102<17:1>	IFS3<6>	IEC3<6>	IPC25<20:18>	IPC25<17:16>	Yes
ADC Data 44	_ADC_DATA44_VECTOR	103	OFF103<17:1>	IFS3<7>	IEC3<7>	IPC25<28:26>	IPC25<25:24>	Yes
Core Performance Counter Interrupt	_CORE_PERF_COUNT_VECTOR	104	OFF104<17:1>	IFS3<8>	IEC3<8>	IPC26<4:2>	IPC26<1:0>	No
Core Fast Debug Channel Interrupt	_CORE_FAST_DEBUG_CHAN_VECTOR	105	OFF105<17:1>	IFS3<9>	IEC3<9>	IPC26<12:10>	IPC26<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MZ EF Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

4: This interrupt source is not available on 124-pin devices.

REGISTER 7-5: IFSx: INTERRUPT FLAG STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS31	IFS30	IFS29	IFS28	IFS27	IFS26	IFS25	IFS24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS23	IFS22	IFS21	IFS20	IFS19	IFS18	IFS17	IFS16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10	IFS9	IFS8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS7	IFS6	IFS5	IFS4	IFS3	IFS2	IFS1	IFS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IFS31-IFS0:** Interrupt Flag Status bits
1 = Interrupt request has occurred
0 = No interrupt request has occurred

Note: This register represents a generic definition of the IFSx register. Refer to Table 7-2 for the exact bit definitions.

REGISTER 7-6: IECx: INTERRUPT ENABLE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC9	IEC8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC7	IEC6	IEC5	IEC4	IEC3	IEC2	IEC1	IEC0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IEC31-IEC0:** Interrupt Enable bits
1 = Interrupt is enabled
0 = Interrupt is disabled

Note: This register represents a generic definition of the IECx register. Refer to Table 7-2 for the exact bit definitions.

REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)

bit 26 **DATATWEN:** Data Toggle Write Enable Control bit (*Host mode*)
1 = DATATGGL can be written
0 = DATATGGL is not writable

bit 25 **DATATGGL:** Data Toggle bit (*Host mode*)
When read, this bit indicates the current state of the endpoint data toggle.
If DATATWEN = 1, this bit may be written with the required setting of the data toggle.
If DATATWEN = 0, any value written to this bit is ignored.

bit 24 **INCOMPRX:** Incomplete Packet Status bit
1 = The packet in the RX FIFO during a high-bandwidth Isochronous/Interrupt transfer is incomplete because parts of the data were not received
0 = Written by then software to clear this bit
In anything other than Isochronous transfer, this bit will always return 0.

bit 23 **CLRDT:** Clear Data Toggle Control bit
1 = Reset the endpoint data toggle to 0
0 = Leave endpoint data toggle alone

bit 22 **SENTSTALL:** STALL Handshake Status bit (*Device mode*)
1 = STALL handshake is transmitted
0 = Written by the software to clear this bit

RXSTALL: STALL Handshake Receive Status bit (*Host mode*)
1 = A STALL handshake has been received. An interrupt is generated.
0 = Written by the software to clear this bit

bit 21 **SENDSTALL:** STALL Handshake Control bit (*Device mode*)
1 = Issue a STALL handshake
0 = Terminate stall condition

REQPKT: IN Transaction Request Control bit (*Host mode*)
1 = Request an IN transaction.
0 = No request
This bit is cleared when RXPKTRDY is set.

bit 20 **FLUSH:** Flush FIFO Control bit
1 = Flush the next packet to be read from the endpoint RX FIFO. The FIFO pointer is reset and the RXPKTRDY bit is cleared. This should only be used when RXPKTRDY is set. If the FIFO is double-buffered, FLUSH may need to be set twice to completely clear the FIFO.
0 = Normal FIFO operation
This bit is automatically cleared.

bit 19 **DATAERR:** Data Packet Error Status bit (*Device mode*)
1 = The data packet has a CRC or bit-stuff error.
0 = No data error
This bit is cleared when RXPKTRDY is cleared. This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.

DERRNAKT: Data Error/NAK Time-out Status bit (*Host mode*)
1 = The data packet has a CRC or bit-stuff error. In Bulk mode, the RX endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK limit.
0 = No data or NAK time-out error

12.2 Registers for Slew Rate Control

Some I/O pins can be configured for various types of slew rate control on its associated port. This is controlled by the Slew Rate Control bits in the SRCON1x and SRCON0x registers that are associated with each I/O port. The slew rate control is configured using the corresponding bit in each register, as shown in Table 12-1.

As an example, writing 0x0001, 0x0000 to SRCON1A and SRCON0A, respectively, will enable slew rate control on the RA0 pin and sets the slew rate to the slow edge rate.

TABLE 12-1: SLEW RATE CONTROL BIT SETTINGS

SRCON1x	SRCON0x	Description
1	1	Slew rate control is enabled and is set to the slowest edge rate.
1	0	Slew rate control is enabled and is set to the slow edge rate.
0	1	Slew rate control is enabled and is set to the medium edge rate.
0	0	Slew rate control is disabled and is set to the fastest edge rate.

Note: By default, all of the Port pins are set to the fastest edge rate.

12.3 CLR, SET, and INV Registers

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.

12.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

PPS configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

12.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation "RPn" in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable port number.

12.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital-only peripherals. These include general serial communications (UART, SPI, and CAN), general purpose timer clock inputs, timer-related peripherals (input capture and output compare), interrupt-on-change inputs, and reference clocks (input and output).

In comparison, some digital-only peripheral modules are never included in the PPS feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

TABLE 12-22: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1444	IC4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC4R<3:0>				0000
1448	IC5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC5R<3:0>				0000
144C	IC6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC6R<3:0>				0000
1450	IC7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC7R<3:0>				0000
1454	IC8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC8R<3:0>				0000
1458	IC9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC9R<3:0>				0000
1460	OCFAR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	OCFAR<3:0>				0000
1468	U1RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U1RXR<3:0>				0000
146C	U1CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U1CTSR<3:0>				0000
1470	U2RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U2RXR<3:0>				0000
1474	U2CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U2CTSR<3:0>				0000
1478	U3RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U3RXR<3:0>				0000
147C	U3CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U3CTSR<3:0>				0000
1480	U4RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U4RXR<3:0>				0000
1484	U4CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U4CTSR<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

2: This register is not available on devices without a CAN module.

15.1 Deadman Timer Control Registers

TABLE 15-1: DEADMAN TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0A00	DMTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	x000
0A10	DMTPRECLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STEP1<7:0>								—	—	—	—	—	—	—	—	0000
0A20	DMTCLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STEP2<7:0>								0000
0A30	DMTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN	0000
0A40	DMTCNT	31:16	COUNTER<31:0>																0000
		15:0																	0000
0A60	DMTPSCNT	31:16	PSCNT<31:0>																0000
		15:0																	00xx
0A70	DMTPSINTV	31:16	PSINTV<31:0>																0000
		15:0																	000x

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

16.0 WATCHDOG TIMER (WDT)

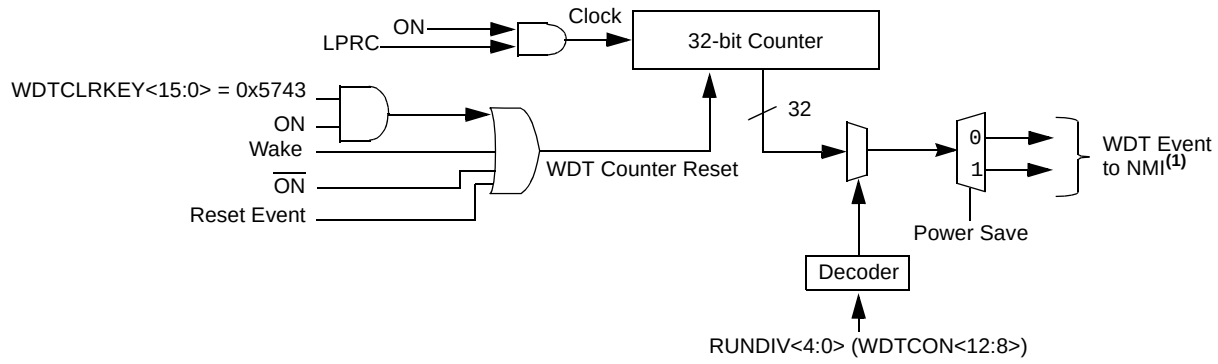
Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

When enabled, the Watchdog Timer (WDT) operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are key features of the WDT module:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle

FIGURE 16-1: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: Refer to **6.0 "Resets"** for more information.

REGISTER 21-2: I2CxSTAT: I^{2}C STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0, HS, HC	R-0, HS, HC	R/C-0, HS, HC	U-0	U-0	R/C-0, HS	R-0, HS, HC	R-0, HS, HC
	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10
7:0	R/C-0, HS, SC	R/C-0, HS, SC	R-0, HS, HC	R/C-0, HS, HC	R/C-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF

Legend:	HS = Hardware Set	HC = Hardware Cleared	SC = Software Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	C = Clearable bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I^{2}C master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware set or clear at end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I^{2}C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

bit 13 **ACKTIM:** Acknowledge Time Status bit (Valid in I^{2}C Slave mode only)
1 = I^{2}C bus is in an Acknowledge sequence, set on the eight falling edge of SCL clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCL clock

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware set at detection of bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 **ADD10:** 10-bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I^{2}C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

26.1 Crypto Engine Control Registers

TABLE 26-2: CRYPTO ENGINE REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5000	CEVER	31:16	REVISION<7:0>								VERSION<7:0>								0000
		15:0	ID<15:0>																0000
5004	CECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	SWAPOEN	SWRST	SWAPEN	—	—	BDPCHST	BDPPLEN	DMAEN	0000
5008	CEBDADDR	31:16	BDPADDR<31:0>																0000
		15:0																	0000
500C	CEBDPADDR	31:16	BASEADDR<31:0>																0000
		15:0																	0000
5010	CESTAT	31:16	ERRMODE<2:0>			ERROP<2:0>			ERRPHASE<1:0>		—	—	BDSTATE<3:0>				START	ACTIVE	0000
		15:0	BDCTRL<15:0>																0000
5014	CEINTSRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIF	PKTIF	CBDIF	PENDIF	0000
5018	CEINTEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIE	PKTIE	CBDIE	PENDIE	0000
501C	CEPOLLCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BDPPLCON<15:0>																0000
5020	CEHDLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	HDRLEN<7:0>								0000
5024	CETRLLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRLRLEN<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 28-5: ADCIMCON1: ADC INPUT MODE CONTROL REGISTER 1 (CONTINUED)

bit 20 **SIGN10:** AN10 Signed Data Mode bit
1 = AN10 is using Signed Data mode
0 = AN10 is using Unsigned Data mode

bit 19 **DIFF9:** AN9 Mode bit
1 = AN9 is using Differential mode
0 = AN9 is using Single-ended mode

bit 18 **SIGN9:** AN9 Signed Data Mode bit
1 = AN9 is using Signed Data mode
0 = AN9 is using Unsigned Data mode

bit 17 **DIFF8:** AN 8 Mode bit
1 = AN8 is using Differential mode
0 = AN8 is using Single-ended mode

bit 16 **SIGN8:** AN8 Signed Data Mode bit
1 = AN8 is using Signed Data mode
0 = AN8 is using Unsigned Data mode

bit 15 **DIFF7:** AN7 Mode bit
1 = AN7 is using Differential mode
0 = AN7 is using Single-ended mode

bit 14 **SIGN7:** AN7 Signed Data Mode bit
1 = AN7 is using Signed Data mode
0 = AN7 is using Unsigned Data mode

bit 13 **DIFF6:** AN6 Mode bit
1 = AN6 is using Differential mode
0 = AN6 is using Single-ended mode

bit 12 **SIGN6:** AN6 Signed Data Mode bit
1 = AN6 is using Signed Data mode
0 = AN6 is using Unsigned Data mode

bit 11 **DIFF5:** AN5 Mode bit
1 = AN5 is using Differential mode
0 = AN5 is using Single-ended mode

bit 10 **SIGN5:** AN5 Signed Data Mode bit
1 = AN5 is using Signed Data mode
0 = AN5 is using Unsigned Data mode

bit 9 **DIFF4:** AN4 Mode bit
1 = AN4 is using Differential mode
0 = AN4 is using Single-ended mode

bit 8 **SIGN4:** AN4 Signed Data Mode bit
1 = AN4 is using Signed Data mode
0 = AN4 is using Unsigned Data mode

bit 7 **DIFF3:** AN3 Mode bit
1 = AN3 is using Differential mode
0 = AN3 is using Single-ended mode

bit 6 **SIGN3:** AN3 Signed Data Mode bit
1 = AN3 is using Signed Data mode
0 = AN3 is using Unsigned Data mode

bit 5 **DIFF2:** AN2 Mode bit
1 = AN2 is using Differential mode
0 = AN2 is using Single-ended mode

REGISTER 28-10: ADCCSS1: ADC COMMON SCAN SELECT REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS31(1)	CSS30(1)	CSS29(1)	CSS28(1)	CSS27(1)	CSS26(1)	CSS25(1)	CSS24(1)
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS23(1)	CSS22(1)	CSS21(1)	CSS20(1)	CSS19(1)	CSS18	CSS17	CSS16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CSS31:CSS0:** Analog Common Scan Select bits(2,3)
1 = Select AN*x* for input scan
0 = Skip AN*x* for input scan

Note 1: This bit is not available on 64-pin devices.

2: In addition to setting the appropriate bits in this register, Class 1 and Class 2 analog inputs must select the STRIG input as the trigger source if they are to be scanned through the CSS*x* bits. Refer to the bit descriptions in the ADCTRGx registers for selecting the STRIG option.

3: If a Class 1 or Class 2 input is included in the scan by setting the CSSx bit to '1' and by setting the TRGSRCx<4:0> bits to STRIG mode (`'0b11`), the user application must ensure that no other triggers are generated for that input using the RQCNVRT bit in the ADCCON3 register or the hardware input or any digital filter. Otherwise, the scan behavior is unpredictable.

REGISTER 30-31: EMAC1MCFG: ETHERNET CONTROLLER MAC MII MANAGEMENT CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	RESETMGMT	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CLKSEL<3:0>(1)				NOPRE	SCANINC

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **RESETMGMT:** Test Reset MII Management bit
1 = Reset the MII Management module
0 = Normal Operation

bit 14-6 **Unimplemented:** Read as '0'

bit 5-2 **CLKSEL<3:0>:** MII Management Clock Select 1 bits(1)
These bits are used by the clock divide logic in creating the MII Management Clock (MDC), which the IEEE 802.3 Specification defines to be no faster than 2.5 MHz. Some PHYs support clock rates up to 12.5 MHz.

bit 1 **NOPRE:** Suppress Preamble bit
1 = The MII Management will perform read/write cycles without the 32-bit preamble field. Some PHYs support suppressed preamble
0 = Normal read/write cycles are performed

bit 0 **SCANINC:** Scan Increment bit
1 = The MII Management module will perform read cycles across a range of PHYs. The read cycles will start from address 1 through the value set in EMAC1MADR<PHYADDR>
0 = Continuous reads of the same PHY

Note 1: Table 30-7 provides a description of the clock divider encoding.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

TABLE 30-7: MIIM CLOCK SELECTION

MIIM Clock Select	EMAC1MCFG<5:2>
TPBCLK5 divided by 4	000x
TPBCLK5 divided by 6	0010
TPBCLK5 divided by 8	0011
TPBCLK5 divided by 10	0100
TPBCLK5 divided by 14	0101
TPBCLK5 divided by 20	0110
TPBCLK5 divided by 28	0111
TPBCLK5 divided by 40	1000
TPBCLK5 divided by 48	1001
TPBCLK5 divided by 50	1010
Undefined	Any other combination

31.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

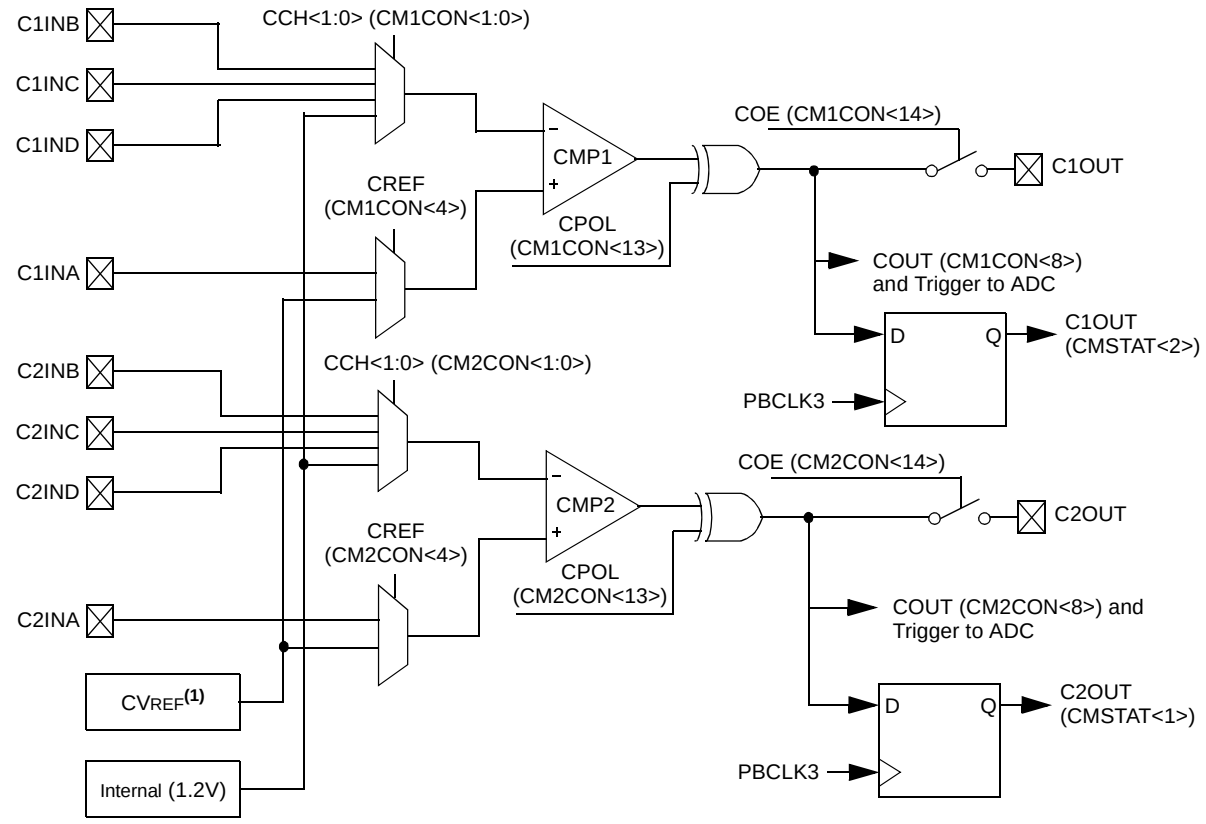
The Analog Comparator module consists of two comparators that can be configured in a variety of ways.

The following are key features of the Analog Comparator module:

- Differential inputs
- Rail-to-rail operation
- Selectable output polarity
- Selectable inputs:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference
  - Comparator voltage reference (CVREF)
- Selectable interrupt generation

A block diagram of the comparator module is illustrated in Figure 31-1.

FIGURE 31-1: COMPARATOR BLOCK DIAGRAM



Note 1: Internally connected. See **Section 32.0 "Comparator Voltage Reference (CVREF)"** for more information.

REGISTER 34-7: CFGCON: CONFIGURATION CONTROL REGISTER (CONTINUED)

bit 7 **IOANCPEN:** I/O Analog Charge Pump Enable bit
The analog IO charge pump improves analog performance when the device is operating at lower voltages. However, the charge pumps consume additional current.
1 = Charge pump is enabled
0 = Charge pump is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **ECCCON<1:0>:** Flash ECC Configuration bits
11 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are writable)
10 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are locked)
01 = Dynamic Flash ECC is enabled (ECCCON<1:0> bits are locked)
00 = Flash ECC is enabled (ECCCON<1:0> bits are locked; disables word Flash writes)

bit 3 **JTAGEN:** JTAG Port Enable bit
1 = Enable the JTAG port
0 = Disable the JTAG port

bit 2 **TROEN:** Trace Output Enable bit
1 = Enable trace outputs and start trace clock (trace probe must be present)
0 = Disable trace outputs and stop trace clock

bit 1 **Unimplemented:** Read as '0'

bit 0 **TDOEN:** TDO Enable for 2-Wire JTAG
1 = 2-wire JTAG protocol uses TDO
0 = 2-wire JTAG protocol does not use TDO

Note 1: To change this bit, the unlock sequence must be performed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

36.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

36.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

TABLE 37-39: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS(2)			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period	20	—	6250	ns	—
Throughput Rate							
AD51	FTP	Sample Rate for ADC0-ADC4 (Class 1 Inputs)	— — — —	— — — —	3.125 3.57 4.16 5	Msps Msps Msps Msps	12-bit resolution Source Impedance ≤ 200Ω 10-bit resolution Source Impedance ≤ 200Ω 8-bit resolution Source Impedance ≤ 200Ω 6-bit resolution Source Impedance ≤ 200Ω
		Sample Rate for ADC7 (Class 2 and Class 3 Inputs)	— — — —	— — — —	2.94 3.33 3.84 4.55	Msps Msps Msps Msps	12-bit resolution Source Impedance ≤ 200Ω 10-bit resolution Source Impedance ≤ 200Ω 8-bit resolution Source Impedance ≤ 200Ω 6-bit resolution Source Impedance ≤ 200Ω
Timing Parameters							
AD60	TSAMP	Sample Time for ADC0-ADC4 (Class 1 Inputs)	3 4 5 13	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
		Sample Time for ADC7 (Class 2 and 3 Inputs)	4 5 6 14	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
		Sample Time for ADC7 (Class 2 and 3 Inputs)	See Table 37-40	—	—	TAD	CVDEN (ADCCON1<11>) = 1
AD62	TCONV	Conversion Time (after sample time is complete)	— — — —	— — — —	13 11 9 7	TAD	12-bit resolution 10-bit resolution 8-bit resolution 6-bit resolution
AD65	TWAKE	Wake-up time from Low-Power Mode	— —	500 20	— —	TAD µs	Lesser of 500 TAD or 20 µs.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

39.1 DC Characteristics

TABLE 39-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts) (Note 1)	Temp. Range (in °C)	Max. Frequency	Comment
			PIC32MZ EF Devices	
MDC5	2.1V-3.6V	-40°C to +85°C	252 MHz	—

Note 1: Overall functional device operation at $V_{BORMIN} < V_{DD} < V_{DDMIN}$ is guaranteed, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below V_{DDMIN}. Refer to parameter BO10 in Table 37-5 for BOR values.

TABLE 39-2: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial	
Parameter No.	**Typical(3)**	**Maximum(6)**	**Units**	**Conditions**
Operating Current (IDD)(1)				
MDC27a	156	170	mA	252 MHz **(Note 2)**
MDC27b	115	135	mA	252 MHz **(Note 4,5)**

Note 1: A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

2: The test conditions for IDD measurements are as follows:

- Oscillator mode is EC+PLL with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBMD = 1), VUSB3V3 is connected to VSS
- CPU, Program Flash, and SRAM data memory are operational, Program Flash memory Wait states are equal to four
- L1 Cache and Prefetch modules are enabled
- No peripheral modules are operating, (ON bit = 0), and the associated PMD bit is set. All clocks are disabled ON bit (PBxDIV<15>) = 0 (x ≠ 1,7)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled

3: Data in "Typical" column is at 3.3V, +25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

4: This parameter is characterized, but not tested in manufacturing.

5: Note 2 applies with the following exceptions: L1 Cache and Prefetch modules are disabled, Program Flash memory Wait states are equal to seven.

6: Data in the "Maximum" column is at 3.3V, +85ºC at specified operating frequency, unless otherwise stated. Parameters are for design guidance only and are not tested.

A.9 Other Peripherals and Features

Most of the remaining peripherals on PIC32MZ EF devices act identical to their counterparts on PIC32MX-5XX/6XX/7XX devices. The main differences have to do with handling the increased peripheral bus clock speed and additional clock sources.

Table A-10 lists the differences (indicated by **Bold** type) that will affect software and hardware migration.

TABLE A-10: PERIPHERAL DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
I^2C	
On PIC32MX devices, all pins are 5V-tolerant.	On PIC32MZ EF devices, the I2C4 port uses non-5V tolerant pins, and will have different VOL/VOH specifications.
I2CxBRG<**11**:0>	The Baud Rate Generator register has been expanded from 12 bits to 16 bits. I2CxBRG<**15**:0>
Watchdog Timer	
Clearing the Watchdog Timer on PIC32MX5XX/6XX/7XX devices required writing a '1' to the WDTCLR bit. **WDTCLR** (WDTCON<**0**>)	On PIC32MZ EF devices, the WDTCLR bit has been replaced with the 16-bit WDTCLRKEY, which must be written with a specific value (0x5743) to clear the Watchdog Timer. In addition, the WDTSPGM (DEVCFG1<21>) bit is used to control operation of the Watchdog Timer during Flash programming. **WDTCLRKEY<15:0>** (WDTCON<**31:16**>)
RTCC	
On PIC32MX devices, the output of the RTCC pin was selected between the Seconds Clock or the Alarm Pulse. RTCSECSEL (RTCCON<7>) 1 = RTCC Seconds Clock is selected for the RTCC pin 0 = RTCC Alarm Pulse is selected for the RTCC pin	On PIC32MZ EF devices, the RTCC Clock is added as an option. RTCSECSEL has been renamed RTCOUTSEL and expanded to two bits. **RTCOUTSEL<1:0>** (RTCCON<**8:**7>) **11 = Reserved** **10 = RTCC Clock is presented on the RTCC pin** 01 = Seconds Clock is presented on the RTCC pin 00 = Alarm Pulse is presented on the RTCC pin when the alarm interrupt is triggered
On PIC32MX devices, the Secondary Oscillator (SOSC) serves as the input clock for the RTCC module.	On PIC32MZ EF devices, an additional clock source, LPRC, is available as a choice for the input clock. **RTCCLKSEL<1:0> (RTCCON<10:9>)** **11 = Reserved** **10 = Reserved** **01 = RTCC uses the external 32.768 kHz SOSC** **00 = RTCC uses the internal 32 kHz oscillator (LPRC)**