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What is "[Embedded - Microcontrollers](#)"?

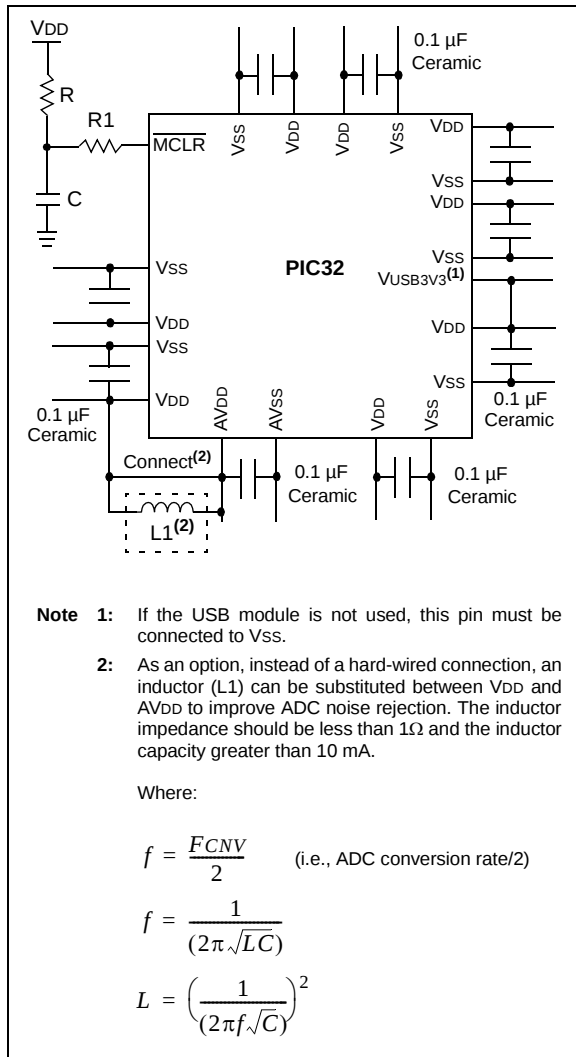
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	97
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512eff124-e-tl

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

2.3 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

- Device Reset
- Device programming and debugging

Pulling The MCLR pin low generates either a device Reset or a POR, depending on the setting of the SMCLR bit (DEVCFG0<15>). Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS

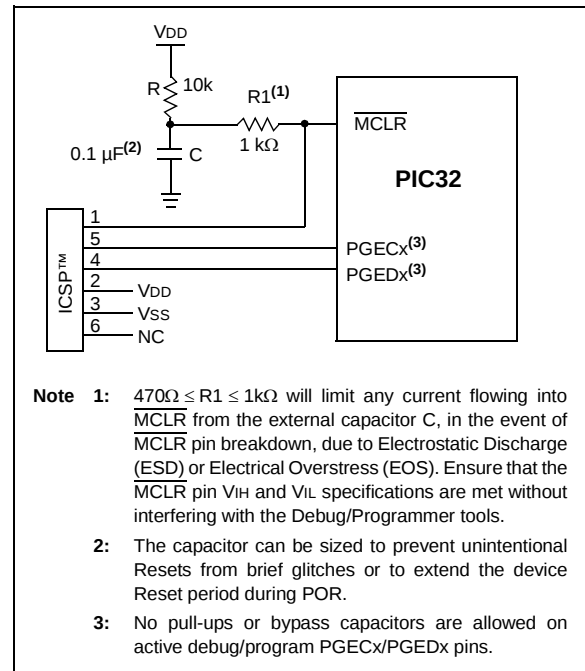


TABLE 4-20: SYSTEM BUS TARGET 12 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
B020	SBT12ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>			0000
B024	SBT12ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
B028	SBT12ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
B030	SBT12ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
B038	SBT12ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
B040	SBT12REG0	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—
B050	SBT12RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
B058	SBT12WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

6.0 RESETS

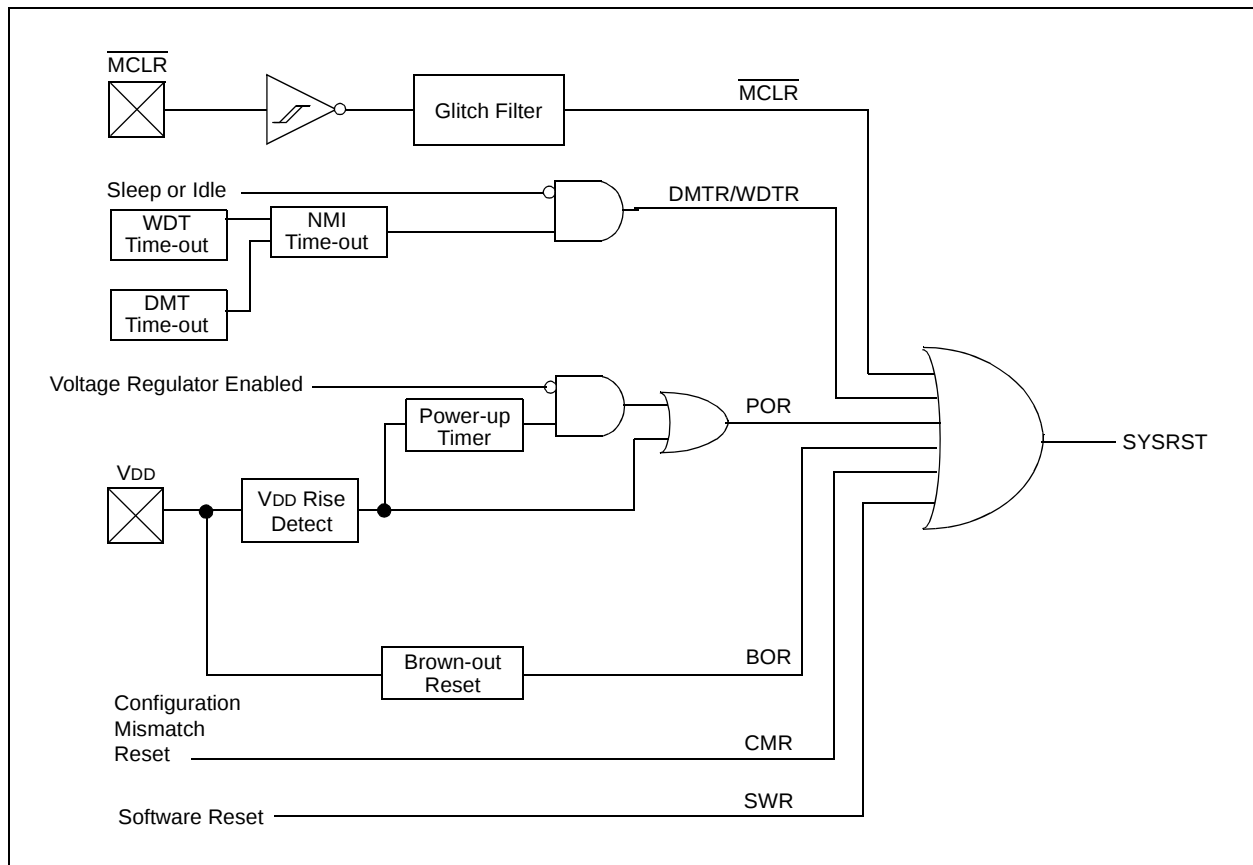
Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. “Resets”** (DS60001118) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Master Clear Reset pin ($\overline{\text{MCLR}}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)
- Deadman Timer Reset (DMTR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM



NOTES:

REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)

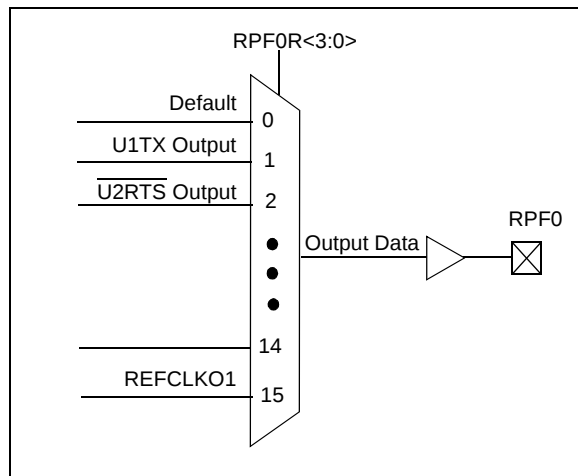
- bit 18 **OVERRUN:** Data Overrun Status bit (*Device mode*)
1 = An OUT packet cannot be loaded into the RX FIFO.
0 = Written by software to clear this bit
This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.
- ERROR:** No Data Packet Received Status bit (*Host mode*)
1 = Three attempts have been made to receive a packet and no data packet has been received. An interrupt is generated.
0 = Written by the software to clear this bit.
This bit is only valid when the RX endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns zero.
- bit 17 **FIFOFULL:** FIFO Full Status bit
1 = No more packets can be loaded into the RX FIFO
0 = The RX FIFO has at least one free space
- bit 16 **RXPKT RDY:** Data Packet Reception Status bit
1 = A data packet has been received. An interrupt is generated.
0 = Written by software to clear this bit when the packet has been unloaded from the RX FIFO.
- bit 15-11 **MULT<4:0>:** Multiplier Control bits
For Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints, multiplies TXMAXP by MULT+1 for the payload size.
For Bulk endpoints, MULT can be up to 32 and defines the number of “USB” packets of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. The data packet is required to be an exact multiple of the payload specified by TXMAXP.
For Isochronous/Interrupts endpoints operating in Hi-Speed mode, MULT may be either 2 or 3 and specifies the maximum number of such transactions that can take place in a single microframe.
- bit 10-0 **RXMAXP<10:0>:** Maximum RX Payload Per Transaction Control bits
This field sets the maximum payload (in bytes) transmitted in a single transaction. The value is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-Speed and Hi-Speed operations.
RXMAXP must be set to an even number of bytes for proper interrupt generation in DMA Mode 1.

12.4.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the PPS options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPNR registers (Register 12-2) are used to control output mapping. Like the [pin name]R registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 12-3 and Figure 12-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 12-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPF0



12.4.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32MZ EF devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

12.4.6.1 Control Register Lock

Under normal operation, writes to the RPNR and [pin name]R registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK Configuration bit (CFGCON<13>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** in the "PIC32 Family Reference Manual" for details.

12.4.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPNR and [pin name]R registers. The IOL1WAY Configuration bit (DEVCFG3<29>) blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.

TABLE 12-11: PORTE REGISTER MAP FOR 100-PIN, 124-PIN, AND 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0400	ANSELE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSE9	ANSE8	ANSE7	ANSE6	ANSE5	ANSE4	—	—	—	—	03F0
0410	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISE9	TRISE8	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	03FF
0420	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
0430	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATE9	LATE8	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
0440	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCE9	ODCE8	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000
0450	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUE9	CNPUE8	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPUE3	CNPUE2	CNPUE1	CNPUE0	0000
0460	CNPDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDE9	CNPDE8	CNPDE7	CNPDE6	CNPDE5	CNPDE4	CNPDE3	CNPDE2	CNPDE1	CNPDE0	0000
0470	CNCONE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0480	CNENE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNENE9	CNENE8	CNENE7	CNENE6	CNENE5	CNENE4	CNENE3	CNENE2	CNENE1	CNENE0	0000
0490	CNSTATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CN STATE9	CN STATE8	CN STATE7	CN STATE6	CN STATE5	CN STATE4	CN STATE3	CN STATE2	CN STATE1	CN STATE0	0000
04A0	CNNEE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNNEE9	CNNEE8	CNNEE7	CNNEE6	CNNEE5	CNNEE4	CNNEE3	CNNEE2	CNNEE1	CNNEE0	0000
04B0	CNFE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNFE9	CNFE8	CNFE7	CNFE6	CNFE5	CNFE4	CNFE3	CNFE2	CNFE1	CNFE0	0000
04C0	SRCONOE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR0E3	SR0E2	SR0E1	SR0E0	0000
04D0	SRCON1E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR1E3	SR1E2	SR1E1	SR1E0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

TABLE 12-16: PORTG REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	ANSELG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSG9	ANSG8	ANSG7	ANSG6	—	—	—	—	—	—	03C0
0610	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	—	—	03C0
0620	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RG9	RG8	RG7	RG6	—	—	—	—	—	—	xxxx
0630	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	—	—	xxxx
0640	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	—	—	0000
0650	CNPUG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	—	—	0000
0660	CNPDG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	—	—	0000
0670	CNCONG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0680	CNENG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNENG9	CNENG8	CNENG7	CNENG6	—	—	—	—	—	—	0000
0690	CNSTATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CN STATG9	CN STATG8	CN STATG7	CN STATG6	—	—	—	—	—	—	0000
06A0	CNNEG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNNEG9	CNNEG8	CNNEG7	CNNEG6	—	—	—	—	—	—	0000
06B0	CNFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNFG9	CNFG8	CNFG7	CNFG6	—	—	—	—	—	—	0000
06C0	SRCON0G	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	SR0G9	—	—	SR0G6	—	—	—	—	—	—	0000
06D0	SRCON1G	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	SR1G9	—	—	SR1G6	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 12-3: CNCONx: CHANGE NOTICE CONTROL FOR PORTx REGISTER (x = A – K)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	ON	—	—	—	EDGEDETECT	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notice (CN) Control ON bit

1 = CN is enabled

0 = CN is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **EDGEDETECT:** Change Notification Style bit

1 = Edge Style. Detect edge transitions (CNF_x used for CN Event).

0 = Mismatch Style. Detect change from last PORT_x read (CNSTAT_x used for CN Event).

bit 10-0 **Unimplemented:** Read as '0'

REGISTER 20-6: SQI1CMDTHR: SQI COMMAND THRESHOLD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TXCMDTHR<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RXCMDTHR<4:0> ⁽¹⁾				

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **TXCMDTHR<4:0>:** Transmit Command Threshold bits

In transmit initiation mode, the SQI module performs a transmit operation when transmit command threshold bytes are present in the TX FIFO. These bits should usually be set to '1' for normal Flash commands, and set to a higher value for page programming. For 16-bit mode, the value should be a multiple of 2.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RXCMDTHR<4:0>:** Receive Command Threshold bits⁽¹⁾

In receive initiation mode, the SQI module attempts to perform receive operations to fetch the receive command threshold number of bytes in the receive buffer. If space for these bytes is not present in the FIFO, the SQI will not initiate a transfer. For 16-bit mode, the value should be a multiple of 2.

If software performs any reads, thereby reducing the FIFO count, hardware would initiate a receive transfer to make the FIFO count equal to the value in these bits. If software would not like any more words latched into the FIFO, command initiation mode needs to be changed to Idle before any FIFO reads by software.

In the case of Boot/XIP mode, the SQI module will use the System Bus burst size, instead of the receive command threshold value.

Note 1: These bits should only be programmed when a receive is not active (i.e., during Idle mode or a transmit).

REGISTER 28-2: ADCCON2: ADC CONTROL REGISTER 2 (CONTINUED)

- bit 14 **REFFLTEN:** Band Gap/VREF Voltage Fault Interrupt Enable bit
1 = Interrupt will be generated when the REFFLT bit is set
0 = No interrupt is generated when the REFFLT bit is set
- bit 13 **EOSIEN:** End of Scan Interrupt Enable bit
1 = Interrupt will be generated when EOSRDY bit is set
0 = No interrupt is generated when the EOSRDY bit is set
- bit 12 **ADCEIOVR:** Early Interrupt Request Override bit
1 = Early interrupt generation is not overridden and interrupt generation is controlled by the ADCEIEN1 and ADCEIEN2 registers
0 = Early interrupt generation is overridden and interrupt generation is controlled by the ADCGIRQEN1 and ADCGIRQEN2 registers
- bit 11 **Unimplemented:** Read as '0'
- bit 10-8 **ADCEIS<2:0>:** Shared ADC (ADC7) Early Interrupt Select bits
These bits select the number of clocks (TAD7) prior to the arrival of valid data that the associated interrupt is generated.
111 = The data ready interrupt is generated 8 ADC clocks prior to end of conversion
110 = The data ready interrupt is generated 7 ADC clocks prior to end of conversion
.
.
.
001 = The data ready interrupt is generated 2 ADC module clocks prior to end of conversion
000 = The data ready interrupt is generated 1 ADC module clock prior to end of conversion

Note: All options are available when the selected resolution, set by the SELRES<1:0> bits (ADCCON1<22:21>), is 12-bit or 10-bit. For a selected resolution of 8-bit, options from '000' to '101' are valid. For a selected resolution of 6-bit, options from '000' to '011' are valid.
- bit 7 **Unimplemented:** Read as '0'
- bit 6-0 **ADCDIV<6:0>:** Shared ADC (ADC7) Clock Divider bits
1111111 = 254 * TQ = TAD7
.
.
.
0000011 = 6 * TQ = TAD7
0000010 = 4 * TQ = TAD7
0000001 = 2 * TQ = TAD7
0000000 = Reserved

The ADCDIV<6:0> bits divide the ADC control clock (TQ) to generate the clock for the Shared ADC, ADC7 (TAD7).

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 28-18: ADCTRG2: ADC TRIGGER SOURCE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC7<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC6<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC5<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC4<4:0>				

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC7<4:0>:** Trigger Source for Conversion of Analog Input AN7 Select bits

11111 = Reserved

•
•
•

01101 = Reserved

01100 = Comparator 2 (COUT)

01011 = Comparator 1 (COUT)

01010 = OCMP5

01001 = OCMP3

01000 = OCMP1

00111 = TMR5 match

00110 = TMR3 match

00101 = TMR1 match

00100 = INT0 External interrupt

00011 = STRIG

00010 = Global level software trigger (GLSWTRG)

00001 = Global software edge Trigger (GSWTRG)

00000 = No Trigger

For STRIG, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSSx registers.

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TRGSRC6<4:0>:** Trigger Source for Conversion of Analog Input AN6 Select bits

See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC5<4:0>:** Trigger Source for Conversion of Analog Input AN5 Select bits

See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC4<4:0>:** Trigger Source for Conversion of Analog Input AN4 Select bits

See bits 28-24 for bit value definitions.

TABLE 34-3: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets ⁽¹⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	CFGCON	31:16	—	—	—	—	—	—	DMAPRI	CPUPRI	—	—	—	—	—	—	ICACLK	OCACLK	0000
		15:0	—	—	IOLOCK	PMDLOCK	PGLOCK	—	—	USBSEN	IOANCPEN	—	ECCCON<1:0>		JTAGEN	TROEN	—	TDOEN	000B
0020	DEVID	31:16	VER<3:0>					DEVID<27:16>											XXXX
		15:0	DEVID<15:0>																XXXX
0030	SYSKEY	31:16	SYSKEY<31:0>																0000
		15:0																	0000
00C0	CFGEBIA ⁽²⁾	31:16	EBIPINEN	—	—	—	—	—	—	—	EBIA23EN	EBIA22EN	EBIA21EN	EBIA20EN	EBIA19EN	EBIA18EN	EBIA17EN	EBIA16EN	0000
		15:0	EBIA15EN	EBIA14EN	EBIA13EN	EBIA12EN	EBIA11EN	EBIA10EN	EBIA9EN	EBIA8EN	EBIA7EN	EBIA6EN	EBIA5EN	EBIA4EN	EBIA3EN	EBIA2EN	EBIA1EN	EBIA0EN	0000
00D0	CFGEBIC ⁽²⁾	31:16	EBI RDYINV3	EBI RDYINV2	EBI RDYINV1	—	EBI RDYEN3	EBI RDYEN2	EBI RDYEN1	—	—	—	—	—	—	—	EBI RDYLV1	EBIRPEN	0000
		15:0	—	—	EBIWEEN	EBIOEEN	—	—	EBIBSEN1	EBIBSEN0	EBICSEN3	EBICSEN2	EBICSEN1	EBICSEN0	—	—	EBIDEN1	EBIDEN0	0000
00E0	CFGPG	31:16	ICD1PG<1:0>		—	—	—	—	CRYPTPG<1:0>		FCPG<1:0>		SQ1PG<1:0>		—	—	ETHPG<1:0>		0000
		15:0	CAN2PG<1:0>		CAN1PG<1:0>		—	—	USBPG<1:0>		—	—	DMAPG<1:0>		—	—	CPUPG<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

Note 2: This register is not available on 64-pin devices.

TABLE 34-4: DEVICE SERIAL NUMBER SUMMARY

Virtual Address (BFC5_#)	Register Name	Bit Range	Bits																All Resets ⁽¹⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4020	DEVSN0	31:16	Device Serial Number <31:16>																XXXX
		15:0	Device Serial Number <15:0>																XXXX
4024	DEVSN1	31:16	Device Serial Number <31:16>																XXXX
		15:0	Device Serial Number <15:0>																XXXX

Legend: x = unknown value on Reset.

Note 1: Reset values are dependent on the device variant.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 34-11: DEVID: DEVICE AND REVISION ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	VER<3:0> ⁽¹⁾				DEVID<27:24> ⁽¹⁾			
23:16	R	R	R	R	R	R	R	R
	DEVID<23:16> ⁽¹⁾							
15:8	R	R	R	R	R	R	R	R
	DEVID<15:8> ⁽¹⁾							
7:0	R	R	R	R	R	R	R	R
	DEVID<7:0> ⁽¹⁾							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **VER<3:0>**: Revision Identifier bits⁽¹⁾

bit 27-0 **DEVID<27:0>**: Device ID⁽¹⁾

Note 1: Refer to “*PIC32 Embedded Connectivity with Floating Point Unit (EF) Family Silicon Errata and Data Sheet Clarification*” (DS80000663) for a list of Revision and Device ID values.

REGISTER 34-12: DEVS_{Nx}: DEVICE SERIAL NUMBER REGISTER 'x' ('x' = 0, 1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	SN<31:24>							
23:16	R	R	R	R	R	R	R	R
	SN<23:16>							
15:8	R	R	R	R	R	R	R	R
	SN<15:8>							
7:0	R	R	R	R	R	R	R	R
	SN<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **SN<31:0>**: Device Unique Serial Number bits

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 37-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

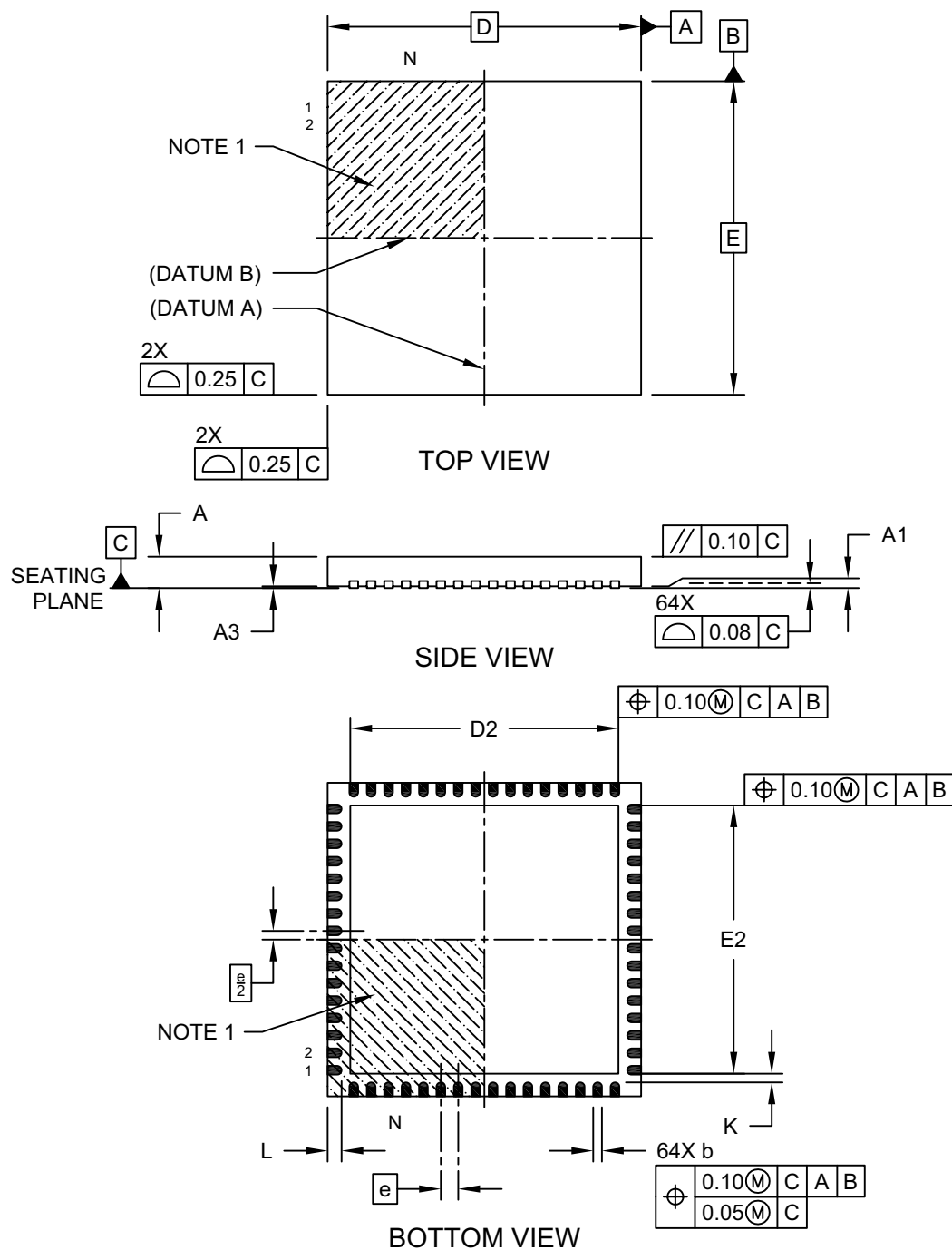
DC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Param.	Sym.	Characteristic	Min.	Typ.	Max.	Units	Conditions ⁽¹⁾
DO10	VOL	Output Low Voltage I/O Pins 4x Sink Driver Pins - RA3, RA9, RA10, RA14, RA15 RB0-RB2, RB4, RB6, RB7, RB11, RB13 RC12-RC15 RD0, RD6-RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8 RG15 RH0, RH1, RH4-RH6, RH8-RH13 RJ0-RJ2, RJ8, RJ9, RJ11	—	—	0.4	V	$I_{OL} \leq 10 \text{ mA}$, $V_{DD} = 3.3\text{V}$
		Output Low Voltage I/O Pins: 8x Sink Driver Pins - RA0-RA2, RA4, RA5 RB3, RB5, RB8-RB10, RB12, RB14, RB15 RC1-RC4 RD1-RD5, RD9, RD10, RD12, RD13, RD15 RE4-RE7 RF0, RF4, RF5, RF12, RF13 RG0, RG1, RG6-RG9 RH2, RH3, RH7, RH14, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	—	—	0.4	V	$I_{OL} \leq 15 \text{ mA}$, $V_{DD} = 3.3\text{V}$
		Output Low Voltage I/O Pins: 12x Sink Driver Pins - RA6, RA7 RE0-RE3 RF1 RG12-RG14	—	—	0.4	V	$I_{OL} \leq 20 \text{ mA}$, $V_{DD} = 3.3\text{V}$

Note 1: Parameters are characterized, but not tested.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.70 x 7.70 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-213B Sheet 1 of 2

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

A.3 CPU

The CPU in the PIC32MZ EF family of devices has been changed to the MIPS32 M-Class MPU architecture. This CPU includes DSP ASE, internal data and instruction L1 caches, and a TLB-based MMU.

Table A-4 summarizes some of the key differences (indicated by **Bold** type) in the internal CPU registers.

TABLE A-4: CPU DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
L1 Data and Instruction Cache and Prefetch Wait States	
On PIC32MX devices, the cache was included in the prefetch module outside the CPU. PREFEN<1:0> (CHECON<5:4>) 11 = Enable predictive prefetch for both cacheable and non-cacheable regions 10 = Enable predictive prefetch for non-cacheable regions only 01 = Enable predictive prefetch for cacheable regions only 00 = Disable predictive prefetch DCSZ<1:0> (CHECON<9:8>) Changing these bits causes all lines to be reinitialized to the "invalid" state. 11 = Enable data caching with a size of 4 lines 10 = Enable data caching with a size of 2 lines 01 = Enable data caching with a size of 1 line 00 = Disable data caching CHECOH (CHECON<16>) 1 = Invalidate all data and instruction lines 0 = Invalidate all data and instruction lines that are not locked	On PIC32MZ EF devices, the CPU has a separate L1 instruction and data cache in the core. The PREFEN<1:0> bits still enable the prefetch module; however, the K0<2:0> bits in the CP0 registers controls the internal L1 cache for the designated regions. PREFEN<1:0> (PRECON<5:4>) 11 = Enable predictive prefetch for any address 10 = Enable predictive prefetch for CPU instructions and CPU data 01 = Enable predictive prefetch for CPU instructions only 00 = Disable predictive prefetch K0<2:0> (CP0 Reg 16, Select 0) 011 = Cacheable, non-coherent, write-back, write allocate 010 = Uncached 001 = Cacheable, non-coherent, write-through, write allocate 000 = Cacheable, non-coherent, write-through, no write allocate
PFMWS<2:0> (CHECON<2:0>) 111 = Seven Wait states 110 = Six Wait states 101 = Five Wait states 100 = Four Wait states 011 = Three Wait states 010 = Two Wait states (61-80 MHz) 001 = One Wait state (31-60 MHz) 000 = Zero Wait state (0-30 MHz)	The Program Flash Memory read wait state frequency points have changed in PIC32MZ EF devices. The register for accessing the PFMWS field has changed from CHECON to PRECON. PFMWS<2:0> (PRECON<2:0>) 111 = Seven Wait states • • • 100 = Four Wait states (200-252 MHz) 011 = Reserved 010 = Two Wait states (133-200 MHz) 001 = One Wait state (66-133 MHz) 000 = Zero Wait states (0-66 MHz) Note: Wait states listed are for ECC enabled.
Core Instruction Execution	
On PIC32MX devices, the CPU can execute MIPS16e instructions and uses a 16-bit instruction set, which reduces memory size. MIPS16e®	On PIC32MZ EF devices, the CPU can operate a mode called microMIPS. microMIPS mode is an enhanced MIPS32® instruction set that uses both 16-bit and 32-bit opcodes. This mode of operation reduces memory size with minimum performance impact. microMIPS™ The BOOTISA (DEVCFG0<6>) Configuration bit controls the MIPS32 and microMIPS modes for boot and exception code. 1 = Boot code and Exception code is MIPS32® (ISAONEXC bit is set to '0' and the ISA<1:0> bits are set to '10' in the CP0 Config3 register) 0 = Boot code and Exception code is microMIPS™ (ISAONEXC bit is set to '1' and the ISA<1:0> bits are set to '11' in the CP0 Config3 register)

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

A.10 Package Differences

In general, PIC32MZ EF devices are mostly pin compatible with PIC32MX5XX/6XX/7XX devices; however, some pins are not. In particular, the VDD and VSS pins have been added and moved to different pins. In addition, I/O functions that were on fixed pins now will largely be on remappable pins.

TABLE A-11: PACKAGE DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
VCAP Pin	
On PIC32MX devices, an external capacitor is required between a VCAP pin and GND, which provides a filtering capacitor for the internal voltage regulator. A low-ESR capacitor (typically 10 μ F) is required on the VCAP pin.	On PIC32MZ EF devices, this requirement has been removed. No VCAP pin.
VDD and VSS Pins	
VDD on 64-pin packages: 10, 26, 38, 57 VDD on 100-pin packages: 2, 16, 37, 46, 62, 86	There are more VDD pins on PIC32MZ EF devices, and many are located on different pins. VDD on 64-pin packages: 8, 26, 39, 54, 60 VDD on 100-pin packages: 14, 37, 46, 62, 74, 83, 93
VSS on 64-pin packages: 9, 25, 41 VSS on 100-pin packages: 15, 36, 45, 65, 75	There are more VSS pins on PIC32MZ EF devices, and many are located on different pins. VSS on 64-pin packages: 7, 25, 35, 40, 55, 59 VSS on 100-pin packages: 13, 36, 45, 53, 63, 75, 84, 92
PPS I/O Pins	
All peripheral functions are fixed as to what pin upon which they operate.	Peripheral functions on PIC32MZ EF devices are now routed through a PPS module, which routes the signals to the desired pins. When migrating software, it is necessary to initialize the PPS I/O functions in order to get the signal to and from the correct pin. PPS functionality for the following peripherals: • CAN • UART • SPI (except SCK) • Input Capture • Output Compare • External Interrupt (except INT0) • Timer Clocks (except Timer1) • Reference Clocks (except REFCLK2)

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

DMSTAT (Deadman Timer Status)	297	sum).....	534
DMTCLR (Deadman Timer Clear)	296	ETHPMM0 (Ethernet Controller Pattern Match Mask 0).	533
DMTCNT (Deadman Timer Count)	298	ETHPMM1 (Ethernet Controller Pattern Match Mask 1).	533
DMTCON (Deadman Timer Control).....	295	ETHRXFC (Ethernet Controller Receive Filter Configura-	535
DMTPRECLR (Deadman Timer Preclear)	295	tion).....	535
DMTPSINTV (Post Status Configure DMT Interval Sta-	299	ETHRXOVFLOW (Ethernet Controller Receive Overflow	543
tus)	299	Statistics)	543
EBICSx (External Bus Interface Chip Select)	385	ETHRXST (Ethernet Controller RX Packet Descriptor	531
EBIFTRPDx (External Bus Interface Flash Timing) ..	388	Start Address).....	531
EBIMSKx (External Bus Interface Address Mask)	386	ETHRXWM (Ethernet Controller Receive Watermarks) .	537
EBISMCON (External Bus Interface Static Memory Con-	389	ETHSCOLFRM (Ethernet Controller Single Collision	545
trol).....	389	Frames Statistics).....	545
EBISMTx (External Bus Interface Static Memory Timing)	387	ETHSTAT (Ethernet Controller Status).....	541
EMAC1CFG1 (Ethernet Controller MAC Configuration 1)	550	ETHTXST (Ethernet Controller TX Packet Descriptor	531
EMAC1CFG2 (Ethernet Controller MAC Configuration 2)	551	Start Address).....	531
EMAC1CLRT (Ethernet Controller MAC Collision Win-	555	FCCR (Floating Point Condition Codes Register - CP1	56
dow/Retry Limit)	555	Register 25)	56
EMAC1IPGR (Ethernet Controller MAC Non-Back-to-	554	FCSR (Floating Point Control and Status Register - CP1	59
Back Interpacket Gap)	554	Register 31)	59
EMAC1IPGT (Ethernet Controller MAC Back-to-Back In-	553	FENR (Floating Point Exceptions and Modes Enable	58
terpacket Gap)	553	Register - CP1 Register 28)	58
EMAC1MADR (Ethernet Controller MAC MII Manage-	561	FEXR (Floating Point Exceptions Status Register - CP1	57
ment Address).....	561	Register 26)	57
EMAC1MAXF (Ethernet Controller MAC Maximum	556	FIR (Floating Point Implementation Register - CP1 Reg-	55
Frame Length)	556	ister 0).....	55
EMAC1MCFG (Ethernet Controller MAC MII Manage-	559	I2CxCON (I2C Control).....	357
ment Configuration)	559	I2CxSTAT (I2C Status).....	359
EMAC1MCMD (Ethernet Controller MAC MII Manage-	560	ICxCON (Input Capture x Control).....	308
ment Command)	560	IECx (Interrupt Enable Control)	149
EMAC1MIND (Ethernet Controller MAC MII Manage-	563	IFSx (Interrupt Flag Status)	149
ment Indicators)	563	INTCON (Interrupt Control).....	145
EMAC1MRDD (Ethernet Controller MAC MII Manage-	562	INTSTAT (Interrupt Status).....	148
ment Read Data).....	562	IPCx (Interrupt Priority Control)	150
EMAC1MWTD (Ethernet Controller MAC MII Manage-	562	IPTMR (Interrupt Proximity Timer).....	148
ment Write Data).....	562	NVMADDR (Flash Address)	104
EMAC1SA0 (Ethernet Controller MAC Station Address	564	NVMBWP (Flash Boot (Page) Write-protect).....	107
0).....	564	NVMCON (Programming Control)	101, 103
EMAC1SA1 (Ethernet Controller MAC Station Address	565	NVMDATAx (Flash Data ('x' = 0-3))	105
1).....	565	NVMKEY (Programming Unlock).....	104
EMAC1SA2 (Ethernet Controller MAC Station Address	566	NVMPWP (Program Flash Write-Protect).....	106
2).....	566	NVMSRCADDR (Source Data Address)	105
EMAC1SUPP (Ethernet Controller MAC PHY Support) .	557	OCxCON (Output Compare x Control)	313
EMAC1TEST (Ethernet Controller MAC Test).....	558	OSCCON (Oscillator Control)	158
ETHALGNERR (Ethernet Controller Alignment Errors	549	OSCTUN (FRC Tuning).....	160
Statistics)	549	PMADDR (Parallel Port Address).....	375
ETHCON1 (Ethernet Controller Control 1).....	528	PMAEN (Parallel Port Pin Enable).....	377
ETHCON2 (Ethernet Controller Control 2).....	530	PMCON (Parallel Port Control).....	371
ETHFCSERR (Ethernet Controller Frame Check Se-	548	PMDIN (Parallel Port Input Data).....	376, 381
quence Error Statistics).....	548	PMDOUT (Parallel Port Output Data).....	376
ETHFRMRXOK (Ethernet Controller Frames Received	547	PMODE (Parallel Port Mode).....	373
OK Statistics)	547	PMRADDR (Parallel Port Read Address).....	380
ETHFRMTXOK (Ethernet Controller Frames Transmit-	544	PMSTAT (Parallel Port Status (Slave Modes Only))..	378
ted OK Statistics)	544	PMWADDR (Parallel Port Write Address)	379
ETHHT0 (Ethernet Controller Hash Table 0)	532	PRECON (Prefetch Module Control)	171
ETHHT1 (Ethernet Controller Hash Table 1)	532	PRESTAT (Prefetch Module Status)	172
ETHIEN (Ethernet Controller Interrupt Enable).....	538	PRISS (Priority Shadow Select)	146
ETHIRQ (Ethernet Controller Interrupt Request)	539	PSCNT (Post Status Configure DMT Count Status). 298	
ETHMCOLFRM (Ethernet Controller Multiple Collision	546	PWRCON (Power Control)	114
Frames Statistics)	546	REFOxCON (Reference Oscillator Control ('x' = 1-4)) ...	163
ETHPM0 (Ethernet Controller Pattern Match Offset) 534		REFOxTRIM (Reference Oscillator Trim ('x' = 1-4)). 164	
ETHPMCS (Ethernet Controller Pattern Match Check-		RNMICON (Non-maskable Interrupt Control)	113

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

RPnR (Peripheral Pin Select Output).....	281
RSWRST (Software Reset)	112
RTCALRM (RTC ALARM Control).....	395
RTCCON (RTCC Control).....	393
RTCDATE (Real-Time Clock Date Value)	398
RTCTIME (Real-Time Clock Time Value).....	397
SBFLAG (System Bus Status Flag)	91
SBTxELRM (System Bus Target 'x' Multiple Error Clear ('x' = 0-13)).....	95
SBTxELRS (System Bus Target 'x' Single Error Single ('x' = 0-13)).....	95
SBTxECON (System Bus Target 'x' Error Control ('x' = 0-13)).....	94
SBTxELOG1 (System Bus Target 'x' Error Log 1 ('x' = 0-13)).....	92
SBTxELOG2 (System Bus Target 'x' Error Log 2 ('x' = 0-13)).....	94
SBTxRDy (System Bus Target 'x' Region 'y' Read Permissions ('x' = 0-13); ('y' = 0-8)).....	97
SBTxREGy (System Bus Target 'x' Region 'y' ('x' = 0-13); ('y' = 0-8)).....	96
SBTxWRy (System Bus Target 'x' Region 'y' Write Permissions ('x' = 0-13); ('y' = 0-8)).....	98
SPIxCON (SPI Control).....	318
SPIxCON2 (SPI Control 2).....	321
SPIxSTAT (SPI Status).....	322
SPLLCON (System PLL Control).....	161
SQI1XCON1 (SQI XIP Control 1)	328
SQI1XCON2 (SQI XIP Control Register 2)	330
T1CON (Type A Timer Control)	285
TxCON (Type B Timer Control)	291
USBCSR0 (USB Control Status 0)	206
USBCSR1 (USB Control Status 1)	208
USBCSR2 (USB Control Status 2)	209
USBCSR3 (USB Control Status 3)	211
USBCSRCON (USB Clock/Reset Control)	245
USBDMAINT (USB DMA Interrupt).....	236
USBDMAx (USB DMA Channel 'x' Memory Address)..	238
USBDMAxC (USB DMA Channel 'x' Control)	237
USBDMAxN (USB DMA Channel 'x' Count)	238
USBDPBF (USB Double Packet Buffer Disable)....	239
USBEOFRST (USB End-of-Frame/Soft Reset Control)..	233
USBExRPC (USB Endpoint 'x' Request Packet Count (Host Mode Only))	239
USBExRXA (USB Endpoint 'x' Receive Address)	235
USBExTXA (USB Endpoint 'x' Transmit Address)....	234
USBFI (USB FIFO Address).....	230
USBHWVER (USB Hardware Version).....	231
USBIE0CSR0 (USB Indexed Endpoint Control Status 0 (Endpoint 0))	213
USBIE0CSR2 (USB Indexed Endpoint Control Status 2 (Endpoint 0))	215
USBIE0CSR3 (USB Indexed Endpoint Control Status 3 (Endpoint 0))	216
USBIENCSR0 (USB Indexed Endpoint Control Status 0 (Endpoint 1-7)).....	217
USBIENCSR1 (USB Indexed Endpoint Control Status 1 (Endpoint 1-7)).....	220

USBIENCSR2 (USB Indexed Endpoint Control Status 2 (Endpoint 1-7)).....	223
USBIENCSR3 (USB Indexed Endpoint Control Status 3 (Endpoint 1-7)).....	224
USBINFO (USB Information).....	232
USBLPMR1 (USB Link Power Management Control 1) .	241
USBLPMR2 (USB Link Power Management Control 2) .	243
USBTMCON1 (USB Timing Control 1).....	240
USBTMCON2 (USB Timing Control 2).....	240
WDTCON (Watchdog Timer Control)	303
Resets	109
Revision History.....	721

S

Serial Peripheral Interface (SPI) and Inter-IC Sound (I2S)	315
Serial Quad Interface (SQI)	325
Software Simulator (MPLAB X SIM)	609
Special Features.....	581

T

Timer1 Module.....	283
Timer2/3, Timer4/5, Timer6/7, and Timer8/9 Modules	287
Timing Diagrams	
CAN I/O	649
EJTAG	662
External Clock	625
I/O Characteristics	628
I2Cx Bus Data (Master Mode)	645
I2Cx Bus Data (Slave Mode).....	647
I2Cx Bus Start/Stop Bits (Master Mode).....	645
I2Cx Bus Start/Stop Bits (Slave Mode).....	647
Input Capture (CAPx)	634
OCx/PWM.....	635
Output Compare (OCx)	635
Parallel Master Port Read	655
Parallel Master Port Write.....	656
Parallel Slave Port	654
SPIx Master Mode (CKE = 0)	636
SPIx Master Mode (CKE = 1)	638
SPIx Slave Mode (CKE = 0)	640
SPIx Slave Mode (CKE = 1)	641
Timer1-Timer9 External Clock.....	633
UART Reception.....	368
UART Transmission (8-bit or 9-bit Data)	368
Timing Requirements	
CLKO and I/O	629
Timing Specifications	
CAN I/O Requirements.....	649
I2Cx Bus Data Requirements (Master Mode).....	645
I2Cx Bus Data Requirements (Slave Mode).....	647
Input Capture Requirements	634
Output Compare/PWM Requirements	635
Simple OCx/PWM Mode Requirements	635
SPIx Master Mode (CKE = 0) Requirements.....	637
SPIx Master Mode (CKE = 1) Requirements.....	639
SPIx Slave Mode (CKE = 1) Requirements.....	641
SPIx Slave Mode Requirements (CKE = 0).....	640