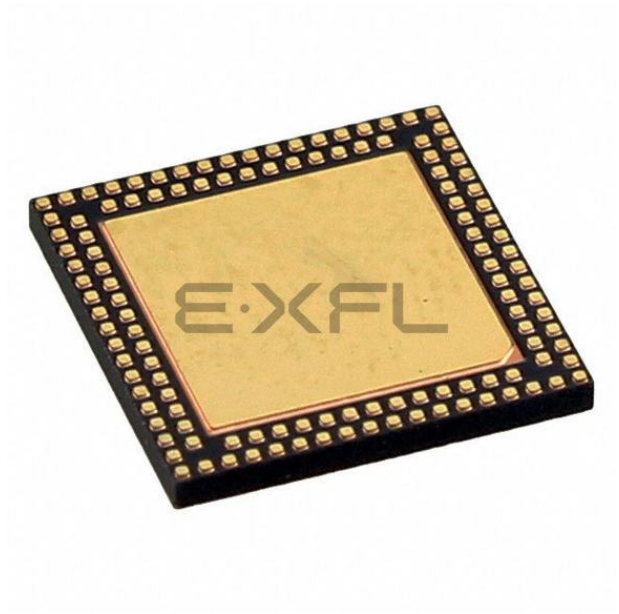

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	97
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512eff124-i-tl

3.1 Architecture Overview

The MIPS32 M-Class Microprocessor core in PIC32MZ EF family devices contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution unit
- General Purpose Register (GPR)
- Multiply/Divide Unit (MDU)
- System control coprocessor (CP0)
- Floating Point Unit (FPU)
- Memory Management Unit (MMU)
- Instruction/Data cache controllers
- Power Management
- Instructions and data caches
- microMIPS support
- Enhanced JTAG (EJTAG) controller

3.1.1 EXECUTION UNIT

The processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. Seven additional register file shadow sets (containing thirty-two registers) are added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Trap condition comparator
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the `CLZ` and `CLO` instructions
- Arithmetic Logic Unit (ALU) for performing arithmetic and bitwise logical operations
- Shifter and store aligner
- DSP ALU and logic block for performing DSP instructions, such as arithmetic/shift/compare operations

3.1.2 MULTIPLY/DIVIDE UNIT (MDU)

The processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations, and DSP ASE multiply instructions. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x32 booth recoded multiplier, four pairs of result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x32) represents the *rs* operand. The second number ('32' of 32x32) represents the *rt* operand.

The MDU supports execution of one multiply or multiply-accumulate operation every clock cycle.

Divide operations are implemented with a simple 1-bit-per-clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent `MDU` instruction while a divide is still active causes an IU pipeline stall until the divide operation has completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the processor core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MIPS32® M-CLASS MICROPROCESSOR CORE HIGH-PERFORMANCE INTEGER MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul *rt*) (div *rs*)	Latency	Repeat Rate
`MULT/MULTU, MADD/MADDU, MSUB/MSUBU` (HI/LO destination)	16 bits	5	1
	32 bits	5	1
`MUL` (GPR destination)	16 bits	5	1
	32 bits	5	1
`DIV/DIVU`	8 bits	12/14	12/14
	16 bits	20/22	20/22
	24 bits	28/30	28/30
	32 bits	36/38	36/38

REGISTER 5-2: NVMCON2: FLASH PROGRAMMING CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
	SWAPLOCK<1:0>		—	—	—	—	—	—

Legend:	HC = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-6 **SWAPLOCK<1:0>:** Flash Memory Swap Lock Control bits
11 = PFSWAP and BFSWAP are not writable and SWAPLOCK is not writable
10 = PFSWAP and BFSWAP are not writable and SWAPLOCK is writable
01 = PFSWAP and BFSWAP are not writable and SWAPLOCK is writable
00 = PFSWAP and BFSWAP are writable and SWAPLOCK is writable

bit 5-0 **Unimplemented:** Read as '0'

REGISTER 5-8: NVMBWP: FLASH BOOT (PAGE) WRITE-PROTECT REGISTER

bit 4 **UBWP4:** Upper Boot Alias Page 4 Write-protect bit(1)
1 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF enabled
0 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF disabled

bit 3 **UBWP3:** Upper Boot Alias Page 3 Write-protect bit(1)
1 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF enabled
0 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF disabled

bit 2 **UBWP2:** Upper Boot Alias Page 2 Write-protect bit(1)
1 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF enabled
0 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF disabled

bit 1 **UBWP1:** Upper Boot Alias Page 1 Write-protect bit(1)
1 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF enabled
0 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF disabled

bit 0 **UBWP0:** Upper Boot Alias Page 0 Write-protect bit(1)
1 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF enabled
0 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF disabled

Note 1: These bits are only available when the NVMKEY unlock sequence is performed and the associated Lock bit (LBWPULOCK or UBWPULOCK) is set.

Note:	The bits in this register are only writable when the NVMKEY unlock sequence is followed.

REGISTER 10-7: DCHxCON: DMA CHANNEL x CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPIGN<7:0>							
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0
	CHBUSY	—	CHIPGNEN	—	CHPATLEN	—	—	CHCHNS(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R/W-0
	CHEN(2)	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **CHPIGN<7:0>:** Channel Register Data bits
Pattern Terminate mode:
Any byte matching these bits during a pattern match may be ignored during the pattern match determination when the CHPIGNEN bit is set. If a byte is read that is identical to this data byte, the pattern match logic will treat it as a "don't care" when the pattern matching logic is enabled and the CHPIGEN bit is set.

bit 23-16 **Unimplemented:** Read as '0'

bit 15 **CHBUSY:** Channel Busy bit
1 = Channel is active or has been enabled
0 = Channel is inactive or has been disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CHPIGNEN:** Enable Pattern Ignore Byte bit
1 = Treat any byte that matches the CHPIGN<7:0> bits as a "don't care" when pattern matching is enabled
0 = Disable this feature

bit 12 **Unimplemented:** Read as '0'

bit 11 **CHPATLEN:** Pattern Length bit
1 = 2 byte length
0 = 1 byte length

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **CHCHNS:** Chain Channel Selection bit(1)
1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 **CHEN:** Channel Enable bit(2)
1 = Channel is enabled
0 = Channel is disabled

bit 6 **CHAED:** Channel Allow Events If Disabled bit
1 = Channel start/abort events will be registered, even if the channel is disabled
0 = Channel start/abort events will be ignored if the channel is disabled

bit 5 **CHCHN:** Channel Chain Enable bit
1 = Allow channel to be chained
0 = Do not allow channel to be chained

Note 1: The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).

2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

REGISTER 10-16: DCHxCSIZ: DMA CHANNEL x CELL-SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCSIZ<15:0>:** Channel Cell-Size bits

1111111111111111 = 65,535 bytes transferred on an event
•
•
•
0000000000000010 = 2 bytes transferred on an event
0000000000000001= 1 byte transferred on an event
0000000000000000 = 65,536 bytes transferred on an event

REGISTER 10-17: DCHxCPTR: DMA CHANNEL x CELL POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCPTR<15:0>:** Channel Cell Progress Pointer bits

1111111111111111 = 65,535 bytes have been transferred since the last event
•
•
•
0000000000000001 = 1 byte has been transferred since the last event
0000000000000000 = 0 bytes have been transferred since the last event

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3128	USB E2CSR2	31:16	Indexed by the same bits in USBIE2CSR2																0000
		15:0																	0000
312C	USB E2CSR3	31:16	Indexed by the same bits in USBIE2CSR3																0000
		15:0																	0000
3130	USB E3CSR0	31:16	Indexed by the same bits in USBIE3CSR0																0000
		15:0																	0000
3134	USB E3CSR1	31:16	Indexed by the same bits in USBIE3CSR1																0000
		15:0																	0000
3138	USB E3CSR2	31:16	Indexed by the same bits in USBIE3CSR2																0000
		15:0																	0000
313C	USB E3CSR3	31:16	Indexed by the same bits in USBIE3CSR3																0000
		15:0																	0000
3140	USB E4CSR0	31:16	Indexed by the same bits in USBIE4CSR0																0000
		15:0																	0000
3144	USB E4CSR1	31:16	Indexed by the same bits in USBIE4CSR1																0000
		15:0																	0000
3148	USB E4CSR2	31:16	Indexed by the same bits in USBIE4CSR2																0000
		15:0																	0000
314C	USB E4CSR3	31:16	Indexed by the same bits in USBIE4CSR3																0000
		15:0																	0000
3150	USB E5CSR0	31:16	Indexed by the same bits in USBIE5CSR0																0000
		15:0																	0000
3154	USB E5CSR1	31:16	Indexed by the same bits in USBIE5CSR1																0000
		15:0																	0000
3158	USB E5CSR2	31:16	Indexed by the same bits in USBIE5CSR2																0000
		15:0																	0000
315C	USB E5CSR3	31:16	Indexed by the same bits in USBIE5CSR3																0000
		15:0																	0000
3160	USB E6CSR0	31:16	Indexed by the same bits in USBIE6CSR0																0000
		15:0																	0000
3164	USB E6CSR1	31:16	Indexed by the same bits in USBIE6CSR1																0000
		15:0																	0000
3168	USB E6CSR2	31:16	Indexed by the same bits in USBIE6CSR2																0000
		15:0																	0000
316C	USB E6CSR3	31:16	Indexed by the same bits in USBIE6CSR3																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

REGISTER 11-4: USBCSR3: USB CONTROL STATUS REGISTER 3 (CONTINUED)

bit 19-16 **ENDPOINT<3:0>:** Endpoint Registers Select bits
1111 = Reserved
•
•
•
1000 = Reserved
0111 = Endpoint 7
•
•
•
0000 = Endpoint 0
These bits select which endpoint registers are accessed through addresses 3010-301F.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **RFRMNUM<10:0>:** Last Received Frame Number bits

REGISTER 11-10: USBIENCSR2: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 2 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXINTERV<7:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>			
15:8	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	RXCNT<13:8>					
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXCNT<7:0>							

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **TXINTERV<7:0>:** Endpoint TX Polling Interval/NAK Limit bits (*Host mode*)

For Interrupt and Isochronous transfers, this field defines the polling interval for the endpoint. For Bulk endpoints, this field sets the number of frames/microframes after which the endpoint should time out on receiving a stream of NAK responses.

The following table describes the valid values and interpretation for these bits:

Transfer Type	Speed	Valid Values (m)	Interpretation
Interrupt	Low/Full	0x01 to 0xFF	Polling interval is 'm' frames.
	High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames.
Isochronous	Full or High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames/microframes.
Bulk	Full or High	0x02 to 0x10	NAK limit is $2^{(m-1)}$ frames/microframes. A value of '0' or '1' disables the NAK time-out function.

bit 23-22 **SPEED<1:0>:** TX Endpoint Operating Speed Control bits (*Host mode*)
11 = Low-Speed
10 = Full-Speed
01 = Hi-Speed
00 = Reserved

bit 21-20 **PROTOCOL<1:0>:** TX Endpoint Protocol Control bits
11 = Interrupt
10 = Bulk
01 = Isochronous
00 = Control

bit 19-16 **TEP<3:0>:** TX Target Endpoint Number bits

This value is the endpoint number contained in the TX endpoint descriptor returned to the USB module during device enumeration.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **RXCNT<13:0>:** Receive Count bits

The number of received data bytes in the endpoint RX FIFO. The value returned changes as the contents of the FIFO change and is only valid while RXPKTRDY is set.

TABLE 12-15: PORTG REGISTER MAP FOR 100-PIN, 124-PIN, AND 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	ANSELG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSG15	—	—	—	—	—	ANSG9	ANSG8	ANSG7	ANSG6	—	—	—	—	—	—	83C0
0610	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISG15	TRISG14	TRISG13	TRISG12	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	TRISG1	TRISG0	F3C3
0620	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RG15	RG14	RG13	RG12	—	—	RG9	RG8	RG7	RG6	—	—	—	—	RG1	RG0	xxxx
0630	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATG15	LATG14	LATG13	LATG12	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	LATG1	LATG0	xxxx
0640	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCG15	ODCG14	ODCG13	ODCG12	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	ODCG1	ODCG0	0000
0650	CNPUG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUG15	CNPUG14	CNPUG13	CNPUG12	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	CNPUG1	CNPUG0	0000
0660	CNPDG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDG15	CNPDG14	CNPDG13	CNPDG12	—	—	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	CNPDG1	CNPDG0	0000
0670	CNCONG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0680	CNENG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNENG15	CNENG14	CNENG13	CNENG12	—	—	CNENG9	CNENG8	CNENG7	CNENG6	—	—	—	—	CNENG1	CNENG0	0000
0690	CNSTATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATG15	CN STATG14	CN STATG13	CN STATG12	—	—	CN STATG9	CN STATG8	CN STATG7	CN STATG6	—	—	—	—	CN STATG1	CN STATG0	0000
06A0	CNNEG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEG15	CNNEG14	CNNEG13	CNNEG12	—	—	CNNEG9	CNNEG8	CNNEG7	CNNEG6	—	—	—	—	CNNEG1	CNNEG0	0000
06B0	CNFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFG15	CNFG14	CNFG13	CNFG12	—	—	CNFG9	CNFG8	CNFG7	CNFG6	—	—	—	—	CNFG1	CNFG0	0000
06C0	SRCON0G	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	SR0G14	SR0G13	SR0G12	—	—	SR0G9	—	—	SR0G6	—	—	—	—	—	—	0000
06D0	SRCON1G	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	SR1G14	SR1G13	SR1G12	—	—	SR1G9	—	—	SR1G6	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

FIGURE 26-2: FORMAT OF BD_CTRL

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	DESC_EN	—	CRY_MODE<2:0>			—	—	—
23-16	—	SA_ FETCH_EN	—	—	LAST_BD	LIFM	PKT_ INT_EN	CBD_ INT_EN
15-8	BD_BUFLEN<15:8>							
7-0	BD_BUFLEN<7:0>							

bit 31 **DESC_EN**: Descriptor Enable
1 = The descriptor is owned by hardware. After processing the BD, hardware resets this bit to '0'.
0 = The descriptor is owned by software

bit 30 **Unimplemented:** Must be written as '0'

bit 29-27 **CRY_MODE<2:0>:** Crypto Mode
111 = Reserved
110 = Reserved
101 = Reserved
100 = Reserved
011 = CEK operation
010 = KEK operation
001 = Preboot authentication
000 = Normal operation

bit 22 **SA_FETCH_EN:** Fetch Security Association From External Memory
1 = Fetch SA from the SA pointer. This bit needs to be set to '1' for every new packet.
0 = Use current fetched SA or the internal SA

bit 21-20 **Unimplemented:** Must be written as '0'

bit 19 **LAST_BD:** Last Buffer Descriptors
1 = Last Buffer Descriptor in the chain
0 = More Buffer Descriptors in the chain
After the last BD, the CEBDADDR goes to the base address in CEBDPADDR.

bit 18 **LIFM:** Last In Frame
In case of Receive Packets (from H/W-> Host), this field is filled by the Hardware to indicate whether the packet goes across multiple buffer descriptors. In case of transmit packets (from Host -> H/W), this field indicates whether this BD is the last in the frame.

bit 17 **PKT_INT_EN:** Packet Interrupt Enable
Generate an interrupt after processing the current buffer descriptor, if it is the end of the packet.

bit 16 **CBD_INT_EN:** CBD Interrupt Enable
Generate an interrupt after processing the current buffer descriptor.

bit 15-0 **BD_BUFLEN<15:0>:** Buffer Descriptor Length
This field contains the length of the buffer and is updated with the actual length filled by the receiver.

FIGURE 26-3: FORMAT OF BD_SADDR

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	BD_SAADDR<31:24>							
23-16	BD_SAADDR<23:16>							
15-8	BD_SAADDR<15:8>							
7-0	BD_SAADDR<7:0>							

bit 31-0 **BD_SAADDR<31:0>:** Security Association IP Session Address
The sessions' SA pointer has the keys and IV values.

26.3 Security Association Structure

Table 26-4 shows the Security Association Structure. The Crypto Engine uses the Security Association to determine the settings for processing a Buffer Descriptor Processor. The Security Association contains:

- Which algorithm to use
- Whether to use engines in parallel (for both authentication and encryption/decryption)
- The size of the key
- Authentication key
- Encryption/decryption key
- Authentication Initialization Vector (IV)
- Encryption IV

TABLE 26-4: CRYPTO ENGINE SECURITY ASSOCIATION STRUCTURE

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SA_CTRL	31:24	—	—	VERIFY	—	NO_RX	OR_EN	ICVONLY	IRFLAG
	23:16	LNC	LOADIV	FB	FLAGS	—	—	—	ALGO<6>
	15:8	ALGO<5:0>						ENCTYPE	KEYSIZE<1>
	7:0	KEYSIZE<0>	MULTITASK<2:0>			CRYPTOALGO<3:0>			
SA_AUTHKEY1	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY2	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY3	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY4	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY5	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY6	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY7	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY8	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_ENCKEY1	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY2	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							

REGISTER 28-1: ADCCON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 20-16 **STRGSRC<4:0>:** Scan Trigger Source Select bits
11111 = Reserved
•
•
•
01101 = Reserved
01100 = Comparator 2 (COUT)
01011 = Comparator 1 (COUT)
01010 = OCMP5
01001 = OCMP3
01000 = OCMP1
00111 = TMR5 match
00110 = TMR3 match
00101 = TMR1 match
00100 = INT0 External interrupt
00011 = Reserved
00010 = Global level software trigger (GLSWTRG)
00001 = Global software edge trigger (GSWTRG)
00000 = No Trigger

bit 15 **ON:** ADC Module Enable bit
1 = ADC module is enabled
0 = ADC module is disabled
Note: The ON bit should be set only after the ADC module has been configured.

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **AICPMPEN:** Analog Input Charge Pump Enable bit
1 = Analog input charge pump is enabled (default)
0 = Analog input charge pump is disabled

bit 11 **CVDEN:** Capacitive Voltage Division Enable bit
1 = CVD operation is enabled
0 = CVD operation is disabled

bit 10 **FSSCLKEN:** Fast Synchronous System Clock to ADC Control Clock bit
1 = Fast synchronous system clock to ADC control clock is enabled
0 = Fast synchronous system clock to ADC control clock is disabled

bit 9 **FSPBCLKEN:** Fast Synchronous Peripheral Clock to ADC Control Clock bit
1 = Fast synchronous peripheral clock to ADC control clock is enabled
0 = Fast synchronous peripheral clock to ADC control clock is disabled

bit 8-7 **Unimplemented:** Read as '0'

bit 6-4 **IRQVS<2:0>:** Interrupt Vector Shift bits
To determine interrupt vector address, this bit specifies the amount of left shift done to the ARDYx status bits in the ADCDSTAT1 and ADCDSTAT2 registers, prior to adding with the ADCBASE register.
Interrupt Vector Address = Read Value of ADCBASE and Read Value of ADCBASE = Value written to ADCBASE + x << IRQVS<2:0>, where 'x' is the smallest active input ID from the ADCDSTAT1 or ADCDSTAT2 registers (which has highest priority).
111 = Shift x left 7 bit position
110 = Shift x left 6 bit position
101 = Shift x left 5 bit position
100 = Shift x left 4 bit position
011 = Shift x left 3 bit position
010 = Shift x left 2 bit position
001 = Shift x left 1 bit position
000 = Shift x left 0 bit position

REGISTER 28-7: ADCIMCON3: ADC INPUT MODE CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DIFF44	SIGN44
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF43	SIGN43	DIFF42(2)	SIGN42(2)	DIFF41(2)	SIGN41(2)	DIFF40(2)	SIGN40(2)
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF39(2)	SIGN39(2)	DIFF38(2)	SIGN38(2)	DIFF37(2)	SIGN37(2)	DIFF36(2)	SIGN36(2)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF35(2)	SIGN35(2)	DIFF34(1)	SIGN34(1)	DIFF33(1)	SIGN33(1)	DIFF32(1)	SIGN32(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **DIFF44:** AN44 Mode bit
1 = AN44 is using Differential mode
0 = AN44 is using Single-ended mode

bit 24 **SIGN44:** AN44 Signed Data Mode bit
1 = AN44 is using Signed Data mode
0 = AN44 is using Unsigned Data mode

bit 23 **DIFF43:** AN43 Mode bit
1 = AN43 is using Differential mode
0 = AN43 is using Single-ended mode

bit 22 **SIGN43:** AN43 Signed Data Mode bit
1 = AN43 is using Signed Data mode
0 = AN43 is using Unsigned Data mode

bit 21 **DIFF42:** AN42 Mode bit(2)
1 = AN42 is using Differential mode
0 = AN42 is using Single-ended mode

bit 20 **SIGN42:** AN42 Signed Data Mode bit(2)
1 = AN42 is using Signed Data mode
0 = AN42 is using Unsigned Data mode

bit 19 **DIFF41:** AN41 Mode bit(2)
1 = AN41 is using Differential mode
0 = AN41 is using Single-ended mode

bit 18 **SIGN41:** AN41 Signed Data Mode bit(2)
1 = AN41 is using Signed Data mode
0 = AN41 is using Unsigned Data mode

bit 17 **DIFF40:** AN40 Mode bit(2)
1 = AN40 is using Differential mode
0 = AN40 is using Single-ended mode

Note 1: This bit is not available on 64-pin devices.
2: This bit is not available on 64-pin and 100-pin devices.

NOTES:

34.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 32. "Configuration"** (DS60001124) and **Section 33. "Programming and Diagnostics"** (DS60001129) in the *"PIC32 Family Reference Manual"*, which are available from the Microchip web site (www.microchip.com/PIC32).

PIC32MZ EF devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

- Flexible device configuration
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming™ (ICSP™)
- Internal temperature sensor

34.1 Configuration Bits

PIC32MZ EF devices contain two Boot Flash memories (Boot Flash 1 and Boot Flash 2), each with an associated configuration space. These configuration spaces can be programmed to contain various device configurations. Configuration space that is aliased by the Lower Boot Alias memory region is used to provide values for the following Configuration registers. See **4.1.1 "Boot Flash Sequence and Configuration Spaces"** for more information.

- DEVSIGN0/ADEVSIGN0: Device Signature Word 0 Register
- DEVCP0/ADEVCP0: Device Code-Protect 0 Register
- DEVCFG0/ADEVCFG0: Device Configuration Word 0
- DEVCFG1/ADEVCFG1: Device Configuration Word 1
- DEVCFG2/ADEVCFG2: Device Configuration Word 2
- DEVCFG3/ADEVCFG3: Device Configuration Word 3
- DEVADCx: Device ADC Calibration Word 'x' ('x' = 0-4, 7)

The following run-time programmable Configuration registers provide additional configuration control:

- CFGCON: Configuration Control Register
- CFGEBIA: External Bus Interface Address Pin Configuration Register
- CFGEBIC: External Bus Interface Control Pin Configuration Register
- CFGPG: Permission Group Configuration Register

In addition, the DEVID register provides device and revision information, the DEVADC0-DEVADC4 and DEVADC7 registers provide ADC module calibration/ configuration data, and the DEVSN0 and DEVSN1 registers contain a unique serial number of the device.

Note: Do not use Word program operation (NVMOP<3:0> = 0001) when programming the device Words that are described in this section.

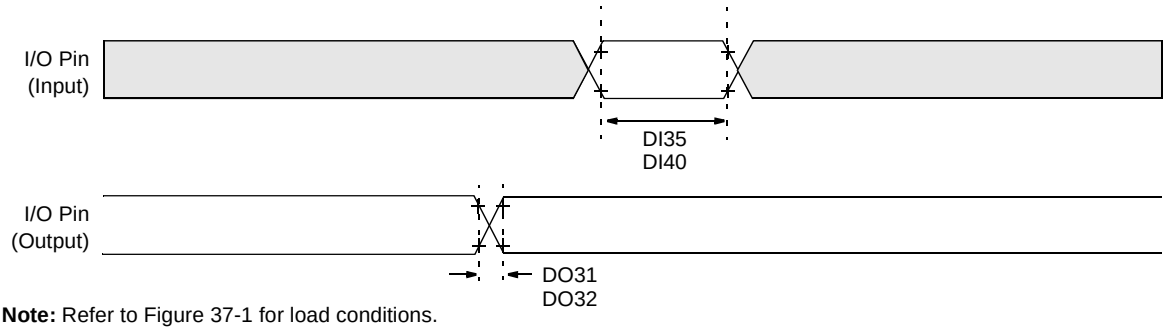
35.0 INSTRUCTION SET

The PIC32MZ EF family instruction set complies with the MIPS32® Release 5 instruction set architecture. The PIC32MZ EF device family *does not* support the following features:

- Core extend instructions
- Coprocessor 2 instructions

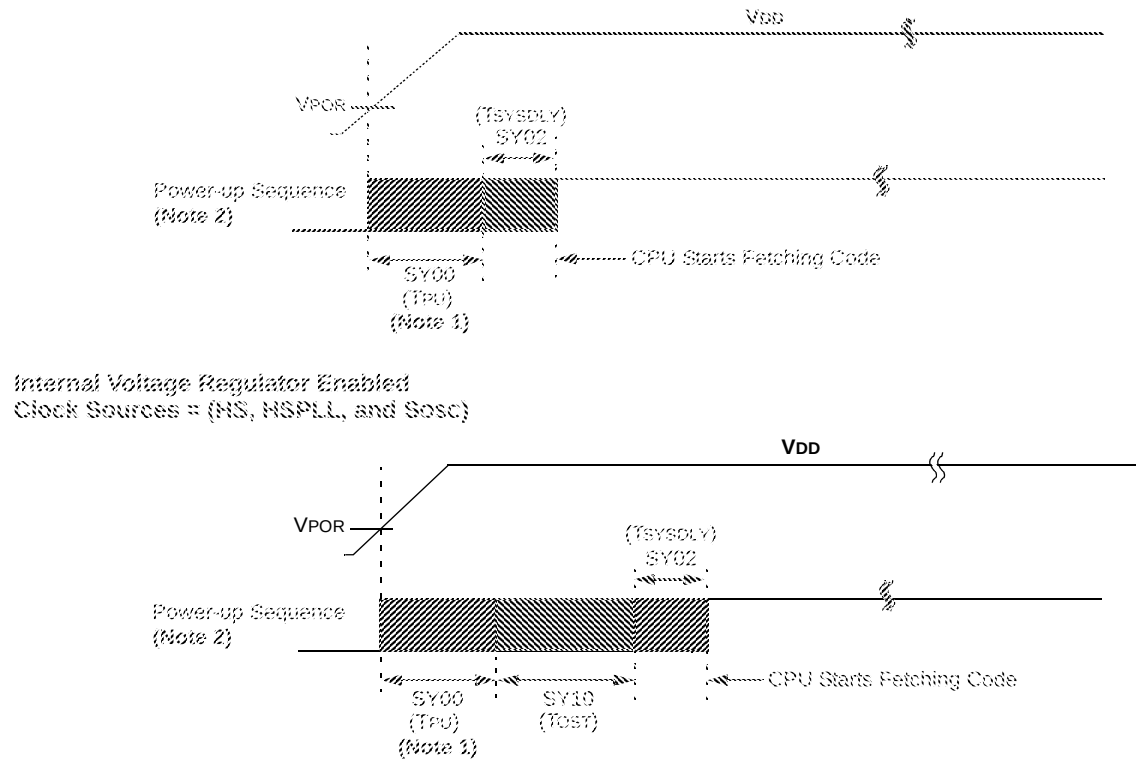
Note: Refer to *"MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set"* at www.imgtec.com for more information.

FIGURE 37-3: I/O TIMING CHARACTERISTICS



Note: Refer to Figure 37-1 for load conditions.

FIGURE 37-4: POWER-ON RESET TIMING CHARACTERISTICS

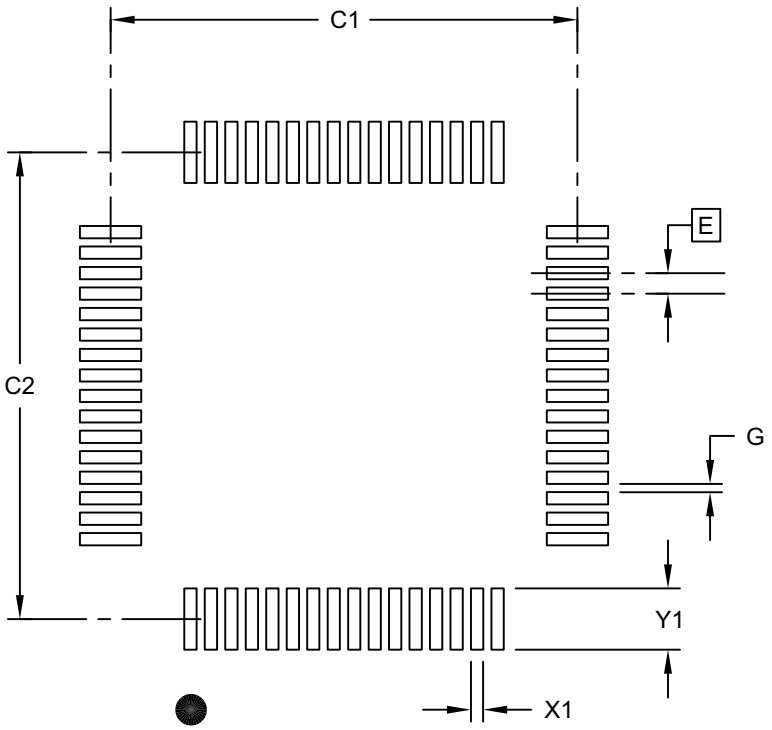


Note 1: The power-up period will be extended if the power-up sequence completes before the device exits from BOR ($V_{DD} < V_{DDMIN}$).

2: Includes interval voltage regulator stabilization delay.

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

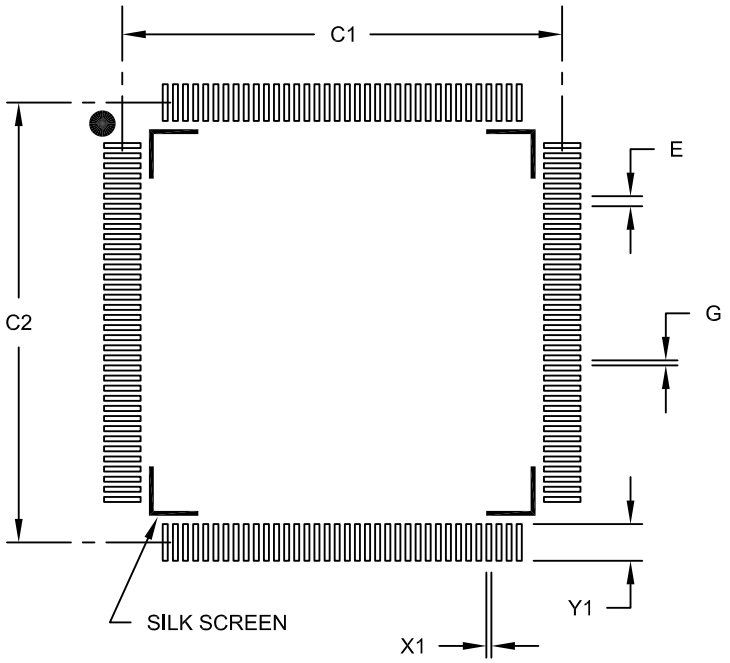
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2085B Sheet 1 of 1

144-Lead Plastic Thin Quad Flat Pack (PH) - 16x16 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		17.40	
Contact Pad Spacing	C2		17.40	
Contact Pad Width (X144)	X1			0.20
Contact Pad Length (X144)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2155B