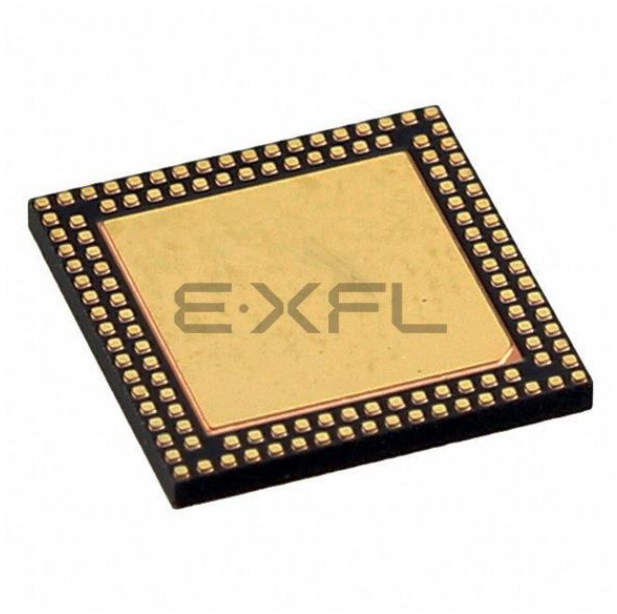
Microchip Technology - PIC32MZ0512EFF124T-I/TL Datasheet



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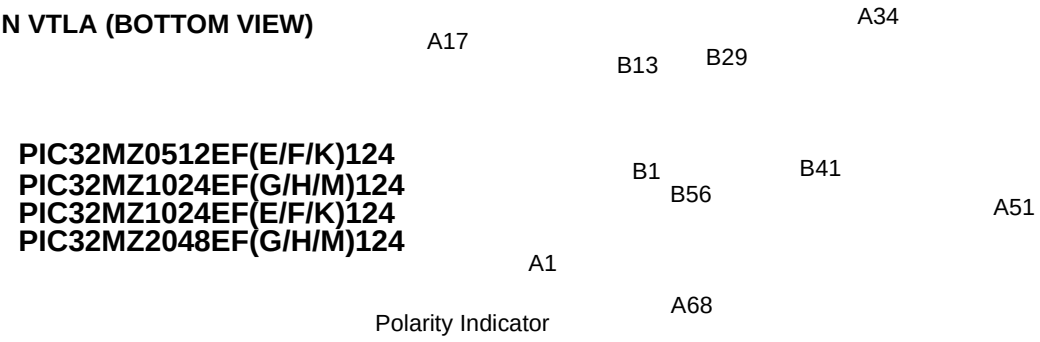
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	97
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512eff124t-i-tl

TABLE 4: PIN NAMES FOR 124-PIN DEVICES

124-PIN VTLA (BOTTOM VIEW)



Package Pin #	Full Pin Name	Package Pin #	Full Pin Name
A1	No Connect	A35	VBUS
A2	AN23/RG15	A36	VUSB3V3
A3	EBID5/AN17/RPE5/PMD5/RE5	A37	D-
A4	EBID7/AN15/PMD7/RE7	A38	RPF3/USBID/RF3
A5	AN35/ETXD0/RJ8	A39	EBIRDY2/RPF8/SCL3/RF8
A6	EBIA12/AN21/RPC2/PMA12/RC2	A40	ERXD3/RH9
A7	$\overline{\text{EBIOE}}$/AN19/RPC4/PMRD/RC4	A41	$\overline{\text{EBICS0}}$/SCL2/RA2
A8	EBIA4/AN13/C1INC/RPG7/SDA4/PMA4/RG7	A42	EBIA14/PMCS1/PMA14/RA4
A9	VSS	A43	VSS
A10	$\overline{\text{MCLR}}$	A44	EBIA8/RPF5/SCL5/PMA8/RF5
A11	TMS/EBIA16/AN24/RA0	A45	RPA15/SDA1/RA15
A12	AN26/RPE9/RE9	A46	RPD10/SCK4/RD10
A13	AN4/C1INB/RB4	A47	ECRS/RH12
A14	AN3/C2INA/RPB3/RB3	A48	RPD0/RTCC/INT0/RD0
A15	VDD	A49	SOSCO/RPC14/T1CK/RC14
A16	AN2/C2INB/RPB2/RB2	A50	VDD
A17	PGEC1/AN1/RPB1/RB1	A51	VSS
A18	PGED1/AN0/RPB0/RB0	A52	RPD1/SCK1/RD1
A19	PGED2/AN47/RPB7/RB7	A53	EBID15/RPD3/PMD15/RD3
A20	VREF+/CVREF+/AN28/RA10	A54	EBID13/PMD13/RD13
A21	AVSS	A55	EMDIO/RJ1
A22	AN39/ETXD3/RH1	A56	$\overline{\text{SQICS0}}$/RPD4/RD4
A23	EBIA7/AN49/RPB9/PMA7/RB9	A57	ETXEN/RPD6/RD6
A24	AN6/RB11	A58	VDD
A25	VDD	A59	EBID11/RPF0/PMD11/RF0
A26	TDI/EBIA18/AN30/RPF13/SCK5/RF13	A60	EBID9/RPG1/PMD9/RG1
A27	EBIA11/AN7/PMA11/RB12	A61	TRCLK/SQICLK/RA6
A28	EBIA1/AN9/RPB14/SCK3/PMA1/RB14	A62	RJ4
A29	VSS	A63	VSS
A30	AN40/ERXERR/RH4	A64	EBID1/PMD1/RE1
A31	AN42/ERXD2/RH6	A65	TRD1/SQID1/RG12
A32	AN33/RPD15/SCK6/RD15	A66	EBID2/SQID2/PMD2/RE2
A33	OSC2/CLKO/RC15	A67	EBID4/AN18/PMD4/RE4
A34	No Connect	A68	No Connect

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RJx) can be used as a change notification pin (CNAx-CNJx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4.1.1 BOOT FLASH SEQUENCE AND CONFIGURATION SPACES

Sequence space is used to identify which boot Flash is aliased by aliased regions. If the value programmed into the TSEQ<15:0> bits of the BF1SEQ3 word is equal to or greater than the value programmed into the TSEQ<15:0> bits of the BF2SEQ3 word, boot Flash 1 is aliased by the lower boot alias region, and boot Flash 2 is aliased by the upper boot alias region. If the TSEQ<15:0> bits of the BF2SEQ3 word is greater than the TSEQ<15:0> bits of the BF1SEQ3 word, the opposite is true (see Table 4-2 and Table 4-3 for BFxSEQ3 word memory locations).

The CSEQ<15:0> bits must contain the one's complement value of the TSEQ<15:0> bits; otherwise, the value of the TSEQ<15:0> bits is considered invalid, and an alternate sequence is used. See **Section 4.1.2 "Alternate Sequence and Configuration Words"** for more information.

Once boot Flash memories are aliased, configuration space located in the lower boot alias region is used as the basis for the Configuration words, DEVSIGN0, DEVCP0, and DEVCFGx (and the associated alternate configuration registers). This means that the boot Flash region to be aliased by lower boot alias region memory must contain configuration values in the appropriate memory locations.

Note:	Do not use word program operation (NVMOP<3:0> = `0001`) when programming data into the sequence and configuration spaces.

4.1.2 ALTERNATE SEQUENCE AND CONFIGURATION WORDS

Every word in the configuration space and sequence space has an associated alternate word (designated by the letter A as the first letter in the name of the word). During device start-up, primary words are read and if uncorrectable ECC errors are found, the BCFGERR (RCON<27>) flag is set and alternate words are used. If uncorrectable ECC errors are found in primary and alternate words, the BCFGFAIL (RCON<26>) flag is set and the default configuration is used.

TABLE 4-9: SYSTEM BUS TARGET 1 REGISTER MAP (CONTINUED)

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
84E0	SBT1REG5	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
84F0	SBT1RD5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84F8	SBT1WR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8500	SBT1REG6	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8510	SBT1RD6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8518	SBT1WR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8520	SBT1REG7	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8530	SBT1RD7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8538	SBT1WR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8540	SBT1REG8	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8550	SBT1RD8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8558	SBT1WR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

7.1 CPU Exceptions

CPU coprocessor 0 contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events or program errors. Table 7-1 lists the exception types in order of priority.

TABLE 7-1: MIPS32® M-CLASS MICROPROCESSOR CORE EXCEPTION TYPES

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Highest Priority						
Reset	Assertion $\overline{\text{MCLR}}$ or a Power-on Reset (POR).	0xBFC0_0000	BEV, ERL	—	—	_on_reset
Soft Reset	Assertion of a software Reset.	0xBFC0_0000	BEV, SR, ERL	—	—	_on_reset
DSS	EJTAG debug single step.	0xBFC0_0480	—	DSS	—	—
DINT	EJTAG debug interrupt. Caused by the assertion of the external EJ_DINT input or by setting the EjtagBrk bit in the ECR register.	0xBFC0_0480	—	DINT	—	—
NMI	Assertion of NMI signal.	0xBFC0_0000	BEV, NMI, ERL	—	—	_nmi_handler
Machine Check	TLB write that conflicts with an existing entry.	EBASE+0x180	MCHECK, EXL	—	0x18	_general_exception_handler
Interrupt	Assertion of unmasked hardware or software interrupt signal.	See Table 7-2.	IPL<2:0>	—	0x00	See Table 7-2.
Deferred Watch	Deferred watch (unmasked by K|DM=>!(K|DM) transition).	EBASE+0x180	WP, EXL	—	0x17	_general_exception_handler
DIB	EJTAG debug hardware instruction break matched.	0xBFC0_0480	—	DIB	—	—
WATCH	A reference to an address that is in one of the Watch registers (fetch).	EBASE+0x180	EXL	—	0x17	_general_exception_handler
AdEL	Fetch address alignment error. Fetch reference to protected address.	EBASE+0x180	EXL	—	0x04	_general_exception_handler
TLBL	Fetch TLB miss or fetch TLB hit to page with V = 0.	EBASE if Status.EXL = 0	—	—	0x02	—
		EBASE+0x180 if Status.EXL == 1	—	—	0x02	_general_exception_handler
TLBL Execute Inhibit	An instruction fetch matched a valid TLB entry that had the XI bit set.	EBASE+0x180	EXL	—	0x14	_general_exception_handler
IBE	Instruction fetch bus error.	EBASE+0x180	EXL	—	0x06	_general_exception_handler

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0638	OFF062	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
063C	OFF063	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0640	OFF064	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0644	OFF065	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0648	OFF066	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
064C	OFF067	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0650	OFF068	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0654	OFF069	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0658	OFF070	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
065C	OFF071	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0660	OFF072	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0664	OFF073	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0668	OFF074	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
066C	OFF075	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0670	OFF076	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

REGISTER 11-6: USBIE0CSR2: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 2 (ENDPOINT 0)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	NAKLIM<4:0>				
23:16	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
	SPEED<1:0>		—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	RXCNT<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **NAKLIM<4:0>:** Endpoint 0 NAK Limit bits

The number of frames/microframes (Hi-Speed transfers) after which Endpoint 0 should time-out on receiving a stream of NAK responses.

bit 23-22 **SPEED<1:0>:** Operating Speed Control bits
11 = Low-Speed
10 = Full-Speed
01 = Hi-Speed
00 = Reserved

bit 21-7 **Unimplemented:** Read as '0'

bit 6-0 **RXCNT<6:0>:** Receive Count bits

The number of received data bytes in the Endpoint 0 FIFO. The value returned changes as the contents of the FIFO change and is only valid while RXPKTRDY is set.

REGISTER 20-22: SQI1INTSIGEN: SQI INTERRUPT SIGNAL ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DMAEISE	PKT DONEISE	BD DONEISE	CON THRISE
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CON EMPTYISE	CON FULLISE	RX THRISE	RX FULLISE	RX EMPTYISE	TX THRISE	TX FULLISE	TX EMPTYISE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11 **DMAEISE:** DMA Bus Error Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 10 **PKTDONEISE:** Receive Error Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 9 **BDDONEISE:** Transmit Error Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 8 **CONTHRISE:** Control Buffer Threshold Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 7 **CONEMPTYISE:** Control Buffer Empty Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 6 **CONFULLISE:** Control Buffer Full Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 5 **RXTHRISE:** Receive Buffer Threshold Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 4 **RXFULLISE:** Receive Buffer Full Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 3 **RXEMPTYISE:** Receive Buffer Empty Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 2 **TXTHRISE:** Transmit Buffer Threshold Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 1 **TXFULLISE:** Transmit Buffer Full Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 0 **TXEMPTYISE:** Transmit Buffer Empty Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

NOTES:

26.2 Crypto Engine Buffer Descriptors

Host software creates a linked list of buffer descriptors and the hardware updates them. Table 26-3 provides a list of the Crypto Engine buffer descriptors, followed by format descriptions of each buffer descriptor (see Figure 26-2 through Figure 26-9).

TABLE 26-3: CRYPTO ENGINE BUFFER DESCRIPTORS

Name (see Note 1)		Bit 31/2315/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
BD_CTRL	31:24	DESC_EN	—	CRY_MODE<2:0>			—	—	—
	23:16	—	SA_FETCH_EN	—	—	LAST_BD	LIFM	PKT_INT_EN	CBD_INT_EN
	15:8	BD_BUFLEN<15:8>							
	7:0	BD_BUFLEN<7:0>							
BD_SA_ADDR	31:24	BD_SAADDR<31:24>							
	23:16	BD_SAADDR<23:16>							
	15:8	BD_SAADDR<15:8>							
	7:0	BD_SAADR<7:0>							
BD_SCRADDR	31:24	BD_SRCADDR<31:24>							
	23:16	BD_SRCADDR<23:16>							
	15:8	BD_SRCADDR<15:8>							
	7:0	BD_SRCADDR<7:0>							
BD_DSTADDR	31:24	BD_DSTADDR<31:24>							
	23:16	BD_DSTADDR<23:16>							
	15:8	BD_DSTADDR<15:8>							
	7:0	BD_DSTADDR<7:0>							
BD_NXTPTR	31:24	BD_NXTADDR<31:24>							
	23:16	BD_NXTADDR<23:16>							
	15:8	BD_NXTADDR<15:8>							
	7:0	BD_NXTADDR<7:0>							
BD_UPDPTR	31:24	BD_UPDADDR<31:24>							
	23:16	BD_UPDADDR<23:16>							
	15:8	BD_UPDADDR<15:8>							
	7:0	BD_UPDADDR<7:0>							
BD_MSG_LEN	31:24	MSG_LENGTH<31:24>							
	23:16	MSG_LENGTH<23:16>							
	15:8	MSG_LENGTH<15:8>							
	7:0	MSG_LENGTH<7:0>							
BD_ENC_OFF	31:24	ENCR_OFFSET<31:24>							
	23:16	ENCR_OFFSET<23:16>							
	15:8	ENCR_OFFSET<15:8>							
	7:0	ENCR_OFFSET<7:0>							

Note 1: The buffer descriptor must be allocated in memory on a 64-bit boundary.

TABLE 26-4: CRYPTO ENGINE SECURITY ASSOCIATION STRUCTURE (CONTINUED)

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SA_ENCIV1	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV2	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV3	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV4	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							

REGISTER 28-4: ADCTRGMODE: ADC TRIGGERING MODE FOR DEDICATED ADC REGISTER

bit 9 **STRGEN1:** ADC1 Presynchronized Triggers bit
1 = ADC1 uses presynchronized triggers
0 = ADC1 does not use presynchronized triggers

bit 8 **STRGEN0:** ADC0 Presynchronized Triggers bit
1 = ADC0 uses presynchronized triggers
0 = ADC0 does not use presynchronized triggers

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **SSAMPEN4:** ADC4 Synchronous Sampling bit
1 = ADC4 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC4 does not use synchronous sampling

bit 3 **SSAMPEN3:** ADC3 Synchronous Sampling bit
1 = ADC3 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC3 does not use synchronous sampling

bit 2 **SSAMPEN2:** ADC2Synchronous Sampling bit
1 = ADC2 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC2 does not use synchronous sampling

bit 1 **SSAMPEN1:** ADC1 Synchronous Sampling bit
1 = ADC1 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC1 does not use synchronous sampling

bit 0 **SSAMPEN0:** ADC0 Synchronous Sampling bit
1 = ADC0 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC0 does not use synchronous sampling

34.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 32. "Configuration"** (DS60001124) and **Section 33. "Programming and Diagnostics"** (DS60001129) in the *"PIC32 Family Reference Manual"*, which are available from the Microchip web site (www.microchip.com/PIC32).

PIC32MZ EF devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

- Flexible device configuration
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming™ (ICSP™)
- Internal temperature sensor

34.1 Configuration Bits

PIC32MZ EF devices contain two Boot Flash memories (Boot Flash 1 and Boot Flash 2), each with an associated configuration space. These configuration spaces can be programmed to contain various device configurations. Configuration space that is aliased by the Lower Boot Alias memory region is used to provide values for the following Configuration registers. See **4.1.1 "Boot Flash Sequence and Configuration Spaces"** for more information.

- DEVSIGN0/ADEVSIGN0: Device Signature Word 0 Register
- DEVCP0/ADEVCP0: Device Code-Protect 0 Register
- DEVCFG0/ADEVCFG0: Device Configuration Word 0
- DEVCFG1/ADEVCFG1: Device Configuration Word 1
- DEVCFG2/ADEVCFG2: Device Configuration Word 2
- DEVCFG3/ADEVCFG3: Device Configuration Word 3
- DEVADCx: Device ADC Calibration Word 'x' ('x' = 0-4, 7)

The following run-time programmable Configuration registers provide additional configuration control:

- CFGCON: Configuration Control Register
- CFGEBIA: External Bus Interface Address Pin Configuration Register
- CFGEBIC: External Bus Interface Control Pin Configuration Register
- CFGPG: Permission Group Configuration Register

In addition, the DEVID register provides device and revision information, the DEVADC0-DEVADC4 and DEVADC7 registers provide ADC module calibration/ configuration data, and the DEVSN0 and DEVSN1 registers contain a unique serial number of the device.

Note: Do not use Word program operation (NVMOP<3:0> = 0001) when programming the device Words that are described in this section.

REGISTER 34-5: DEVCFG2/ADEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	R/P	r-1	r-1	r-1	r-1	r-1	r-1
	—	UPLLFSEL	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P
	—	—	—	—	—	FPLLODIV<2:0>		
15:8	r-1	R/P	R/P	R/P	R/P	R/P	R/P	R/P
		FPLLMULT<6:0>						
7:0	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FPLLICLK	FPLLRNG<2:0>			—	FPLLIDIV<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** Write as '1'

bit 30 **UPLLFSEL:** USB PLL Input Frequency Select bit
1 = UPLL input clock is 24 MHz
0 = UPLL input clock is 12 MHz

bit 29-19 **Reserved:** Write as '1'

bit 18-16 **FPLLODIV<2:0>:** Default System PLL Output Divisor bits
111 = PLL output divided by 32
110 = PLL output divided by 32
101 = PLL output divided by 32
100 = PLL output divided by 16
011 = PLL output divided by 8
010 = PLL output divided by 4
001 = PLL output divided by 2
000 = PLL output divided by 2

bit 15 **Reserved:** Write as '1'

bit 14-8 **FPLLMULT<6:0>:** System PLL Feedback Divider bits
1111111 = Multiply by 128
1111110 = Multiply by 127
1111101 = Multiply by 126
1111100 = Multiply by 125
•
•
•
0000000 = Multiply by 1

bit 7 **FPLLICLK:** System PLL Input Clock Select bit
1 = FRC is selected as input to the System PLL
0 = POSC is selected as input to the System PLL

bit 6-4 **FPLLRNG<2:0>:** System PLL Divided Input Clock Frequency Range bits
111 = Reserved
110 = Reserved
101 = 34-64 MHz
100 = 21-42 MHz
011 = 13-26 MHz
010 = 8-16 MHz
001 = 5-10 MHz
000 = Bypass

TABLE 37-10: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
DI60a	IICL	**Input Low Injection Current**	0	—	-5(2,5)	mA	This parameter applies to all pins, with the exception of RB10. Maximum IICH current for this exception is 0 mA.
DI60b	IICH	**Input High Injection Current**	0	—	+5(3,4,5)	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, OSCI, OSCO, SOSCI, SOSCO, D+, D- and RB10. Maximum IICH current for these exceptions is 0 mA.
DI60c	∑IICT	**Total Input Injection Current (sum of all I/O and control pins)**	-20(6)	—	+20(6)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL + | IICH |) ≤ ∑IICT

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: VIL source < (VSS - 0.3). Characterized but not tested.

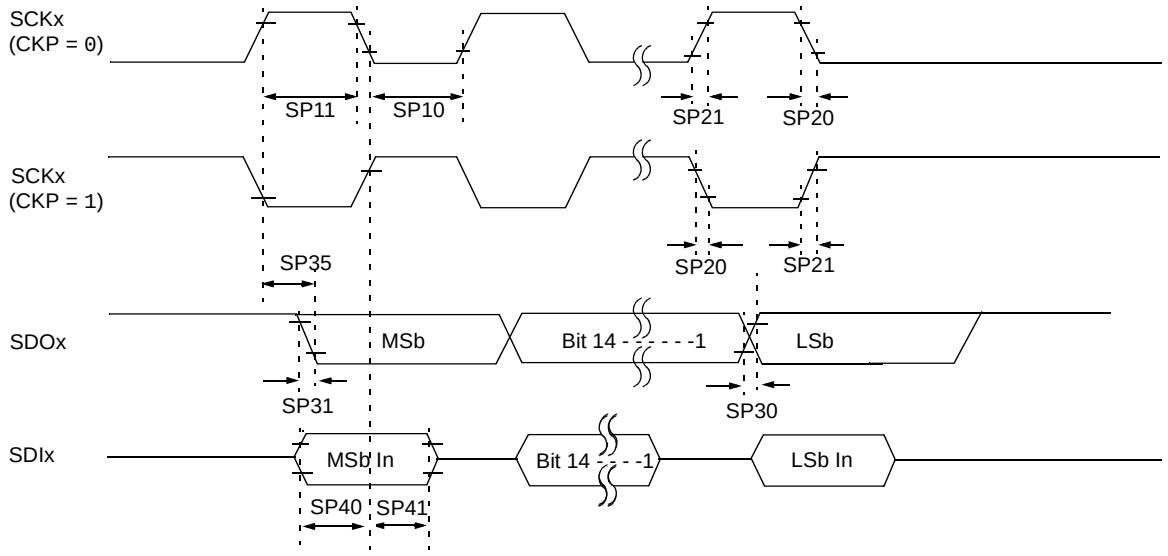
3: VIH source > (VDD + 0.3) for non-5V tolerant pins only.

4: Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any “positive” input injection current.

5: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

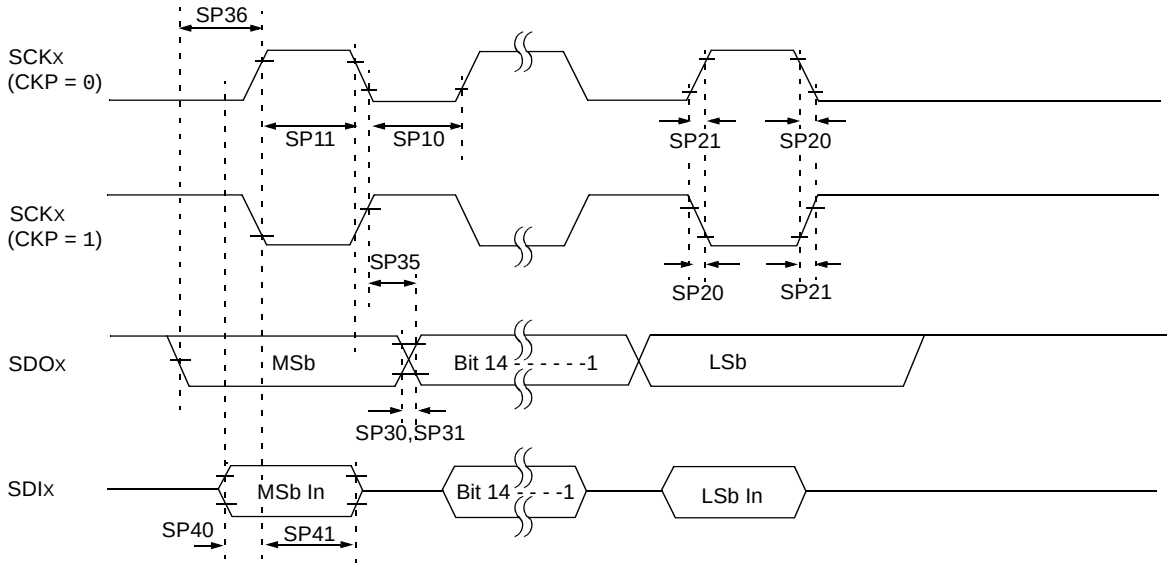
6: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. If **Note 2**, IICL = (((Vss - 0.3) - VIL source) / Rs). If **Note 3**, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

FIGURE 37-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 37-1 for load conditions.

FIGURE 37-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 37-1 for load conditions.

40.0 AC AND DC CHARACTERISTICS GRAPHS

Note: The graphs provided are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 40-1: VOH – 4x DRIVER PINS

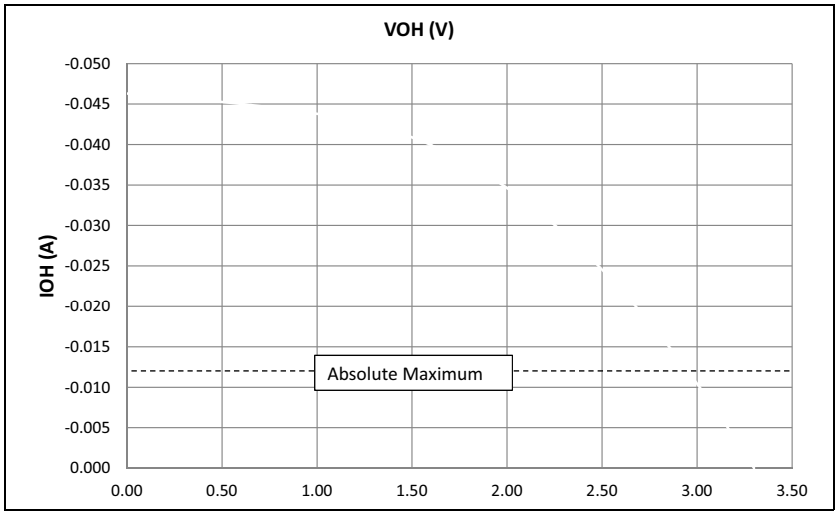


FIGURE 40-2: VOL – 4x DRIVER PINS

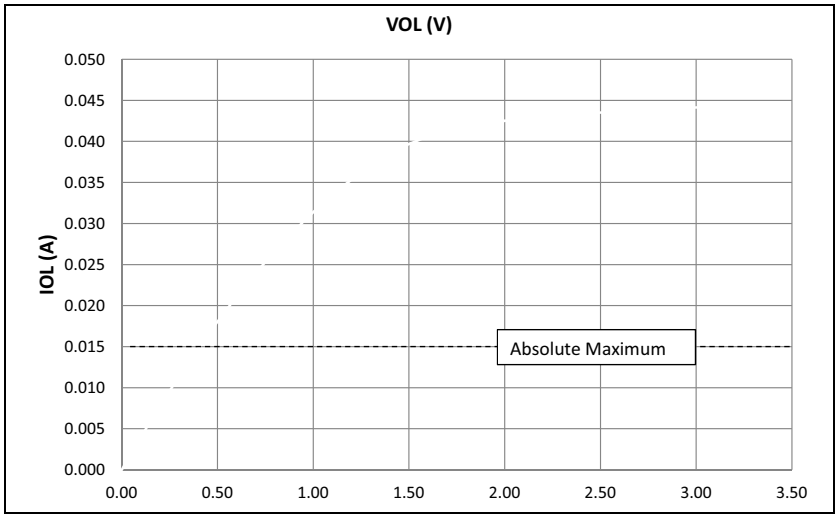


FIGURE 40-3: VOH – 8x DRIVER PINS

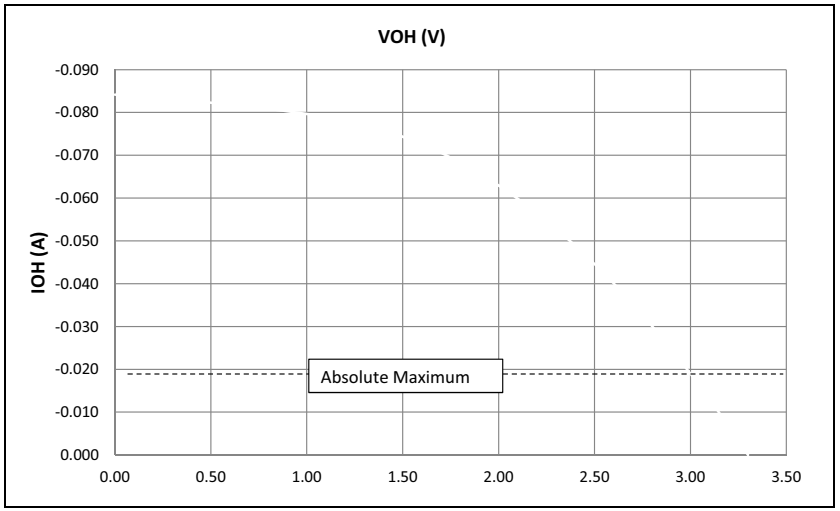
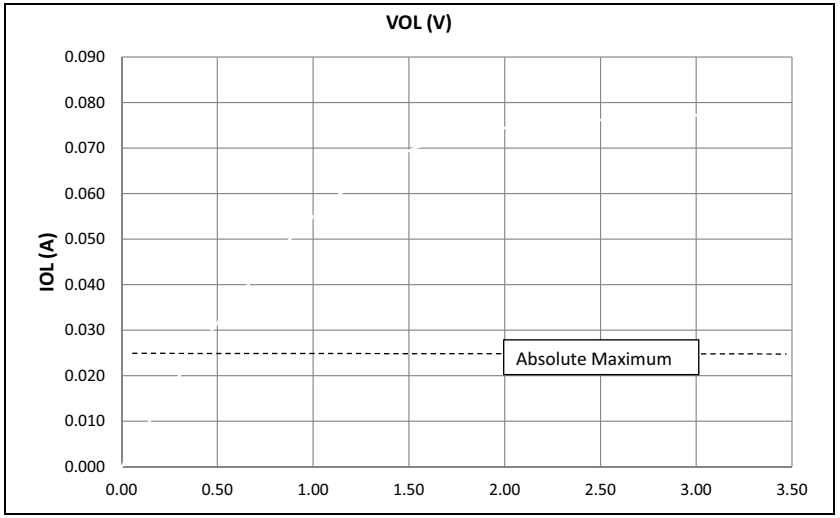
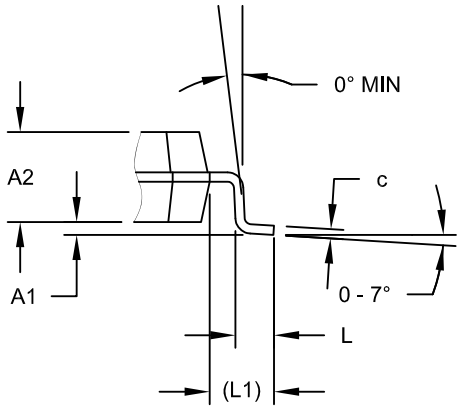


FIGURE 40-4: VOL – 8x DRIVER PINS

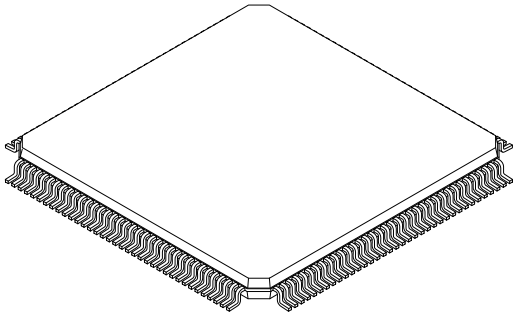


144-Lead Plastic Low Profile Quad Flatpack (PL) – 20x20x1.40 mm Body, with 2.00 mm Footprint [LQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		144	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.60
Molded Package Height	A2	1.35	1.40	1.45
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 (REF)		
Overall Width	E	22.00 BSC		
Overall Length	D	22.00 BSC		
Molded Body Width	E1	20.00 BSC		
Molded Body Length	D1	20.00 BSC		
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-044B Sheet 2 of 2

Revision C (March 2016)

In this revision, the Preliminary status was removed from the document footer.

The revision also includes the following major changes, which are referenced by their respective chapter in Table C-2. In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE C-2: MAJOR SECTION UPDATES

Section Name	Update Description
2.0 "Guidelines for Getting Started with 32-bit Microcontrollers"	**2.9.1.3 "EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations"** and Figure 2-5 were updated.
4.0 "Memory Organization"	The names of the Boot Flash Words were updated from BFxSEQ0 to BFxSEQ3 (see **4.1.1 "Boot Flash Sequence and Configuration Spaces"**). The ABFxSEQx registers were removed from the Boot Flash Sequence and Configuration tables (see Table 4-2 and Table 4-3).
7.0 "CPU Exceptions and Interrupt Controller"	The Cache Error exception type was removed from the MIPS32 M-Class Microprocessor Core Exception Types (see Table 7-1).
8.0 "Oscillator Configuration"	The PLLODIV<2:0> bit value settings were updated in the SPLLCON register (see Register 8-3).
12.0 "I/O Ports"	The SIDL bit was removed from the CNCONx registers (see Table 12-4 through Table 12-21 and Register 12-3).
20.0 "Serial Quad Interface (SQI)"	The following bits were removed from the SQI1XCON1 register (see Table 20-1 and Register 20-1): DDRDATA, DDRDUMMY, DDRMODE, DDRADDR, and DDRCMD. The DDRMODE bit was removed from the SQI1CON register (see Table 20-1 and Register 20-4).
28.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"	A note was added to the SELRES<1:0> bits in the ADCCON1 and ADCxTIME registers (see Register 28-1 and Register 28-27). The ADCID<2:0 bit values were updated in the ADCFSTAT register (see Register 28-22).
34.0 "Special Features"	The bit value definitions for the POSCGAIN<1:0> and SOSCGAIN<1:0> bits were updated (see Register 34-3). The Device ADC Calibration Word (DEVADCx) register was added (see Table 34-5 and Register 34-13).

TABLE C-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
37.0 "Electrical Characteristics"	The DC Characteristics: Operating Current (I_{DD}) and Note 6 were updated (see Table 37-6). The DC Characteristics: Idle Current (I_{IDLE}) and Note 4 were updated (see Table 37-7). Parameter DC40m and Note 5 in the DC Characteristics: Power-down Current (I_{PD}) were updated (see Table 37-8). Parameter DO50 (Cosco) was removed from the Capacitive Loading Requirements on Output Pins (see Table 37-16). The Internal FRC Accuracy and Internal LPRC conditions were updated for 125ºC (see Table 37-20 and Table 37-21). Parameter SP15 and Note 5 of the SPIx Module Master Mode Timing Requirements were updated (see Table 37-30 and Table 37-31). The Temperature Sensor Specifications were updated (see Table 37-41).
38.0 "Extended Temperature Electrical Characteristics"	New chapter for Extended Temperature devices was added.
39.0 "AC and DC Characteristics Graphs"	The Typical Temperature Sensor Voltage graph was updated (see Figure 39-7).
40.0 "Packaging Information"	The package drawings and land pattern for the 64-Lead Plastic Quad Flat, No Lead Package (MR) were updated.
Appendix A: "Migrating from PIC32MX5XX/6XX/7XX to PIC32MZ EF"	The Primary Oscillator Configuration section in the Oscillator Configuration Differences was updated (see Table A-1).
Appendix B: "Migrating from PIC32MZ EC to PIC32MZ EF"	Boot Flashing aliasing was updated for PIC32MZ EF devices (see Table B-4).