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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	MIDS32@ M Class
Core Processor	
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TFBGA
Supplier Device Package	144-TFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512eff144-e-jwx

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The System Bus arbitration scheme implements a nonprogrammable, Least Recently Serviced (LRS) priority, which provides Quality Of Service (QOS) for most initiators. However, some initiators can use Fixed High Priority (HIGH) arbitration to guarantee their access to data.

The arbitration scheme for the available initiators is shown in Table 4-5.

Name	ID	QOS
CPU	1	LRS <sup>(1)</sup>
CPU	2	HIGH <sup>(1,2)</sup>
DMA Read	3	LRS <sup>(1)</sup>
DMA Read	4	HIGH <sup>(1,2)</sup>
DMA Write	5	LRS <sup>(1)</sup>
DMA Write	6	HIGH <sup>(1,2)</sup>
USB	7	LRS
Ethernet Read	8	LRS
Ethernet Write	9	LRS
CAN1	10	LRS
CAN2	11	LRS
SQI1	12	LRS
Flash Controller	13	HIGH <sup>(2)</sup>
Crypto	14	LRS

TABLE 4-5:INITIATOR ID AND QOS

- Note 1: When accessing SRAM, the DMAPRI bit (CFGCON<25>) and the CPUPRI bit (CFGCON<24>) provide arbitration control for the DMA and CPU (when servicing an interrupt (i.e., EXL = 1)), respectively, by selecting the use of LRS or HIGH When using HIGH, the DMA and CPU get arbitration preference over all initiators using LRS.
  - 2: Using HIGH arbitration can have serious negative effects on other initiators. Therefore, it is recommended to not enable this type of arbitration for an initiator that uses significant system bandwidth. HIGH arbitration is intended to be used for low bandwidth applications that require low latency, such as LCC graphics applications.

## 4.3 Permission Access and System Bus Registers

The System Bus on PIC32MZ EF family of microcontrollers provides access control capabilities for the transaction initiators on the System Bus.

The System Bus divides the entire memory space into fourteen target regions and permits access to each target by initiators via permission groups. Four Permission Groups (0 through 3) can be assigned to each initiator. Each permission group is independent of the others and can have exclusive or shared access to a region.

Using the CFGPG register (see Register 34-10 in **Section 34.0 "Special Features"**), Boot firmware can assign a permission group to each initiator, which can make requests on the System Bus.

The available targets and their regions, as well as the associated control registers to assign protection, are described and listed in Table 4-6.

Register 4-2 through Register 4-10 are used for setting and controlling access permission groups and regions.

To change these registers, they must be unlocked in hardware. The register lock is controlled by the PGLOCK Configuration bit (CFGCON<11>). Setting PGLOCK prevents writes to the control registers; clearing PGLOCK allows writes.

To set or clear the PGLOCK bit, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** in the *"PIC32 Family Reference Manual"* for details.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0	U-0
31:24	—	—	—	—	PFMDED	PFMSEC		—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—		—
15.9	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.6	—	—	—	—	—	—		—
7:0	R/W-0, HS	R/W-0, HS	R/W-0, HS					
7.0				PFMSEC	CNT<7:0>			

## REGISTER 9-2: PRESTAT: PREFETCH MODULE STATUS REGISTER

Legend:		HS = Hardware Set		
R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-28 Unimplemented: Read as '0'

- bit 27 **PFMDED:** Flash Double-bit Error Detected (DED) Status bit
  This bit is set in hardware and can only be cleared (i.e., set to '0') in software.
  1 = A DED error has occurred
  - 0 = A DED error has not occurred
- bit 26 **PFMSEC:** Flash Single-bit Error Corrected (SEC) Status bit 1 = A SEC error occurred when PFMSECCNT<7:0> was equal to zero 0 = A SEC error has not occurred
- bit 25-8 Unimplemented: Read as '0'
- bit 7-0 **PFMSECCNT<7:0>:** Flash SEC Count bits 11111111 - 00000000 = SEC count

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0		
31.24		VPLEN<7:0>								
22.16	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0		
23.10	WTCON<3:0>				WTID<3:0>					
15.0	R-1	R-0	R-0	R-0	R-1	R-1	R-0	R-0		
15.0	DMACHANS<3:0>				RAMBITS<3:0>					
7.0	R-0	R-1	R-1	R-1	R-0	R-1	R-1	R-1		
7:0	RXENDPTS<3:0>				TXENDPTS<3:0>					

#### **REGISTER 11-16: USBINFO: USB INFORMATION REGISTER**

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 VPLEN<7:0>: VBUS pulsing charge length bits Sets the duration of the VBUS pulsing charge in units of 546.1 µs. (The default setting corresponds to 32.77 ms.)

bit 23-20 WTCON<3:0>: Connect/Disconnect filter control bits

Sets the wait to be applied to allow for the connect/disconnect filter in units of 533.3 ns. The default setting corresponds to 2.667  $\mu$ s.

- bit 19-6 WTID<3:0>: ID delay valid control bits Sets the delay to be applied from IDPULLUP being asserted to IDDIG being considered valid in units of 4.369ms. The default setting corresponds to 52.43ms.
- bit 15-12 DMACHANS<3:0>: DMA Channels bits These read-only bits provide the number of DMA channels in the USB module. For the PIC32MZ EF family, this number is 8.
- bit 11-8 **RAMBITS<3:0>:** RAM address bus width bits These read-only bits provide the width of the RAM address bus. For the PIC32MZ EF family, this number is 12.
- bit 7-4 RXENDPTS<3:0>: Included RX Endpoints bits

This read-only register gives the number of RX endpoints in the design. For the PIC32MZ EF family, this number is 7.

bit 3-0 **TXENDPTS<3:0>:** Included TX Endpoints bits

These read-only bits provide the number of TX endpoints in the design. For the PIC32MZ EF family, this number is 7.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	
31:24	—	—	—	—	—	—	NRSTX	NRST	
00.40	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R.W-0	R/W-1	R/W-0	
23.10	LSEOF<7:0>								
15.0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R.W-1	R/W-1	R/W-1	
15:8	FSEOF<7:0>								
7.0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R.W-0	R/W-0	R/W-0	
7.0				HSEO	F<7:0>				

#### REGISTER 11-17: USBEOFRST: USB END-OF-FRAME/SOFT RESET CONTROL REGISTER

## Legend:

3			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-26 Unimplemented: Read as '0'

- bit 25 NRSTX: Reset of XCLK Domain bit
  - 1 = Reset the XCLK domain, which is clock recovered from the received data by the PHY 0 = Normal operation

#### bit 24 NRST: Reset of CLK Domain bit

1 = Reset the CLK domain, which is clock recovered from the peripheral bus

0 = Normal operation

bit 23-16 LSEOF<7:0>: Low-Speed EOF bits These bits set the Low-Speed transaction in units of 1.067 μs (default setting is 121.6 μs) prior to the EOF to stop new transactions from beginning.

# bit 15-8 **FSEOF<7:0>:** Full-Speed EOF bits These bits set the Full-Speed transaction in units of 533.3 µs (default setting is 63.46 µs) prior to the EOF to stop new transactions from beginning.

#### bit 7-0 **HSEOF<7:0>:** Hi-Speed EOF bits These bits set the Hi-Speed transaction in units of 133.3 µs (default setting is 17.07µs) prior to the EOF to stop new transactions from beginning.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	-	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	-	—	—
45.0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
15:8	ON	—	—	—	EDGEDETECT	-	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
		_						

## REGISTER 12-3: CNCONX: CHANGE NOTICE CONTROL FOR PORTX REGISTER (X = A - K)

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read a	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-16 Unimplemented: Read as '0'

bit 15 **ON:** Change Notice (CN) Control ON bit

1 = CN is enabled

0 = CN is disabled

#### bit 14-12 Unimplemented: Read as '0'

- bit 11 EDGEDETECT: Change Notification Style bit
  - 1 = Edge Style. Detect edge transitions (CNFx used for CN Event).
  - 0 = Mismatch Style. Detect change from last PORTx read (CNSTATx used for CN Event).
- bit 10-0 Unimplemented: Read as '0'

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—		—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	—	—	—	—	DMAEISE	PKT DONEISE	BD DONEISE	CON THRISE
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	CON EMPTYISE	CON FULLISE	RX THRISE	RX FULLISE	RX EMPTYISE	TX THRISE	TX FULLISE	TX EMPTYISE

## REGISTER 20-22: SQI1INTSIGEN: SQI INTERRUPT SIGNAL ENABLE REGISTER

## Legend:

· J · · ·						
R = Readable bit	= Readable bit W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

#### bit 31-12 Unimplemented: Read as '0'

bit 11	DMAEISE: DMA Bus Error Interrupt Signal Enable bit
	1 = Interrupt signal is enabled
	0 = Interrupt signal is disabled
bit 10	PKTDONEISE: Receive Error Interrupt Signal Enable bit
	1 = Interrupt signal is enabled
	0 = Interrupt signal is disabled
bit 9	BDDONEISE: Transmit Error Interrupt Signal Enable bit
	1 = Interrupt signal is enabled
	0 = Interrupt signal is disabled
bit 8	<b>CONTHRISE:</b> Control Buffer Threshold Interrupt Signal Enable bit
	1 = Interrupt signal is enabled
	0 = Interrupt signal is disabled
bit 7	CONEMPTYISE: Control Buffer Empty Interrupt Signal Enable bit
	1 = Interrupt signal is enabled
1.11.0	
DIT 6	CONFULLISE: Control Buffer Full Interrupt Signal Enable bit
	1 = Interrupt signal is enabled
hit E	0 = Interrupt Signal is disabled
DIL D	1 – Interrupt signal is onabled
	$\Omega = $ Interrupt signal is disabled
hit 4	<b>BXFULLISE:</b> Receive Buffer Full Interrunt Signal Enable bit
	1 = Interrupt signal is enabled
	0 = Interrupt signal is disabled
bit 3	<b>RXEMPTYISE:</b> Receive Buffer Empty Interrupt Signal Enable bit
	1 = Interrupt signal is enabled
	0 = Interrupt signal is disabled
bit 2	TXTHRISE: Transmit Buffer Threshold Interrupt Signal Enable bit
	1 = Interrupt signal is enabled
	0 = Interrupt signal is disabled
bit 1	TXFULLISE: Transmit Buffer Full Interrupt Signal Enable bit
	1 = Interrupt signal is enabled
	0 = Interrupt signal is disabled
bit 0	<b>TXEMPTYISE:</b> Transmit Buffer Empty Interrupt Signal Enable bit
	1 = Interrupt signal is enabled
	0 = Interrupt signal is disabled

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31.24		—	—	INIT1SCHECK	INIT1CO	UNT<1:0>	INIT1TY	INIT1TYPE<1:0>	
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23:16	INIT1CMD3<7:0> <sup>(1)</sup>								
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15:8	INIT1CMD2<7:0> <sup>(1)</sup>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
		INIT1CMD1<7:0> <sup>(1)</sup>							

#### REGISTER 20-25: SQI1XCON3: SQI XIP CONTROL REGISTER 3

## Legend:

3				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

#### bit 31-29 Unimplemented: Read as '0'

- bit 28 INIT1SCHECK: Flash Initialization 1 Command Status Check bit
  - 1 = Check the status after executing the INIT1 command
  - 0 = Do not check the status

#### bit 27-26 INIT1COUNT<1:0>: Flash Initialization 1 Command Count bits

- 11 = INIT1CMD1, INIT1CMD2, and INIT1CMD3 are sent
- 10 = INIT1CMD1 and INIT1CMD2 are sent, but INIT1CMD3 is still pending
- 01 = INIT1CMD1 is sent, but INIT1CMD2 and INIT1CMD3 are still pending
- 00 = No commands are sent

#### bit 25-24 INIT1TYPE<1:0>: Flash Initialization 1 Command Type bits

- 11 = Reserved
- 10 = INIT1 commands are sent in Quad Lane mode
- 01 = INIT1 commands are sent in Dual Lane mode
- 00 = INIT1 commands are sent in Single Lane mode
- bit 24-16 **INIT1CMD3<7:0>:** Flash Initialization Command 3 bits<sup>(1)</sup> Third command of the Flash initialization.
- bit 15-8 **INIT1CMD2<7:0>:** Flash Initialization Command 2 bits<sup>(1)</sup> Second command of the Flash initialization.
- bit 7-0 **INIT1CMD1<7:0>:** Flash Initialization Command 1 bits<sup>(1)</sup> First command of the Flash initialization.
- **Note 1:** INIT1CMD1 can be WEN and INIT1CMD2 can be SECTOR UNPROTECT.

**Note:** Some Flash devices require Write Enable and Sector Unprotect commands before read/write operations and this register is useful in working with those Flash types (XIP mode only)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	—	—	—	—	—	—	—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	—	—	—	—	—	—	—	—		
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	CS2 <sup>(1)</sup>	CS1 <sup>(3)</sup>		ADDR<13:8>						
	ADDR15 <sup>(2)</sup>	ADDR14 <sup>(4)</sup>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	ADDR<7:0>									

#### REGISTER 23-3: PMADDR: PARALLEL PORT ADDRESS REGISTER

#### Legend:

bit 15

- 3				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

#### bit 31-16 Unimplemented: Read as '0'

- bit 15 CS2: Chip Select 2 bit<sup>(1)</sup>
  - 1 = Chip Select 2 is active
  - 0 = Chip Select 2 is inactive
  - ADDR<15>: Target Address bit 15<sup>(2)</sup>
- bit 14 CS1: Chip Select 1 bit<sup>(3)</sup>
  - 1 = Chip Select 1 is active 0 = Chip Select 1 is inactive
- bit 14 ADDR<14>: Target Address bit 14<sup>(4)</sup>
- bit 13-0 ADDR<13:0>: Address bits
- Note 1: When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.
  - **2:** When the CSF<1:0> bits (PMCON<7:6>) = 00.
  - **3:** When the CSF<1:0> bits (PMCON<7:6>) = 10.
  - **4:** When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

**Note:** If the DUALBUF bit (PMCON<17>) = 0, the bits in this register control both read and write target addressing. If the DUALBUF bit = 1, the bits in this register are not used. In this instance, use the PMRADDR register for Read operations and the PMWADDR register for Write operations.

## 25.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 29. "Real-Time Calendar Clock and (RTCC)" (DS60001125) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Lowpower optimization provides extended battery lifetime while keeping track of time. The following are key features of the RTCC module:

- · Time: hours, minutes, and seconds
- 24-hour format (military time)
- · Visibility of one-half second period
- Provides calendar: Weekday, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month, and one year
- · Alarm repeat with decrementing counter
- · Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- · BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Uses external 32.768 kHz crystal or 32 kHz internal oscillator
- Alarm pulse, seconds clock, or internal clock output on RTCC pin



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Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
04.04	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
31:24	—	—	—	TRGSRC7<4:0>						
00.40	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23.10	—	—	—	TRGSRC6<4:0>						
45.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	—	—	—	TRGSRC5<4:0>						
7.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7:0		_			TRGSRC4<4:0>					

#### REGISTER 28-18: ADCTRG2: ADC TRIGGER SOURCE 2 REGISTER

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-29 Unimplemented: Read as '0'

bit 28-24 TRGSRC7<4:0>: Trigger Source for Conversion of Analog Input AN7 Select bits

```
11111 = Reserved

.

.

01101 = Reserved

01100 = Comparator 2 (COUT)

01011 = Comparator 1 (COUT)

01010 = OCMP5

01001 = OCMP3

01000 = OCMP1

00111 = TMR5 match

00101 = TMR3 match

00101 = TMR1 match

00101 = TMR1 match

00101 = STRIG

00011 = STRIG

00010 = Global level software trigger (GLSWTRG)

00001 = Global software edge Trigger (GSWTRG)

00000 = No Trigger
```

For STRIG, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSS*x* registers.

- bit 23-21 Unimplemented: Read as '0'
- bit 20-16 **TRGSRC6<4:0>:** Trigger Source for Conversion of Analog Input AN6 Select bits See bits 28-24 for bit value definitions.
- bit 15-13 Unimplemented: Read as '0'
- bit 12-8 **TRGSRC5<4:0>:** Trigger Source for Conversion of Analog Input AN5 Select bits See bits 28-24 for bit value definitions.
- bit 7-5 Unimplemented: Read as '0'
- bit 4-0 **TRGSRC4<4:0>:** Trigger Source for Conversion of Analog Input AN4 Select bits See bits 28-24 for bit value definitions.

# REGISTER 28-21: ADCCMPCONx: ADC DIGITAL COMPARATOR 'x' CONTROL REGISTER ('x' = 2 THROUGH 6) (CONTINUED)

- bit 1 IELOHI: Low/High Digital Comparator 'x' Event bit
  - 1 = Generate a Digital Comparator 'x' Event when the DCMPLO<15:0> bits ≤ DATA<31:0> bits
  - 0 = Do not generate an event
- bit 0 IELOLO: Low/Low Digital Comparator 'x' Event bit
  - 1 = Generate a Digital Comparator 'x' Event when the DATA<31:0> bits < DCMPLO<15:0> bits
  - 0 = Do not generate an event

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	—	_					
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—		_				
	R/W-1	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	SOFT	SIM			RESET	RESET	RESET	RESET
	RESET	RESET	_		RMCS	RFUN	TMCS	TFUN
	U-0	U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1
7:0			_	LOOPBACK	TX PAUSE	RX PAUSE	PASSALL	RX ENABLE

## REGISTER 30-23: EMAC1CFG1: ETHERNET CONTROLLER MAC CONFIGURATION 1 REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

## bit 31-16 Unimplemented: Read as '0'

bit 15	SOFTRESET: Soft Reset bit
	Setting this bit will put the MACMII in reset. Its default value is '1'.
bit 14	SIMRESET: Simulation Reset bit
	Setting this bit will cause a reset to the random number generator within the Transmit Function.
bit 13-12	Unimplemented: Read as '0'
bit 11	RESETRMCS: Reset MCS/RX bit
	Setting this bit will put the MAC Control Sub-layer/Receive domain logic in reset.
bit 10	RESETRFUN: Reset RX Function bit
	Setting this bit will put the MAC Receive function logic in reset.
bit 9	RESETTMCS: Reset MCS/TX bit
	Setting this bit will put the MAC Control Sub-layer/TX domain logic in reset.
bit 8	RESETTFUN: Reset TX Function bit
	Setting this bit will put the MAC Transmit function logic in reset.
bit 7-5	Unimplemented: Read as '0'
bit 4	LOOPBACK: MAC Loopback mode bit
	<ul> <li>1 = MAC Transmit interface is loop backed to the MAC Receive interface</li> <li>0 = MAC normal operation</li> </ul>
bit 3	TXPAUSE: MAC TX Flow Control bit
	<ul> <li>1 = PAUSE Flow Control frames are allowed to be transmitted</li> <li>0 = PAUSE Flow Control frames are blocked</li> </ul>
bit 2	RXPAUSE: MAC RX Flow Control bit
	<ul><li>1 = The MAC acts upon received PAUSE Flow Control frames</li><li>0 = Received PAUSE Flow Control frames are ignored</li></ul>
bit 1	PASSALL: MAC Pass all Receive Frames bit
	<ul><li>1 = The MAC will accept all frames regardless of type (Normal vs. Control)</li><li>0 = The received Control frames are ignored</li></ul>
bit 0	RXENABLE: MAC Receive Enable bit
	<ul><li>1 = Enable the MAC receiving of frames</li><li>0 = Disable the MAC receiving of frames</li></ul>

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

#### 31.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 19. "Comparator" (DS60001110) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The Analog Comparator module consists of two comparators that can be configured in a variety of ways.

The following are key features of the Analog Comparator module:

- Differential inputs
- Rail-to-rail operation
- Selectable output polarity
- Selectable inputs:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference
  - Comparator voltage reference (CVREF)
- Selectable interrupt generation

A block diagram of the comparator module is illustrated in Figure 31-1.



#### **FIGURE 31-1:** COMPARATOR BLOCK DIAGRAM

# 32.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

Note:	This data sheet summarizes the
	features of the PIC32MZ EF family of
	devices. It is not intended to be a
	comprehensive reference source. To
	complement the information in this data
	sheet, refer to Section 20. "Comparator
	Voltage Reference (CVREF)"
	(DS60001109) in the "PIC32 Family
	Reference Manual", which is available
	from the Microchip web site
	(www.microchip.com/PIC32).

The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The comparator voltage reference has the following features:

- High and low range selection
- · Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- · Output can be connected to a pin

A block diagram of the CVREF module is illustrated in Figure 32-1.





AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial				
Param. No.SymbolCharacteristicsMinimumTypical			Typical	Maximum	Units	Conditions	
OS51	Fsys	System Frequency	DC		200	MHz	USB module disabled
			60		200	MHz	USB module enabled
OS55a	Fpb	Peripheral Bus Frequency	DC	_	100	MHz	For PBCLKx, 'x' $\neq$ 4, 7
OS55b			DC		200	MHz	For PBCLK4, PBCLK7
OS56	Fref	Reference Clock Frequency	_	_	50	MHz	For REFCLKI1, 3, 4 and REFCLKO1, 3, 4 pins

## TABLE 37-18: SYSTEM TIMING REQUIREMENTS

## TABLE 37-19: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.1V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param. No.	Symbol	Characteristics <sup>(1)</sup>		Min.	Typical	Max.	Units	Conditions
OS50	Fin	PLL Input Frequency Range		5		64	MHz	ECPLL, HSPLL, FRCPLL modes
OS52	TLOCK	PLL Start-up Time (Lock Time)		_		100	μs	—
OS53	DCLK	CLKO Stability <sup>(2)</sup> (Period Jitter or Cumulative)		-0.25		+0.25	%	Measured over 100 ms period
OS54	FVco	PLL Vco Frequency Range		350	_	700	MHz	—
OS54a	FPLL	PLL Output Frequency Range		10	_	200	MHz	_

**Note 1:** These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{PBCLK2}{\sqrt{CommunicationClock}}}}$$

For example, if PBCLK2 = 100 MHz and SPI bit rate = 50 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{100}{50}}} = \frac{D_{CLK}}{1.41}$$

AC CHARACTERISTICS			Standard Oper (unless otherv Operating temp	Standard Operating Conditions: 2.1V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param. No.	Symbol	Characteristics <sup>(2)</sup>		Min.	Тур. <sup>(1)</sup>	Max.	Units	Conditions	
DO32	<sup>132</sup> TIOF <b>Port Output Fall Time</b> I/O Pins: 4x Source Driver Pins - RA3, RA9, RA10, RA14, RA15 RB0-RB2, RB4, RB6-RB7, RB11, RB13		_	_	9.5	ns	CLOAD = 50 pF		
RC12-RC15 RD0, RD6-RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8 RG15 RH0, RH1, RH4-RH6, RH8-RH13 RJ0-RJ2, RJ8, RJ9, RJ11 <b>Port Output Fall Time</b> I/O Pins: 8x Source Driver Pins - RA0-RA2, RA4, RA5 RB3, RB5, RB8-RB10, RB12, RB14, RB15 RC1-RC4		1, RD14 , RH8-RH13 RJ11	_	_	6	ns	Cload = 20 pF		
		<b>e</b> : - ), RB12, RB14,		_	8	ns	CLOAD = 50 pF		
		RD1-RD5, RD9, RD10 RD15 RE4-RE7 RF0, RF4, RF5, RF12 RG0, RG1, RG6-RG9 RH2, RH3, RH7, RH1 RJ3-RJ7, RJ10, RJ12 RK0-RK7	0, RD12, RD13, 2, RF13 4, RH15 2-RJ15	_	_	6	ns	Cload = 20 pF	
		Port Output Fall Tim I/O Pins: 12x Source Driver Pin RA6 RA7	<b>e</b> 15 -	_	_	3.5	ns	Cload = 50 pF	
		RE0-RE3 RF1 RG12-RG14		_	_	2	ns	CLOAD = 20 pF	
DI35	TINP	INTx Pin High or Low Time		5	—	—	ns	—	
DI40	Trbp	CNx High or Low Time	e (input)	5	—	—	ns	—	

## TABLE 37-23: I/O TIMING REQUIREMENTS (CONTINUED)

**Note 1:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: This parameter is characterized, but not tested in manufacturing.

## 124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Number of Pins	N		124		
Pitch	eT	0.50 BSC			
Pitch (Inner to outer terminal ring)	eR	0.50 BSC			
Overall Height	A	0.80	0.85	0.90	
Standoff	A1	0.00	-	0.05	
Overall Width	E		9.00 BSC		
Exposed Pad Width	E2	6.40	6.55	6.70	
Overall Length	D		9.00 BSC		
Exposed Pad Length	D2	6.40	6.55	6.70	
Contact Width	b	0.20	0.25	0.30	
Contact Length	L	0.20	0.25	0.30	
Contact-to-Exposed Pad	K	0.20	-	-	

#### Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-193A Sheet 2 of 2

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature				
Crystal/Oscillator Selection for USB					
Any frequency that can be divided down to 4 MHz using UPLLIDIV, including 4, 8, 12, 16, 20, 40, and 48 MHz.	If the USB module is used, the Primary Oscillator is limited to either 12 MHz or 24 MHz. Which frequency is used is selected using the UPLLFSEL (DEVCFG2<30>) bit.				
USB PLL Configuration					
On PIC32MX devices, the PLL for the USB requires an input fre- quency of 4 MHz.	On PIC32MZ EF devices, the HS USB PHY requires an input frequency of 12 MHz or 24 MHz. UPLLIDIV has been replaced with UPLLFSEL.				
UPLLIDIV<2:0> (DEVCFG2<10:8>) 111 = 12x divider 110 = 10x divider 101 = 6x divider 101 = 5x divider 011 = 4x divider 010 = 3x divider 010 = 3x divider 001 = 2x divider 000 = 1x divider	UPLLFSEL (DEVCFG2<30>) 1 = UPLL input clock is 24 MHz 0 = UPLL input clock is 12 MHz				
Peripheral Bus C	ock Configuration				
On PIC32MX devices, there is one peripheral bus, and the clock for that bus is divided from the SYSCLK using FPBDIV/PBDIV. In addition, the maximum PBCLK frequency is the same as SYSCLK. FPBDIV<1:0> (DEVCFG1<5:4>) PBDIV<1:0> (OSCCON<20:19>) 11 = PBCLK is SYSCLK divided by 8 10 = PBCLK is SYSCLK divided by 4 01 = PBCLK is SYSCLK divided by 2 00 = PBCLK is SYSCLK divided by 1	On PIC32MZ EF devices, there are eight peripheral buses with their own clocks. FPBDIV is removed, and each PBDIV is in its own register for each PBCLK. The initial PBCLK speed is fixed at reset, and the maximum PBCLK speed is limited to100 MHz for all buses, with the exception of PBCLK7, which is 200 MHz. PBDIV<6:0> (PBxDIV<6:0>) 1111111 = PBCLKx is SYSCLK divided by 128 1111110 = PBCLKx is SYSCLK divided by 127 • • • • • • • • • • • • • • • • • • •				
	(default value for x < 7) 0000000 = PBCLKx is SYSCLK divided by 1				
	(default value for x ≥ 7)				
CPU Clock (	Configuration				
	Dir Fieszwiz er devices, tile OPU clock is derived from PBCLK7.				
On PIC32MX devices, the default value for FRCDIV was to divide the FRC clock by two.	On PIC32MZ EF devices, the default has been changed to divide by one.				
FRCDIV<2:0> (OSCCON<26:24>) 111 = FRC divided by 256 110 = FRC divided by 64 101 = FRC divided by 32 100 = FRC divided by 16 011 = FRC divided by 8 010 = FRC divided by 4 001 = FRC divided by 2 (default) 000 = FRC divided by 1	FRCDIV<2:0> (OSCCON<26:24>) 111 = FRC divided by 256 110 = FRC divided by 64 101 = FRC divided by 32 100 = FRC divided by 16 011 = FRC divided by 8 010 = FRC divided by 4 001 = FRC divided by 2 000 = FRC divided by 1 (default)				

## TABLE A-1: OSCILLATOR CONFIGURATION DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature				
Scan Trigger Source					
On PIC32MX devices, there are four sources that can trigger a scan conversion in the ADC module: Auto, Timer3, INT0, and clearing the SAMP bit.	On PIC32MZ EF devices, the list of sources for triggering a scan conversion has been expanded to include the comparators, Output Compare, and two additional Timers. In addition, trigger sources can be simulated by setting the RQCNVRT (ADCCON3<8) bit.				
SSRC<2:0> (AD1CON1<7:5>) 111 = Auto convert 110 = Reserved 101 = Reserved 010 = Reserved 011 = Reserved 010 = Timer3 period match 001 = Active transition on INT0 pin 000 = Clearing SAMP bit	STRGSRC<4:0> (ADCCON1<20:16>) 11111 = Reserved • • • • • • • • • • • • •				
	00000 = No trigger				
On PIC32MX devices, the output format was decided for all ADC channels based on the setting of the FORM<2:0> bits.	On PIC32MZ EF devices, the FRACT bit determines whether fractional or integer format is used. Then, each input can have its own setting for input (differential or single-ended) and sign (signed or unsigned) using the DIFFx and SIGNx bits in the ADCIMODx registers.				
FORM<2:0> (AD1CON1<10:8>) 011 = Signed Fractional 16-bit 010 = Fractional 16-bit 001 = Signed Integer 16-bit 000 = Integer 16-bit 111 = Signed Fractional 32-bit 110 = Fractional 32-bit 101 = Signed Integer 32-bit 100 = Integer 32-bit	FRACT (ADCCON1<23>) 1 = Fractional 0 = Integer DIFFx (ADCIMODy) 1 = Channel x is using Differential mode 0 = Channel x is using Single-ended mode SIGNx (ADCMODy) 1 = Channel x is using Signed Data mode 0 = Channel x is using Unsigned Data mode				
Interrupts					
On PIC32MX devices, an interrupt is triggered from the ADC module when a certain number of conversions have taken place, irrespective of which channel was converted.	On PIC32MZ EF devices, the ADC module can trigger an inter- rupt for each channel when it is converted. Use the Interrupt Con- troller bits, IEC1<31:27>, IEC2<31:0>, and IEC3<7:0>, to enable/ disable them. In addition, the ADC support one global interrupt to indicate conversion on any number of channels.				
<pre>SMPI&lt;3:0&gt; (AD1CON2&lt;5:2&gt;) 1111 = Interrupt for each 16th sample/convert sequence 1110 = Interrupt for each 15th sample/convert sequence</pre>	AGIENxx (ADCGIRQENx <y>) 1 = Data ready event will generate a Global ADC interrupt 0 = No global interrupt In addition, interrupts can be generated for filter and comparator events.</y>				

# TABLE A-3: ADC DIFFERENCES (CONTINUED)

#### APPENDIX C: **REVISION HISTORY**

## **Revision A (January 2015)**

This is the initial released version of the document.

## **Revision B (July 2015)**

The document status was updated from Advance Information to Preliminary.

The revision includes the following major changes, which are referenced by their respective chapter in Table C-1.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE C-1: MAJOR SECTION UPDATES					
Section Name	Update Description				
32-bit MCUs (up to 2 MB Live- Update Flash and 512 KB SRAM) with FPU, Audio and Graphics Interfaces, HS USB, Ethernet, and Advanced Analog	The Operating Conditions were updated to: 2.1V to 3.6V.				
4.0 "Memory Organization"	Legal information on the System Bus was added (see <b>4.2</b> "System Bus Arbitration").				
5.0 "Flash Program Memory"	The BOOTSWAP bit in the NVMCON register was changed to: BFSWAP (see Register 5-1).				
6.0 "Resets"	The NVMLTA bit was removed from the RCON register (see Register 6-1).				
	The GNMI bit was added to the RNMICON register (see Register 6-3).				
7.0 "CPU Exceptions and	The ADC FIFO Data Ready Interrupt, IRQ 45, was added (see Table 7-2).				
Interrupt Controller"	ADC FIFO bits were added, and Note 7 regarding devices without a Crypto module was added to the Interrupt Register Map (see Table 7-3).				
	The NMIKEY<7:0> bits were added to the INTCON register (see Register 7-1)				
8.0 "Oscillator Configuration"	The SPLLRDY bit was removed and the SPLLDIVRDY bit was added to the CLKSTAT register (see Register 8-8				
11.0 "Hi-Speed USB with On-The- Go (OTG)"	The VBUSIE and VBUSIF bits were changed to: VBUSERRIE and VBUSERRIF, respectively in the USBCSR2 register (see Register 11-3).				
15.0 "Deadman Timer (DMT)"	The POR values were updated for the PSCNT<4:0> bits in the Post Status Configure DMT Count Status register (see Register 15-6).				
	The POR values were updated for the PSINTV<2:0> bits in the Post Status Configure DMT Interval Status register (see Register 15-7).				
16.0 "Watchdog Timer (WDT)"	The WDTCON register was updated (see Register 16-1).				
23.0 "Parallel Master Port (PMP)"	The PMDOUT, PMDIN, and PMRDIN registers were added (see Register 23-4, Register 23-4, and Register 23-10).				
	The PMADDR, PMWADDR, and PMRADDR registers were updated (see Register 23-3, Register 23-8, and Register 23-9).				
	The PMRDATA register was removed.				
24.0 "External Bus Interface (EBI)"	Reset values for the EBIMSK2, EBIMSK3, EBISMT0-EBISMT2, and EBIFTRPD registers were updated in the EBI Register Map (see Table 24-2).				
	POR value changes were implemented to the EBI Static Memory Timing Register (see Register 24-3).				

#### MA IOD SECTION LIDDATES