Microchip Technology - PIC32MZ0512EFF144-E/PH Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512eff144-e-ph

TABLE 4-4: INITIATORS TO TARGETS ACCESS ASSOCIATION

Target #	Initiator ID	1	2	3	4	5	6	7	8	9	10	11	12	13	14
	Name	CPU		DMA Read		DMA Write		USB	Ethernet Read	Ethernet Write	CAN1	CAN2	SQI1	Flash Controller	Crypto
1	**Flash Memory:** Program Flash Boot Flash Prefetch Module	X		X				X	X		X	X			X
2	RAM Bank 1 Memory	X		X		X		X	X	X	X	X	X	X	X
3	RAM Bank 2 Memory	X		X		X		X	X	X	X	X	X	X	X
4	External Memory via EBI and EBI Module	X		X		X		X	X	X	X	X	X		X
5	**Peripheral Set 1:** System Control, Flash Control, DMT, RTCC, CVR, PPS Input, PPS Output, Interrupts, DMA, WDT	X													
6	**Peripheral Set 2:** SPI1-SPI6 I2C1-I2C5 UART1-UART6 PMP	X		X		X									
7	**Peripheral Set 3:** Timer1-Timer9 IC1-IC9 OC1-OC9 ADC Comparator 1 Comparator 2	X		X		X									
8	**Peripheral Set 4:** PORTA-PORTK	X		X		X									
9	**Peripheral Set 5:** CAN1 CAN2 Ethernet Controller	X													
10	**Peripheral Set 6**: USB	X													
11	External Memory via SQI1 and SQI1 Module	X													
12	**Peripheral Set 7:** Crypto Engine	X													
13	**Peripheral Set 8:** RNG Module	X													

TABLE 4-17: SYSTEM BUS TARGET 9 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A420	SBT9ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
A424	SBT9ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
A428	SBT9ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
A430	SBT9ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A438	SBT9ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A440	SBT9REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
A450	SBT9RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A458	SBT9WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A460	SBT9REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
A470	SBT9RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A478	SBT9WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
01F0	IPC11	31:16	—	—	—	ADCDC2IP<2:0>			ADCDC2IS<1:0>		—	—	—	ADCDC1IP<2:0>			ADCDC1IS<1:0>		0000
		15:0	—	—	—	ADCFIFOIP<2:0>			ADCFIFOIS<1:0>		—	—	—	ADCIP<2:0>			ADCIS<1:0>		0000
0200	IPC12	31:16	—	—	—	ADCDC6IP<2:0>			ADCDC6IS<1:0>		—	—	—	ADCDC5IP<2:0>			ADCDC5IS<1:0>		0000
		15:0	—	—	—	ADCDC4IP<2:0>			ADCDC4IS<1:0>		—	—	—	ADCDC3IP<2:0>			ADCDC3IS<1:0>		0000
0210	IPC13	31:16	—	—	—	ADCDF4IP<2:0>			ADCDF4IS<1:0>		—	—	—	ADCDF3IP<2:0>			ADCDF3IS<1:0>		0000
		15:0	—	—	—	ADCDF2IP<2:0>			ADCDF2IS<1:0>		—	—	—	ADCDF1IP<2:0>			ADCDF1IS<1:0>		0000
0220	IPC14	31:16	—	—	—	ADCD0IP<2:0>			ADCD0IS<1:0>		—	—	—	ADCDFLTIP<2:0>			ADCDFLTIS<1:0>		0000
		15:0	—	—	—	ADCDF6IP<2:0>			ADCDF6IS<1:0>		—	—	—	ADCDF5IP<2:0>			ADCDF5IS<1:0>		0000
0230	IPC15	31:16	—	—	—	ADCD4IP<2:0>			ADCD4IS<1:0>		—	—	—	ADCD3IP<2:0>			ADCD3IS<1:0>		0000
		15:0	—	—	—	ADCD2IP<2:0>			ADCD2IS<1:0>		—	—	—	ADCD1IP<2:0>			ADCD1IS<1:0>		0000
0240	IPC16	31:16	—	—	—	ADCD8IP<2:0>			ADCD8IS<1:0>		—	—	—	ADCD7IP<2:0>			ADCD7IS<1:0>		0000
		15:0	—	—	—	ADCD6IP<2:0>			ADCD6IS<1:0>		—	—	—	ADCD5IP<2:0>			ADCD5IS<1:0>		0000
0250	IPC17	31:16	—	—	—	ADCD12IP<2:0>			ADCD12IS<1:0>		—	—	—	ADCD11IP<2:0>			ADCD11IS<1:0>		0000
		15:0	—	—	—	ADCD10IP<2:0>			ADCD10IS<1:0>		—	—	—	ADCD9IP<2:0>			ADCD9IS<1:0>		0000
0260	IPC18	31:16	—	—	—	ADCD16IP<2:0>			ADCD16IS<1:0>		—	—	—	ADCD15IP<2:0>			ADCD15IS<1:0>		0000
		15:0	—	—	—	ADCD14IP<2:0>			ADCD14IS<1:0>		—	—	—	ADCD13IP<2:0>			ADCD13IS<1:0>		0000
0270	IPC19	31:16	—	—	—	ADCD20IP<2:0>(2)			ADCD20IS<1:0>(2)		—	—	—	ADCD19IP<2:0>(2)			ADCD19IS<1:0>(2)		0000
		15:0	—	—	—	ADCD18IP<2:0>			ADCD18IS<1:0>		—	—	—	ADCD17IP<2:0>			ADCD17IS<1:0>		0000
0280	IPC20	31:16	—	—	—	ADCD24IP<2:0>(2)			ADCD24IS<1:0>(2)		—	—	—	ADCD23IP<2:0>(2)			ADCD23IS<1:0>(2)		0000
		15:0	—	—	—	ADCD22IP<2:0>(2)			ADCD22IS<1:0>(2)		—	—	—	ADCD21IP<2:0>(2)			ADCD21IS<1:0>(2)		0000
0290	IPC21	31:16	—	—	—	ADCD28IP<2:0>(2)			ADCD28IS<1:0>(2)		—	—	—	ADCD27IP<2:0>(2)			ADCD27IS<1:0>(2)		0000
		15:0	—	—	—	ADCD26IP<2:0>(2)			ADCD26IS<1:0>(2)		—	—	—	ADCD25IP<2:0>(2)			ADCD25IS<1:0>(2)		0000
02A0	IPC22	31:16	—	—	—	ADCD32IP<2:0>(2)			ADCD32IS<1:0>(2)		—	—	—	ADCD31IP<2:0>(2)			ADCD31IS<1:0>(2)		0000
		15:0	—	—	—	ADCD30IP<2:0>(2)			ADCD30IS<1:0>(2)		—	—	—	ADCD29IP<2:0>(2)			ADCD29IS<1:0>(2)		0000
02B0	IPC23	31:16	—	—	—	ADCD36IP<2:0>(2,4)			ADCD36IS<1:0>(2,4)		—	—	—	ADCD35IP<2:0>(2,4)			ADCD35IS<1:0>(2,4)		0000
		15:0	—	—	—	ADCD34IP<2:0>(2)			ADCD34IS<1:0>(2)		—	—	—	ADCD33IP<2:0>(2)			ADCD33IS<1:0>(2)		0000
02C0	IPC24	31:16	—	—	—	ADCD40IP<2:0>(2,4)			ADCD40IS<1:0>(2,4)		—	—	—	ADCD39IP<2:0>(2,4)			ADCD39IS<1:0>(2,4)		0000
		15:0	—	—	—	ADCD38IP<2:0>(2,4)			ADCD38IS<1:0>(2,4)		—	—	—	ADCD37IP<2:0>(2,4)			ADCD37IS<1:0>(2,4)		0000
02D0	IPC25	31:16	—	—	—	ADCD44IP<2:0>			ADCD44IS<1:0>		—	—	—	ADCD43IP<2:0>			ADCD43IS<1:0>		0000
		15:0	—	—	—	ADCD42IP<2:0>(2,4)			ADCD42IS<1:0>(2,4)		—	—	—	ADCD41IP<2:0>(2,4)			ADCD41IS<1:0>(2,4)		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

REGISTER 10-18: DCHxDAT: DMA CHANNEL x PATTERN DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPDAT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPDAT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHPDAT<15:0>:** Channel Data Register bits

Pattern Terminate mode:
Data to be matched must be stored in this register to allow terminate on match.

All other modes:
Unused.

TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
309C	USB E3RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
30A0	US BE4TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
30A4	USB E4RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
30A8	USB E5TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
30AC	USB E5RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
30B0	USB E6TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
30B4	USB E6RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
30B8	USB E7TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
30BC	USB E7RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
3100	USB E0CSR0	31:16	Indexed by the same bits in USBIE0CSR0																0000
		15:0																	0000
3108	USB E0CSR2	31:16	Indexed by the same bits in USBIE0CSR2																0000
		15:0																	0000
310C	USB E0CSR3	31:16	Indexed by the same bits in USBIE0CSR3																0000
		15:0																	0000
3110	USB E1CSR0	31:16	Indexed by the same bits in USBIE1CSR0																0000
		15:0																	0000
3114	USB E1CSR1	31:16	Indexed by the same bits in USBIE1CSR1																0000
		15:0																	0000
3118	USB E1CSR2	31:16	Indexed by the same bits in USBIE1CSR2																0000
		15:0																	0000
311C	USB E1CSR3	31:16	Indexed by the same bits in USBIE1CSR3																0000
		15:0																	0000
3120	USB E2CSR0	31:16	Indexed by the same bits in USBIE2CSR0																0000
		15:0																	0000
3124	USB E2CSR1	31:16	Indexed by the same bits in USBIE2CSR1																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

TABLE 12-23: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
15B4	RPC13R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC13R<3:0>				0000
15B8	RPC14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC14R<3:0>				0000
15C0	RPD0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD0R<3:0>				0000
15C4	RPD1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD1R<3:0>				0000
15C8	RPD2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD2R<3:0>				0000
15CC	RPD3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD3R<3:0>				0000
15D0	RPD4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD4R<3:0>				0000
15D4	RPD5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD5R<3:0>				0000
15D8	RPD6R(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD6R<3:0>				0000
15DC	RPD7R(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD7R<3:0>				0000
15E4	RPD9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD9R<3:0>				0000
15E8	RPD10R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD10R<3:0>				0000
15EC	RPD11R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD11R<3:0>				0000
15F0	RPD12R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD12R<3:0>				0000
15F8	RPD14R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD14R<3:0>				0000
15FC	RPD15R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD15R<3:0>				0000
160C	RPE3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE3R<3:0>				0000
1614	RPE5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE5R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

2: This register is not available on 64-pin and 100-pin devices.

The timer source for each Output Compare module depends on the setting of the OCACLK bit in the CFGCON register. The available configurations are shown in Table 18-1.

TABLE 18-1: TIMER SOURCE CONFIGURATIONS

Output Compare Module	Timerx	Timery
OCACLK (CFGCON<16>) = 0		
OC1 • • • OC9	Timer2 • • • Timer2	Timer3 • • • Timer3
OCACLK (CFGCON<16>) = 1		
OC1	Timer4	Timer5
OC2	Timer4	Timer5
OC3	Timer4	Timer5
OC4	Timer2	Timer3
OC5	Timer2	Timer3
OC6	Timer2	Timer3
OC7	Timer6	Timer7
OC8	Timer6	Timer7
OC9	Timer6	Timer7

20.0 SERIAL QUAD INTERFACE (SQI)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 46. "Serial Quad Interface (SQI)"** (DS60001244) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

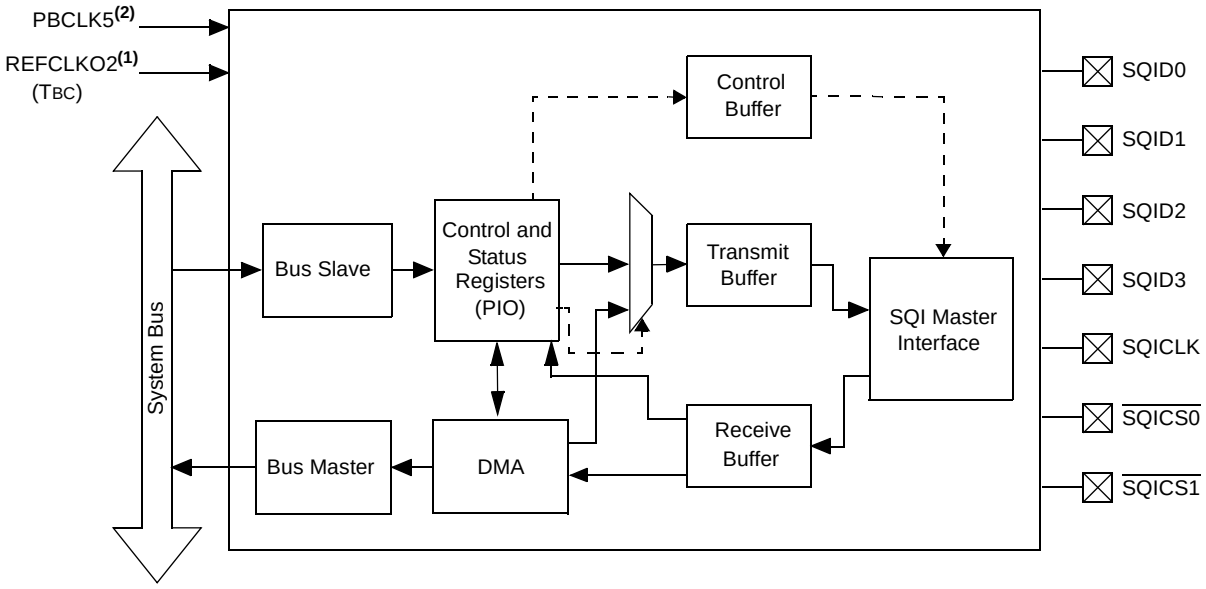
The SQI module is a synchronous serial interface that provides access to serial Flash memories and other serial devices. The SQI module supports Single Lane (identical to SPI), Dual Lane, and Quad Lane modes.

The following are key feature of the SQI module:

- Supports Single, Dual, and Quad Lane modes
- Supports Single Data Rate (SDR) mode
- Programmable command sequence
- eXecute-In-Place (XIP)
- Data transfer:
  - Programmed I/O mode (PIO)
  - Buffer descriptor DMA
- Supports SPI Mode 0 and Mode 3
- Programmable Clock Polarity (CPOL) and Clock Phase (CPHA) bits
- Supports up to two Chip Selects
- Supports up to four bytes of Flash address
- Programmable interrupt thresholds
- 32-byte transmit data buffer
- 32-byte receive data buffer
- 4-word controller buffer

Note: Once the SQI module is configured, external devices are memory mapped into KSEG2 and KSEG3 (see Figure 4-1 through Figure 4-4 in **Section 4.0 "Memory Organization"** for more information). The MMU must be enabled and the TLB must be set up to access this memory (refer to **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) of the *"PIC32 Family Reference Manual"* for more information).

FIGURE 20-1: SQI MODULE BLOCK DIAGRAM



Note 1: When configuring the REFCLKO2 clock source, a value of '0' for the ROTRIM<8:0> bits must be selected.
2: This clock source is only used for SQI Special Function Register (SFR) access.

20.1 SQI Control Registers

TABLE 20-1: SERIAL QUADRATURE INTERFACE (SQI) REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	SQI1 XCON1	31:16	—	—	—	—	—	—	—	—	DUMMYBYTES<2:0>			ADDRBYTES<2:0>			READOPCODE<7:6>		0000
		15:0	READOPCODE<5:0>						TYPEDATA<1:0>		TYPEDUMMY<1:0>		TYPEMODE<1:0>		TYPEADDR<1:0>		TYPECMD<1:0>		0000
2004	SQI1 XCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DEVSEL<1:0>		MODEBYTES<1:0>		MODECODE<7:0>								0000
2008	SQI1CFG	31:16	—	—	—	—	—	—	CSEN<1:0>		SQIEN	—	DATAEN<1:0>		CON FIFORST	RXFIFO RST	TXFIFO RST	RESET	0000
		15:0	—	—	—	BURSTEN	—	HOLD	WP	—	—	—	LSBF	CPOL	CPHA	MODE<2:0>			0000
200C	SQI1CON	31:16	—	—	—	—	—	—	—	SCHECK	—	DASSERT	DEVSEL<1:0>		LANEMODE<1:0>		CMDINIT<1:0>		0000
		15:0	TXRXCOUNT<15:0>																0000
2010	SQI1 CLKCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKDIV<10:8>			0000
		15:0	CLKDIV<7:0>								—	—	—	—	—	—	STABLE	EN	0000
2014	SQI1 CMDTHR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	TXCMDTHR<4:0>					—	—	—	RXCMDTHR<4:0>					0000
2018	SQI1 INTTHR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	TXINTTHR<4:0>					—	—	—	RXINTTHR<4:0>					0000
201C	SQI1 INTEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DMAEIE	PKT COMPIE	BD DONEIE	CON THRIE	CON EMPTYIE	CON FULLIE	RX THRIE	RX FULLIE	RX EMPTYIE	TX THRIE	TX FULLIE	TX EMPTYIE	0000
2020	SQI1 INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DMAEIF	PKT COMPIF	BD DONEIF	CON THRIF	CON EMPTYIF	CON FULLIF	RX THRIF	RX FULLIF	RX EMPTYIF	TX THRIF	TX FULLIF	TX EMPTYIF	0000
2024	SQI1 TXDATA	31:16	TXDATA<31:16>																0000
		15:0	TXDATA<15:0>																0000
2028	SQI1 RXDATA	31:16	RXDATA<31:16>																0000
		15:0	RXDATA<15:0>																0000
202C	SQI1 STAT1	31:16	—	—	—	—	—	—	—	—	TXFIFOFREE<7:0>								0000
		15:0	—	—	—	—	—	—	—	—	RXFIFOCNT<7:0>								0000
2030	SQI1 STAT2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMDSTAT<1:0>		0000
		15:0	—	—	—	—	CONAVAIL<4:0>					SDID3	SDID2	SDID1	SDID0	—	RXUN	TXOV	00x0
2034	SQI1 BDCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	START	POLLEN	DMAEN	0000
2038	SQI1BD CURADD	31:16	BDCURRADDR<31:16>																0000
		15:0	BDCURRADDR<15:0>																0000
2040	SQI1BD BASEADD	31:16	BDADDR<31:16>																0000
		15:0	BDADDR<15:0>																0000

TABLE 26-4: CRYPTO ENGINE SECURITY ASSOCIATION STRUCTURE (CONTINUED)

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY3	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY4	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY5	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY6	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY7	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY8	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_AUTHIV1	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV2	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV3	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV4	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV5	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV6	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV7	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV8	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							

REGISTER 28-3: ADCCON3: ADC CONTROL REGISTER 3 (CONTINUED)

bit 6 **GSWTRG:** Global Software Trigger bit

1 = Trigger conversion for ADC inputs that have selected the GSWTRG bit as the trigger signal, either through the associated TRGSRC<4:0> bits in the ADCTRGx registers or through the STRGSRC<4:0> bits in the ADCCON1 register

0 = Do not trigger an analog-to-digital conversion

Note: This bit is automatically cleared in the next ADC clock cycle.

bit 5-0 **ADINSEL<5:0>:** Analog Input Select bits

These bits select the analog input to be converted when the RQCNVRT bit is set. As a general rule:

111111 = Reserved
•
•
•
101101 = Reserved
101100 = MAX_AN_INPUT + 2 = IV_{TEMP}
101011 = MAX_AN_INPUT + 1 = IV_{REF}
101010 = MAX_AN_INPUT = AN[MAX_AN_INPUT]
•
•
•
000001 = AN1
000000 = AN0

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit will cause settings of SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

2: The SAMP bit only connects Class 2 and Class 3 analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

3: The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion.

4: Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx<4:0> bits and STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

REGISTER 28-4: ADCTRGMODE: ADC TRIGGERING MODE FOR DEDICATED ADC REGISTER

bit 9 **STRGEN1:** ADC1 Presynchronized Triggers bit
1 = ADC1 uses presynchronized triggers
0 = ADC1 does not use presynchronized triggers

bit 8 **STRGEN0:** ADC0 Presynchronized Triggers bit
1 = ADC0 uses presynchronized triggers
0 = ADC0 does not use presynchronized triggers

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **SSAMPEN4:** ADC4 Synchronous Sampling bit
1 = ADC4 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC4 does not use synchronous sampling

bit 3 **SSAMPEN3:** ADC3 Synchronous Sampling bit
1 = ADC3 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC3 does not use synchronous sampling

bit 2 **SSAMPEN2:** ADC2Synchronous Sampling bit
1 = ADC2 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC2 does not use synchronous sampling

bit 1 **SSAMPEN1:** ADC1 Synchronous Sampling bit
1 = ADC1 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC1 does not use synchronous sampling

bit 0 **SSAMPEN0:** ADC0 Synchronous Sampling bit
1 = ADC0 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC0 does not use synchronous sampling

REGISTER 28-7: ADCIMCON3: ADC INPUT MODE CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DIFF44	SIGN44
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF43	SIGN43	DIFF42(2)	SIGN42(2)	DIFF41(2)	SIGN41(2)	DIFF40(2)	SIGN40(2)
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF39(2)	SIGN39(2)	DIFF38(2)	SIGN38(2)	DIFF37(2)	SIGN37(2)	DIFF36(2)	SIGN36(2)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF35(2)	SIGN35(2)	DIFF34(1)	SIGN34(1)	DIFF33(1)	SIGN33(1)	DIFF32(1)	SIGN32(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **DIFF44:** AN44 Mode bit
1 = AN44 is using Differential mode
0 = AN44 is using Single-ended mode

bit 24 **SIGN44:** AN44 Signed Data Mode bit
1 = AN44 is using Signed Data mode
0 = AN44 is using Unsigned Data mode

bit 23 **DIFF43:** AN43 Mode bit
1 = AN43 is using Differential mode
0 = AN43 is using Single-ended mode

bit 22 **SIGN43:** AN43 Signed Data Mode bit
1 = AN43 is using Signed Data mode
0 = AN43 is using Unsigned Data mode

bit 21 **DIFF42:** AN42 Mode bit(2)
1 = AN42 is using Differential mode
0 = AN42 is using Single-ended mode

bit 20 **SIGN42:** AN42 Signed Data Mode bit(2)
1 = AN42 is using Signed Data mode
0 = AN42 is using Unsigned Data mode

bit 19 **DIFF41:** AN41 Mode bit(2)
1 = AN41 is using Differential mode
0 = AN41 is using Single-ended mode

bit 18 **SIGN41:** AN41 Signed Data Mode bit(2)
1 = AN41 is using Signed Data mode
0 = AN41 is using Unsigned Data mode

bit 17 **DIFF40:** AN40 Mode bit(2)
1 = AN40 is using Differential mode
0 = AN40 is using Single-ended mode

Note 1: This bit is not available on 64-pin devices.
2: This bit is not available on 64-pin and 100-pin devices.

REGISTER 28-28: ADCEIEN1: ADC EARLY INTERRUPT ENABLE REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN31(1)	EIEN30(1)	EIEN29(1)	EIEN28(1)	EIEN27(1)	EIEN26(1)	EIEN25(1)	EIEN24(1)
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN23(1)	EIEN22(1)	EIEN21(1)	EIEN20(1)	EIEN19(1)	EIEN18	EIEN17	EIEN16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN15	EIEN14	EIEN13	EIEN12	EIEN11	EIEN10	EIEN9	EIEN8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN7	EIEN6	EIEN5	EIEN4	EIEN3	EIEN2	EIEN1	EIEN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **EIEN31:EIEN0:** Early Interrupt Enable for Analog Input bits

1 = Early Interrupts are enabled for the selected analog input. The interrupt is generated after the early interrupt event occurs (indicated by the EIRDYx bit ('x' = 31-0) of the ADCEISTAT1 register)

0 = Interrupts are disabled

Note 1: This bit is not available on 64-pin devices.

REGISTER 28-29: ADCEIEN2: ADC EARLY INTERRUPT ENABLE REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	EIEN44(2)	EIEN43(2)	EIEN42(2)	EIEN41(2)	EIEN40(2)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN39(2)	EIEN38(2)	EIEN37(2)	EIEN36(2)	EIEN35(2)	EIEN34(1)	EIEN33(1)	EIEN32(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-0 **EIEN44:EIEN32:** Early Interrupt Enable for Analog Input bits

1 = Early Interrupts are enabled for the selected analog input. The interrupt is generated after the early interrupt event occurs (indicated by the EIRDYx bit ('x' = 44-32) of the ADCEISTAT2 register)

0 = Interrupts are disabled

Note 1: This bit is not available on 64-pin devices.

2: This bit is not available on 64-pin and 100-pin devices.

REGISTER 29-15: CiFLTCON5: CAN FILTER CONTROL REGISTER 5 (CONTINUED)

bit 15 **FLTEN21:** Filter 21 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL21<1:0>:** Filter 21 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL21<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN20:** Filter 20 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL20<1:0>:** Filter 20 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL20<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

NOTES:

TABLE 37-12: DC CHARACTERISTICS: PROGRAM MEMORY(3)

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Sym.**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
D130a	EP	Cell Endurance	10,000	—	—	E/W	Without ECC
D130b			20,000	—	—	E/W	With ECC
D131	VPR	VDD for Read	VDDMIN	—	VDDMAX	V	—
D132	VPEW	VDD for Erase or Write	VDDMIN	—	VDDMAX	V	—
D134a	TRETD	Characteristic Retention	10	—	—	Year	Without ECC
D134b			20	—	—	Year	With ECC
D135	IDDP	Supply Current during Programming	—	—	30	mA	—
D136	TRW	Row Write Cycle Time **(Notes 2, 4)**	—	66813	—	FRC Cycles	—
D137	TQWW	Quad Word Write Cycle Time **(Note 4)**	—	773	—	FRC Cycles	—
D138	TWW	Word Write Cycle Time **(Note 4)**	—	383	—	FRC Cycles	—
D139	TCE	Chip Erase Cycle Time **(Note 4)**	—	515373	—	FRC Cycles	—
D140	TPFE	All Program Flash (Upper and Lower regions) Erase Cycle Time **(Note 4)**	—	256909	—	FRC Cycles	—
D141	TPBE	Program Flash (Upper or Lower regions) Erase Cycle Time **(Note 4)**	—	128453	—	FRC Cycles	—
D142	TPGE	Page Erase Cycle Time **(Note 4)**	—	128453	—	FRC Cycles	—

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: The minimum PBCLK5 for row programming is 4 MHz.

3: Refer to the *"PIC32 Flash Programming Specification"* (DS60001145) for operating conditions during programming and erase cycles.

4: This parameter depends on FRC accuracy (see Table 37-20) and FRC tuning values (see the OSCTUN register: Register 8-2).

TABLE 37-13: DC CHARACTERISTICS: PROGRAM FLASH MEMORY WAIT STATES

DC CHARACTERISTICS	Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Required Flash Wait States(1)	**SYSCLK**	**Units**	**Conditions**
With ECC:			
0 Wait states	0 < SYSCLK ≤ 60	MHz	—
1 Wait state	60 < SYSCLK ≤ 120		
2 Wait states	120 < SYSCLK ≤ 200		
Without ECC:			
0 Wait states	0 < SYSCLK ≤ 74	MHz	—
1 Wait state	74 < SYSCLK ≤ 140		
2 Wait states	140 < SYSCLK ≤ 200		

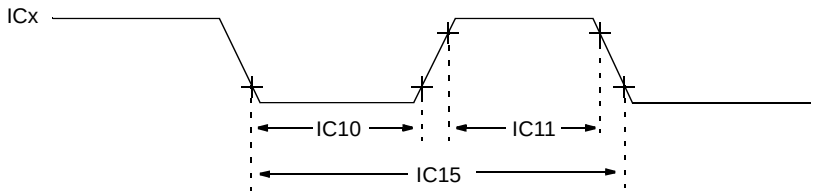
Note 1: To use Wait states, the Prefetch module must be enabled (PREFEN<1:0> ≠ 00) and the PFMWS<2:0> bits must be written with the desired Wait state value.

TABLE 37-26: TIMER2-TIMER9 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**		**Min.**	**Max.**	**Units**	**Conditions**	
TB10	TTXH	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 25 ns	—	ns	Must also meet parameter TB15	N = prescale value (1, 2, 4, 8, 16, 32, 64, 256)
TB11	TTXL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 25 ns	—	ns	Must also meet parameter TB15	
TB15	TTXP	TxCK Input Period	Synchronous, with prescaler	[(Greater of [(25 ns or 2 TPBCLK3)/N] + 30 ns	—	ns	VDD > 2.7V	
				[(Greater of [(25 ns or 2 TPBCLK3)/N] + 50 ns	—	ns	VDD < 2.7V	
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	1	TPBCLK3	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 37-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS



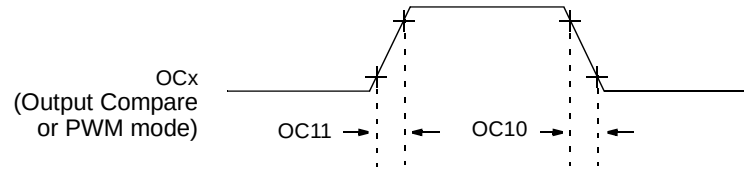
Note: Refer to Figure 37-1 for load conditions.

TABLE 37-27: INPUT CAPTURE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Max.**	**Units**	**Conditions**	
IC10	TCCL	ICx Input Low Time	[(12.5 ns or 1 TPBCLK3) /N] + 25 ns	—	ns	Must also meet parameter IC15.	N = prescale value (1, 4, 16)
IC11	TCCH	ICx Input High Time	[(12.5 ns or 1 TPBCLK3) /N] + 25 ns	—	ns	Must also meet parameter IC15.	
IC15	TCCP	ICx Input Period	[(25 ns or 2 TPBCLK3) /N] + 50 ns	—	ns	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 37-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS



Note: Refer to Figure 37-1 for load conditions.

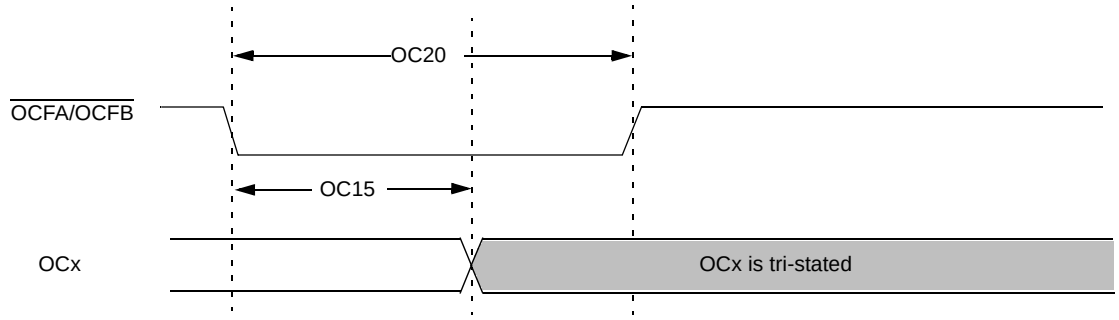
TABLE 37-28: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See parameter DO31

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 37-9: OCx/PWM MODULE TIMING CHARACTERISTICS



Note: Refer to Figure 37-1 for load conditions.

TABLE 37-29: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Typical(2)**	**Max**	**Units**	**Conditions**
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	—
OC20	TFLT	Fault Input Pulse Width	50	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

A.2 Analog-to-Digital Converter (ADC)

The PIC32MZ EF family of devices has a new 12-bit High-Speed Successive Approximation Register (SAR) ADC module that replaces the 10-bit ADC module in PIC32MX5XX/6XX/7XX devices; therefore, the use of **Bold** type to show differences is *not* used in the following table. Note that not all register differences are described in this section; however, the key feature differences are listed in Table A-3.

TABLE A-3: ADC DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Clock Selection and Operating Frequency (TAD)	
On PIC32MX devices, the ADC clock was derived from either the FRC or from the PBCLK. ADRC (AD1CON3<15>) 1 = FRC clock 0 = Clock derived from Peripheral Bus Clock (PBCLK)	On PIC32MZ EF devices, the three possible sources of the ADC clock are FRC, REFCLKO3, and SYSCLK. ADCSEL<1:0> (ADCCON3<31:30>) 11 = FRC 10 = REFCLKO3 01 = SYSCLK 00 = Reserved
On PIC32MX devices, if the ADC clock was derived from the PBCLK, that frequency was divided further down, with a maximum divisor of 512, and a minimum divisor of two. ADCS<7:0> (AD1CON3<7:0>) 11111111 = 512 * TPB = TAD • • • 00000001 = 4 * TPB = TAD 00000000 = 2 * TPB = TAD	On PIC32MZ EF devices, any ADC clock source can be divided down separately for each dedicated ADC and the shared ADC, with a maximum divisor of 254. The input clock can also be fed directly to the ADC. ADCDIV<6:0> (ADCTIMEx<22:16>) ADCDIV<6:0> (ADCCON2<6:0>) 1111111 = 254 * TQ = TAD • • • 0000011 = 6 * TQ = TAD 0000010 = 4 * TQ = TAD 0000001 = 2 * TQ = TAD 0000000 = TQ = TAD