Microchip Technology - PIC32MZ0512EFF144-I/JWX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TFBGA
Supplier Device Package	144-TFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512eff144-i-jwx

The System Bus arbitration scheme implements a non-programmable, Least Recently Serviced (LRS) priority, which provides Quality Of Service (QOS) for most initiators. However, some initiators can use Fixed High Priority (HIGH) arbitration to guarantee their access to data.

The arbitration scheme for the available initiators is shown in Table 4-5.

TABLE 4-5: INITIATOR ID AND QOS

Name	ID	QOS
CPU	1	LRS(1)
CPU	2	HIGH(1,2)
DMA Read	3	LRS(1)
DMA Read	4	HIGH(1,2)
DMA Write	5	LRS(1)
DMA Write	6	HIGH(1,2)
USB	7	LRS
Ethernet Read	8	LRS
Ethernet Write	9	LRS
CAN1	10	LRS
CAN2	11	LRS
SQI1	12	LRS
Flash Controller	13	HIGH(2)
Crypto	14	LRS

Note 1: When accessing SRAM, the DMAPRI bit (CFGCON<25>) and the CPUPRI bit (CFGCON<24>) provide arbitration control for the DMA and CPU (when servicing an interrupt (i.e., EXL = 1)), respectively, by selecting the use of LRS or HIGH When using HIGH, the DMA and CPU get arbitration preference over all initiators using LRS.

2: Using HIGH arbitration can have serious negative effects on other initiators. Therefore, it is recommended to not enable this type of arbitration for an initiator that uses significant system bandwidth. HIGH arbitration is intended to be used for low bandwidth applications that require low latency, such as LCC graphics applications.

4.3 Permission Access and System Bus Registers

The System Bus on PIC32MZ EF family of microcontrollers provides access control capabilities for the transaction initiators on the System Bus.

The System Bus divides the entire memory space into fourteen target regions and permits access to each target by initiators via permission groups. Four Permission Groups (0 through 3) can be assigned to each initiator. Each permission group is independent of the others and can have exclusive or shared access to a region.

Using the CFGPG register (see Register 34-10 in **Section 34.0 “Special Features”**), Boot firmware can assign a permission group to each initiator, which can make requests on the System Bus.

The available targets and their regions, as well as the associated control registers to assign protection, are described and listed in Table 4-6.

Register 4-2 through Register 4-10 are used for setting and controlling access permission groups and regions.

To change these registers, they must be unlocked in hardware. The register lock is controlled by the PGLOCK Configuration bit (CFGCON<11>). Setting PGLOCK prevents writes to the control registers; clearing PGLOCK allows writes.

To set or clear the PGLOCK bit, an unlock sequence must be executed. Refer to **Section 42. “Oscillators with Enhanced PLL”** in the *“PIC32 Family Reference Manual”* for details.

TABLE 4-15: SYSTEM BUS TARGET 7 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9C20	SBT7ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
9C24	SBT7ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
9C28	SBT7ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9C30	SBT7ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9C38	SBT7ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9C40	SBT7REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9C50	SBT7RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9C58	SBT7WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9C60	SBT7REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9C70	SBT7RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9C78	SBT7WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

REGISTER 4-3: SBTxELOG1: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 1 ('x' = 0-13) (CONTINUED)

bit 7-4 **REGION<3:0>:** Requested Region Number bits
1111 - 0000 = Target's region that reported a permission group violation

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **CMD<2:0>:** Transaction Command of the Requester bits
111 = Reserved
110 = Reserved
101 = Write (a non-posted write)
100 = Reserved
011 = Read (a locked read caused by a Read-Modify-Write transaction)
010 = Read
001 = Write
000 = Idle

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

REGISTER 10-2: DMASTAT: DMA STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	RDWR	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	DMACH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **RDWR:** Read/Write Status bit
1 = Last DMA bus access when an error was detected was a read
0 = Last DMA bus access when an error was detected was a write

bit 30-3 **Unimplemented:** Read as '0'

bit 2-0 **DMACH<2:0>:** DMA Channel bits
These bits contain the value of the most recent active DMA channel when an error was detected.

REGISTER 10-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DMAADDR<31:0>:** DMA Module Address bits
These bits contain the address of the most recent DMA access when an error was detected.

REGISTER 10-9: DCHxINT: DMA CHANNEL x INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **CHSDIE:** Channel Source Done Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 22 **CHSHIE:** Channel Source Half Empty Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 21 **CHDDIE:** Channel Destination Done Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 20 **CHDHIE:** Channel Destination Half Full Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 19 **CHBCIE:** Channel Block Transfer Complete Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 18 **CHCCIE:** Channel Cell Transfer Complete Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 17 **CHTAIE:** Channel Transfer Abort Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 16 **CHERIE:** Channel Address Error Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CHSDIF:** Channel Source Done Interrupt Flag bit
- 1 = Channel Source Pointer has reached end of source (CHSPTR = CHSSIZ)
- 0 = No interrupt is pending

bit 6 **CHSHIF:** Channel Source Half Empty Interrupt Flag bit
- 1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2)
- 0 = No interrupt is pending

11.0 HI-SPEED USB WITH ON-THE-GO (OTG)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 51. "Hi-Speed USB with On-The-Go (OTG)"** (DS60001326) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 embedded host, device, or OTG implementation with a minimum of external components.

The module supports Hi-Speed, Full-Speed, or Low-Speed in any of the operating modes. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the RAM controller, packet encode/decode, UTM synchronization, end-point control, a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 11-1.

The USB module includes the following features:

- USB Hi-Speed, Full-Speed, and Low-Speed support for host and device
- USB OTG support with one or more Hi-Speed, Full-Speed, or Low-Speed device
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Integrated 8-channel DMA to access system RAM and Flash
- Seven transmit endpoints and seven receive endpoints, in addition to Endpoint 0
- Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) support
- Suspend and resume signaling support
- Dynamic FIFO sizing
- Integrated RAM for the FIFOs, eliminating the need for system RAM for the FIFOs
- Link power management support

Note 1: The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

2: If the USB module is used, the Primary Oscillator (POSC) is limited to either 12 MHz or 24 MHz.

11.1 USB OTG Control Registers

TABLE 11-1: USB REGISTER MAP 1

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	USBCSR0	31:16	—	—	—	—	—	—	—	—	EP7TXIF	EP6TXIF	EP5TXIF	EP4TXIF	EP3TXIF	EP2TXIF	EP1TXIF	EP0IF	0000
		15:0	ISOUPD(1)	SOFT CONN(1)	HSEN	HSMODE	RESET	RESUME	SUSP MODE	SUSPEN	—	FUNC<6:0>(1)							2000
			—(2)	—(2)								—(2)	—(2)	—(2)	—(2)	—(2)	—(2)	—(2)	
3004	USBCSR1	31:16	—	—	—	—	—	—	—	—	EP7TXIE	EP6TXIE	EP5TXIE	EP4TXIE	EP3TXIE	EP2TXIE	EP1TXIE	EP0IE	00FF
		15:0	—	—	—	—	—	—	—	—	EP7RXIF	EP6RXIF	EP5RXIF	EP4RXIF	EP3RXIF	EP2RXIF	EP1RXIF	—	0000
3008	USBCSR2	31:16	VBUSERRIE	SESSRQIE	DISCONIE	CONNIE	SOFIE	RESETIE	RESUMEIE	SUSPIE	VBUSERRIF	SESSREQIF	DISCONIF	CONNIF	SOFIF	RESETIF	RESUMEIF	SUSPIF	0600
		15:0	—	—	—	—	—	—	—	—	EP7RXIE	EP6RXIE	EP5RXIE	EP4RXIE	EP3RXIE	EP2RXIE	EP1RXIE	—	00FE
300C	USBCSR3	31:16	FORCEHST	FIFOACC	FORCEFS	FORCEHS	PACKET	TESTK	TESTJ	NAK	—	—	—	—	ENDPOINT<3:0>				0000
		15:0	—	—	—	—	—	RFRMNUM<10:0>											0000
3010	USB IE0CSR0(3)	31:16	—	—	—	—	—(1)	—(1)	—(1)	FLSHFIFO	SVC SETEND(1)	SVCRPR(1)	SEND STALL(1)	SETUP END(1)	DATAEND(1)	SENT STALL(1)	TXPKT RDY	RXPKT RDY	0000
							DISPING(2)	DTWREN(2)	DATA TGGL(2)		NAK TMOUT(2)	STATPKT(2)	REQPKT(2)	ERROR(2)	SETUP PKT(2)	RXSTALL(2)			0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
3018	USB IE0CSR2(3)	31:16	—	—	—	NAKLIM<4:0>(2)					SPEED<1:0>(2)		—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	RXCNT<6:0>							0000
301C	USB IE0CSR3(3)	31:16	MPRXEN	MPTXEN	BIGEND	HBRXEN	HBTXEN	DYNFIFOS	SOFTCONE	UTMIDWID	—	—	—	—	—	—	—	—	xx00
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
3010	USB IENCSR0(4)	31:16	AUTOSET	ISO(1)	MODE	DMA REQEN	FRC DATTG	DMA REQMD	—(1)	—(1)	INCOMP TX(1)	CLRDT	SENT STALL(1)	SEND STALL(1)	FLUSH	UNDER RUN(1)	FIFONE	TXPKT RDY	0000
				—					DTWREN(2)	DATA TGGL(2)	NAK TMOUT(2)		RXSTALL(2)	SETUPPKT(2)		ERROR(2)			0000
		15:0	MULT<4:0>					TXMAXP<10:0>											0000
3014	USB IENCSR1(4)	31:16	AUTOCLR	ISO(1)	DMA REQEN	DISNYET(1)	DMA REQMD	—(1)	—(1)	INCOM PRX	CLRDT	SENTSTALL(1)	SENDSTALL(1)	FLUSH	DATAERR(1)	OVERRUN(1)	FIFOFULL	RXPKT RDY	0000
				AUTORQ(2)		PIDERR(2)		DATA TWEN(2)	DATA TGGL(2)			RXSTALL(2)	REQPKT(2)		DERR-NAKT(1)	ERROR(2)			0000
		15:0	MULT<4:0>					RXMAXP<10:0>											0000
3018	USB IENCSR2(4)	31:16	TXINTERV<7:0>(2)								SPEED<1:0>(2)		PROTOCOL<1:0>		TEP<3:0>				0000
		15:0	—	—	RXCNT<13:0>														0000
301C	USB IENCSR3(1,3)	31:16	RXFIFOSZ<3:0>				TXFIFOSZ<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	RXINTERV<7:0>								SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>				0000
3020	USB FIFO0	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3024	USB FIFO1	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

REGISTER 11-11: USBIENCSR3: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 3 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RXFIFOSZ<3:0>				TXFIFOSZ<3:0>			
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXINTERV<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **RXFIFOSZ<3:0>:** Receive FIFO Size bits
1111 = Reserved
1110 = Reserved
1101 = 8192 bytes
1100 = 4096 bytes
•
•
•
0011 = 8 bytes
0010 = Reserved
0001 = Reserved
0000 = Reserved or endpoint has not been configured

This register only has this interpretation when dynamic sizing is not selected. It is not valid where dynamic FIFO sizing is used.

bit 27-24 **TXFIFOSZ<3:0>:** Transmit FIFO Size bits
1111 = Reserved
1110 = Reserved
1101 = 8192 bytes
1100 = 4096 bytes
•
•
•
0011 = 8 bytes
0010 = Reserved
0001 = Reserved
0000 = Reserved or endpoint has not been configured

This register only has this interpretation when dynamic sizing is not selected. It is not valid where dynamic FIFO sizing is used.

bit 23-16 **Unimplemented:** Read as '0'

REGISTER 11-28: USBLPMR1: USB LINK POWER MANAGEMENT CONTROL REGISTER 1 (CONTINUED)

bit 16 **LPMXMT:** LPM Transition to the L1 State bit

When in *Device mode*:

1 = USB module will transition to the L1 state upon the receipt of the next LPM transaction. LPMEN must be set to '0b11. Both LPMXMT and LPMEN must be set in the same cycle.

0 = Maintain current state

When LPMXMT and LPMEN are set, the USB module can respond in the following ways:

- If no data is pending (all TX FIFOs are empty), the USB module will respond with an ACK. The bit will self clear and a software interrupt will be generated.
- If data is pending (data resides in at least one TX FIFO), the USB module will respond with a NYET. In this case, the bit will not self clear however a software interrupt will be generated.

When in *Host mode*:

1 = USB module will transmit an LPM transaction. This bit is self clearing, and will be immediately cleared upon receipt of any Token or three time-outs have occurred.

0 = Maintain current state

bit 15-12 **ENDPOINT<3:0>:** LPM Token Packet Endpoint bits

This is the endpoint in the token packet of the LPM transaction.

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **RMTWAK:** Remote Wake-up Enable bit

This bit is applied on a temporary basis only and is only applied to the current suspend state.

1 = Remote wake-up is enabled

0 = Remote wake-up is disabled

bit 7-4 **HIRD<3:0>:** Host Initiated Resume Duration bits

The minimum time the host will drive resume on the bus. The value in this register corresponds to an actual resume time of:

Resume Time = 50 µs + HIRD * 75 µs. The resulting range is 50 µs to 1200 µs.

bit 3-0 **LNKSTATE<3:0>:** Link State bits

This value is provided by the host to the peripheral to indicate what state the peripheral must transition to after the receipt and acceptance of a LPM transaction. The only valid value for this register is '1' for Sleep State (L1). All other values are reserved.

REGISTER 27-3: RNGPOLYx: RANDOM NUMBER GENERATOR POLYNOMIAL REGISTER 'x' ('x' = 1 OR 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	POLY<31:24>							
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	POLY<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLY<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **POLY<31:0>:** PRNG LFSR Polynomial MSb/LSb bits (RNGPOLY1 = LSb, RNGPOLY2 = MSb)

REGISTER 27-4: RNGNUMGENx: RANDOM NUMBER GENERATOR REGISTER 'x' ('x' = 1 OR 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RNG<31:24>							
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RNG<23:16>							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RNG<15:8>							
7:0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RNG<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **RNG<31:0>:** Current PRNG MSb/LSb Value bits (RNGNUMGEN1 = LSb, RNGNUMGEN2 = MSb)

TABLE 28-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B234	ADCDATA13	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B238	ADCDATA14	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B23C	ADCDATA15	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B240	ADCDATA16	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B244	ADCDATA17	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B248	ADCDATA18	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B24C	ADCDATA19(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B250	ADCDATA20(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B254	ADCDATA21(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B258	ADCDATA22(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B25C	ADCDATA23(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B260	ADCDATA24(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B264	ADCDATA25(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B268	ADCDATA26(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B26C	ADCDATA27(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B270	ADCDATA28(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B274	ADCDATA29(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B278	ADCDATA30(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B27C	ADCDATA31(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This bit or register is not available on 64-pin and 100-pin devices.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

TABLE 28-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B280	ADCDATA32(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B284	ADCDATA33(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B288	ADCDATA34(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B28C	ADCDATA35(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B290	ADCDATA36(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B294	ADCDATA37(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B298	ADCDATA38(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B29C	ADCDATA39(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B2A0	ADCDATA40(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B2A4	ADCDATA41(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B2A8	ADCDATA42(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B2AC	ADCDATA43	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B2B0	ADCDATA44	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This bit or register is not available on 64-pin and 100-pin devices.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

REGISTER 28-19: ADCTRG3: ADC TRIGGER SOURCE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC11<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC10<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC9<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC8<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC11<4:0>:** Trigger Source for Conversion of Analog Input AN11 Select bits
11111 = Reserved
•
•
•
01101 = Reserved
01100 = Comparator 2 (COUT)
01011 = Comparator 1 (COUT)
01010 = OCMP5
01001 = OCMP3
01000 = OCMP1
00111 = TMR5 match
00110 = TMR3 match
00101 = TMR1 match
00100 = INT0 External interrupt
00011 = STRIG
00010 = Global level software trigger (GLSWTRG)
00001 = Global software edge Trigger (GSWTRG)
00000 = No Trigger

For STRIG, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSS*x* registers.

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TRGSRC10<4:0>:** Trigger Source for Conversion of Analog Input AN10 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC9<4:0>:** Trigger Source for Conversion of Analog Input AN9 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC8<4:0>:** Trigger Source for Conversion of Analog Input AN8 Select bits
See bits 28-24 for bit value definitions.

REGISTER 28-21: ADCCMPCONx: ADC DIGITAL COMPARATOR 'x' CONTROL REGISTER ('x' = 2 THROUGH 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	AINID<4:0>				
7:0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **AINID<4:0>:** Digital Comparator 'x' Analog Input Identification (ID) bits

When a digital comparator event occurs (DCMPED = 1), these bits identify the analog input being monitored by the Digital Comparator.

Note: Only analog inputs <31:0> can be processed by the Digital Comparator module 'x' ('x' = 1-5).

11111 = AN31 is being monitored
11110 = AN30 is being monitored
•
•
•
00001 = AN1 is being monitored
00000 = AN0 is being monitored

bit 7 **ENDCMP:** Digital Comparator 'x' Enable bit

1 = Digital Comparator 'x' is enabled
0 = Digital Comparator 'x' is not enabled, and the DCMPED status bit (ADCCMP*x*CON<5>) is cleared

bit 6 **DCMPGIEN:** Digital Comparator 'x' Global Interrupt Enable bit

1 = A Digital Comparator 'x' interrupt is generated when the DCMPED status bit (ADCCMP*x*CON<5>) is set
0 = A Digital Comparator 'x' interrupt is disabled

bit 5 **DCMPED:** Digital Comparator 'x' "Output True" Event Status bit

The logical conditions under which the digital comparator gets "True" are defined by the IEBTWN, IEHIHI, IEHILO, IELOHI and IELOLO bits.

Note: This bit is cleared by reading the AINID<5:0> bits (ADCCMP0CON<13:8>) or by disabling the Digital Comparator module (by setting ENDCMP to '0').

1 = Digital Comparator 'x' output true event has occurred (output of Comparator is '1')
0 = Digital Comparator 'x' output is false (output of Comparator is '0')

bit 4 **IEBTWN:** Between Low/High Digital Comparator 'x' Event bit

1 = Generate a digital comparator event when the DCMPLO<15:0> bits ≤ DATA<31:0> bits < DCMPHI<15:0> bits
0 = Do not generate a digital comparator event

bit 3 **IEHIHI:** High/High Digital Comparator 'x' Event bit

1 = Generate a Digital Comparator 'x' Event when the DCMPHI<15:0> bits ≤ DATA<31:0> bits
0 = Do not generate an event

bit 2 **IEHILO:** High/Low Digital Comparator 'x' Event bit

1 = Generate a Digital Comparator 'x' Event when the DATA<31:0> bits < DCMPHI<15:0> bits
0 = Do not generate an event

REGISTER 29-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	WAKFIL	—	—	—	SEG2PH<2:0>(1,4)		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SEG2PHTS(1)	SAM(2)	SEG1PH<2:0>			PRSEG<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SJW<1:0>(3)		BRP<5:0>					

Legend:	HC = Hardware Clear	S = Settable bit	
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-23 **Unimplemented:** Read as ‘0’

bit 22 **WAKFIL:** CAN Bus Line Filter Enable bit
1 = Use CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 21-19 **Unimplemented:** Read as ‘0’

bit 18-16 **SEG2PH<2:0>:** Phase Buffer Segment 2 bits(1,4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 15 **SEG2PHTS:** Phase Segment 2 Time Select bit(1)
1 = Freely programmable
0 = Maximum of SEG1PH or Information Processing Time, whichever is greater

bit 14 **SAM:** Sample of the CAN Bus Line bit(2)
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 13-11 **SEG1PH<2:0>:** Phase Buffer Segment 1 bits(4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
2: 3 Time bit sampling is not allowed for BRP < 2.
3: SJW ≤ SEG2PH.
4: The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

TABLE 30-5: ETHERNET CONTROLLER REGISTER SUMMARY (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2110	ETH FRMTXOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FRMTXOKCNT<15:0>																0000
2120	ETH SCOLFRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SCOLFRMCNT<15:0>																0000
2130	ETH MCOLFRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MCOLFRMCNT<15:0>																0000
2140	ETH FRMRXOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FRMRXOKCNT<15:0>																0000
2150	ETH FCSERR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FCSERRCNT<15:0>																0000
2160	ETH ALGNERR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALGNERRCNT<15:0>																0000
2200	EMAC1 CFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SOFT RESET	SIM RESET	—	—	RESET RMCS	RESET RFUN	RESET TMCS	RESET TFUN	—	—	—	LOOPBACK	TXPAUSE	RXPAUSE	PASSALL	RXENABLE	800D
2210	EMAC1 CFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	EXCESS DFR	BP NOBKOFF	NOBKOFF	—	—	LONGPRE	PUREPRE	AUTOPAD	VLANPAD	PAD ENABLE	CRC ENABLE	DELAYCRC	HUGEFRM	LENGTHCK	FULLDPLX	4082
2220	EMAC1 IPGT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	B2BIPKTGP<6:0>							0012
2230	EMAC1 IPGR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	NB2BIPKTGP1<6:0>							—	NB2BIPKTGP2<6:0>							0C12
2240	EMAC1 CLRT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CWINDOW<5:0>						—	—	—	—	RETX<3:0>				370F
2250	EMAC1 MAXF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MACMAXF<15:0>																05EE
2260	EMAC1 SUPP	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	RESET RMII	—	—	SPEED RMII	—	—	—	—	—	—	—	—	1000
2270	EMAC1 TEST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	TESTBP	TESTPAUSE	SHRTQNTA	0000
2280	EMAC1 MCFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RESET MGMT	—	—	—	—	—	—	—	—	—	CLKSEL<3:0>				NOPRE	SCANINC	0020
2290	EMAC1 MCMD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCAN	READ	0000
22A0	EMAC1 MADR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PHYADDR<4:0>					—	—	—	REGADDR<4:0>					0100

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

2: Reset values default to the factory programmed value.

34.2 Registers

TABLE 34-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FFC0	DEVCFG3	31:16	—	FUSBIDIO	IOL1WAY	PMDL1WAY	PGL1WAY	—	FETHIO	FMIIEN	—	—	—	—	—	—	—	—	xxxx
		15:0	USERID<15:0>																xxxx
FFC4	DEVCFG2	31:16	—	UPLLFSEL	—	—	—	—	—	—	—	—	—	—	—	FPLLODIV<2:0>			xxxx
		15:0	—	FPLLMULT<6:0>							FPLLICLK	FPLLRNG<2:0>			—	FPLLIDIV<2:0>			xxxx
FFC8	DEVCFG1	31:16	FDMTEN	DMTCNT<4:0>					FWDTWINSZ<1:0>		FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>					xxxx
		15:0	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMOD<1:0>		IESO	FSOSCEN	DMTINTV<2:0>			FNOSC<2:0>			xxxx
FFCC	DEVCFG0	31:16	—	EJTAGBEN	—	—	—	—	—	—	—	—	POSCBOOST	POSCGAIN<1:0>		SOSCBOOST	SOSCGAIN<1:0>		xxxx
		15:0	SMCLR	DBGPER<2:0>			—	FSLEEP	FECCCON<1:0>		—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN	DEBUG<1:0>		xxxx
FFD0	DEVCP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFD4	DEVCP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFD8	DEVCP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFDC	DEVCP0	31:16	—	—	—	CP	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE0	DEVSIGN3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE4	DEVSIGN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE8	DEVSIGN1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFEC	DEVSIGN0	31:16	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

TABLE 37-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial		
Param. No.	**Typical(2)**	**Maximum(5)**	**Units**	**Conditions**	
Power-Down Current (I_{PD}) (Note 1)					
DC40k	0.7	7	mA	-40°C	Base Power-Down Current
DC40l	1.5	7	mA	+25°C	
DC40n	7	20	mA	+85°C	
Module Differential Current					
DC41e	15	50	µA	3.6V	Watchdog Timer Current: ΔI_{WDT} **(Note 3)**
DC42e	25	50	µA	3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} **(Note 3)**
DC43d	3	3.8	mA	3.6V	ADC: ΔI_{ADC} **(Notes 3, 4)**
DC44	15	50	µA	3.6V	Deadman Timer Current: ΔI_{DMT} **(Note 3)**

Note 1: The test conditions for I_{PD} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBMD = 1), V_{USB3V3} is connected to V_{SS}
- CPU is in Sleep mode
- L1 Cache and Prefetch modules are disabled
- No peripheral modules are operating, (ON bit = 0), and the associated PMD bit is set. All clocks are disabled ON bit (PBxDIV<15>) = 0 (x ≠ 1,7)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DD}
- RTCC and JTAG are disabled
- Voltage regulator is in Stand-by mode (VREGS = 0)

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Voltage regulator is operational (VREGS = 1).

5: Data in the "Maximum" column is at 3.3V, +85ºC at specified operating frequency, unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 37-47: EBI TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
EB10	TEBICLK	Internal EBI Clock Period (PBCLK8)	10	—	—	ns	—
EB11	TEBIRC	EBI Read Cycle Time (TRC<5:0>)	20	—	—	ns	—
EB12	TEBIPRC	EBI Page Read Cycle Time (TPRC<3:0>)	20	—	—	ns	—
EB13	TEBIAS	EBI Write Address Setup (TAS<1:0>)	10	—	—	ns	—
EB14	TEBIWP	EBI Write Pulse Width (TWP<5:0>)	10	—	—	ns	—
EB15	TEBIWR	EBI Write Recovery Time (TWR<1:0>)	10	—	—	ns	—
EB16	TEBICO	EBI Output Control Signal Delay	—	—	5	ns	See **Note 1**
EB17	TEBIDO	EBI Output Data Signal Delay	—	—	5	ns	See **Note 1**
EB18	TEBIDS	EBI Input Data Setup	5	—	—	ns	See **Note 1**
EB19	TEBIDH	EBI Input Data Hold	3	—	—	ns	See **Note 1, 2**

Note 1: Maximum pin capacitance = 10 pF.

2: Hold time from EBI Address change is 0 ns.

TABLE 37-48: EBI THROUGHPUT REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
EB20	Asynchronous SRAM Read	—	100	—	Mbps	—
EB21	Asynchronous SRAM Write	—	533	—	Mbps	—

Note 1: Maximum pin capacitance = 10 pF.

2: Hold time from EBI Address change is 0 ns.

TABLE A-1: OSCILLATOR CONFIGURATION DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Fail-Safe Clock Monitor (FSCM)	
On PIC32MX devices, the internal FRC became the clock source on a failure of the clock source.	On PIC32MZ EF devices, a separate internal Backup FRC (BFRC) becomes the clock source upon a failure at the clock source.
On PIC32MX devices, a clock failure resulted in the triggering of a specific interrupt when the switchover was complete. **FSCM generates an interrupt.**	On PIC32MZ EF devices, a NMI is triggered instead, and must be handled by the NMI routine. **FSCM generates a NMI.**
FCKSM<1:0> (DEVCFG1<15:14>) **1x = Clock switching is disabled, FSCM is disabled** 01 = Clock switching is enabled, FSCM is disabled **00 = Clock switching is enabled, FSCM is enabled**	The definitions of the FCKSM<1:0> bits has changed on PIC32MZ EF devices. FCKSM<1:0> (DEVCFG1<15:14>) **11 = Clock switching is enabled and clock monitoring is enabled** **10 = Clock switching is disabled and clock monitoring is enabled** 01 = Clock switching is enabled and clock monitoring is disabled **00 = Clock switching is disabled and clock monitoring is disabled**
On PIC32MX devices, the CF (OSCCON<3>) bit indicates a clock failure. Writing to this bit initiates a FSCM event.	On PIC32MZ EF devices, the CF (OSCCON<3>) bit has the same functionality as that of PIC32MX device; however, an additional CF(RNMICON<1>) bit is available to indicate a NMI event. Writing to this bit causes a NMI event, but not a FSCM event.
On PIC32MX devices, the CLKLOCK (OSCCON<7>) bit is controlled by the FSCM. CLKLOCK (OSCCON<7>) **If clock switching and monitoring is disabled (FCKSM<1:0> = 1x):** 1 = Clock and PLL selections are locked 0 = Clock and PLL selections are not locked and may be modified **If clock switching and monitoring is enabled (FCKSM<1:0> = 0x):** **Clock and PLL selections are never locked and may be modified.**	On PIC32MZ EF devices, the CLKLOCK (OSCCON<7>) bit is not impacted by the FSCM. CLKLOCK (OSCCON<7>) 1 = Clock and PLL selections are locked 0 = Clock and PLL selections are not locked and may be modified

Table A-2 illustrates the difference in code setup of the respective parts for maximum speed using an external 24 MHz crystal.

TABLE A-2: CODE DIFFERENCES FOR MAXIMUM SPEED USING AN EXTERNAL 24 MHz CRYSTAL

PIC32MX5XX/6XX/7XX @ 80 Hz	PIC32MZ EF @ 200 MHz

`#include <xc.h>`
 	
`#pragma config POSCMOD = HS`
`#pragma config FNOSC = PRIPLL`
 	
`#pragma config FPLLIDIV = DIV_6`
 	
`#pragma config FPLLMUL = MUL_20`
`#pragma config FPLLODIV = DIV_1`
 	
`#define SYSFREQ (80000000L)`
	`#include <xc.h>`
	
	`#pragma config POSCMOD = HS`
	`#pragma config FNOSC = SPLL`
	`#pragma config FPLLICLK = PLL_POSC`
	`#pragma config FPLLIDIV = DIV_3`
	`#pragma config FPLLRNG = RANGE_5_10_MHZ`
	`#pragma config FPLLMULT = MUL_50`
	`#pragma config FPLLODIV = DIV_2`
	
	`#define SYSFREQ (200000000L)`