Microchip Technology - PIC32MZ0512EFF144T-I/PH Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512eff144t-i-ph

TABLE 1-1: ADC PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
AN36	—	—	B4	8	I	Analog	Analog Input Channels
AN37	—	—	B12	27	I	Analog	
AN38	—	—	B17	43	I	Analog	
AN39	—	—	A22	44	I	Analog	
AN40	—	—	A30	65	I	Analog	
AN41	—	—	B26	66	I	Analog	
AN42	—	—	A31	67	I	Analog	
AN45	11	20	B11	25	I	Analog	
AN46	17	26	B14	37	I	Analog	
AN47	18	27	A19	38	I	Analog	
AN48	21	32	B18	47	I	Analog	
AN49	22	33	A23	48	I	Analog	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION (CONTINUED)

Interrupt Source[1]	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Digital Comparator 5	_ADC_DC5_VECTOR	50	OFF050<17:1>	IFS1<18>	IEC1<18>	IPC12<20:18>	IPC12<17:16>	Yes
ADC Digital Comparator 6	_ADC_DC6_VECTOR	51	OFF051<17:1>	IFS1<19>	IEC1<19>	IPC12<28:26>	IPC12<25:24>	Yes
ADC Digital Filter 1	_ADC_DF1_VECTOR	52	OFF052<17:1>	IFS1<20>	IEC1<20>	IPC13<4:2>	IPC13<1:0>	Yes
ADC Digital Filter 2	_ADC_DF2_VECTOR	53	OFF053<17:1>	IFS1<21>	IEC1<21>	IPC13<12:10>	IPC13<9:8>	Yes
ADC Digital Filter 3	_ADC_DF3_VECTOR	54	OFF054<17:1>	IFS1<22>	IEC1<22>	IPC13<20:18>	IPC13<17:16>	Yes
ADC Digital Filter 4	_ADC_DF4_VECTOR	55	OFF055<17:1>	IFS1<23>	IEC1<23>	IPC13<28:26>	IPC13<25:24>	Yes
ADC Digital Filter 5	_ADC_DF5_VECTOR	56	OFF056<17:1>	IFS1<24>	IEC1<24>	IPC14<4:2>	IPC14<1:0>	Yes
ADC Digital Filter 6	_ADC_DF6_VECTOR	57	OFF057<17:1>	IFS1<25>	IEC1<25>	IPC14<12:10>	IPC14<9:8>	Yes
ADC Fault	_ADC_FAULT_VECTOR	58	OFF058<17:1>	IFS1<26>	IEC1<26>	IPC14<20:18>	IPC14<17:16>	No
ADC Data 0	_ADC_DATA0_VECTOR	59	OFF059<17:1>	IFS1<27>	IEC1<27>	IPC14<28:26>	IPC14<25:24>	Yes
ADC Data 1	_ADC_DATA1_VECTOR	60	OFF060<17:1>	IFS1<28>	IEC1<28>	IPC15<4:2>	IPC15<1:0>	Yes
ADC Data 2	_ADC_DATA2_VECTOR	61	OFF061<17:1>	IFS1<29>	IEC1<29>	IPC15<12:10>	IPC15<9:8>	Yes
ADC Data 3	_ADC_DATA3_VECTOR	62	OFF062<17:1>	IFS1<30>	IEC1<30>	IPC15<20:18>	IPC15<17:16>	Yes
ADC Data 4	_ADC_DATA4_VECTOR	63	OFF063<17:1>	IFS1<31>	IEC1<31>	IPC15<28:26>	IPC15<25:24>	Yes
ADC Data 5	_ADC_DATA5_VECTOR	64	OFF064<17:1>	IFS2<0>	IEC2<0>	IPC16<4:2>	IPC16<1:0>	Yes
ADC Data 6	_ADC_DATA6_VECTOR	65	OFF065<17:1>	IFS2<1>	IEC2<1>	IPC16<12:10>	IPC16<9:8>	Yes
ADC Data 7	_ADC_DATA7_VECTOR	66	OFF066<17:1>	IFS2<2>	IEC2<2>	IPC16<20:18>	IPC16<17:16>	Yes
ADC Data 8	_ADC_DATA8_VECTOR	67	OFF067<17:1>	IFS2<3>	IEC2<3>	IPC16<28:26>	IPC16<25:24>	Yes
ADC Data 9	_ADC_DATA9_VECTOR	68	OFF068<17:1>	IFS2<4>	IEC2<4>	IPC17<4:2>	IPC17<1:0>	Yes
ADC Data 10	_ADC_DATA10_VECTOR	69	OFF069<17:1>	IFS2<5>	IEC2<5>	IPC17<12:10>	IPC17<9:8>	Yes
ADC Data 11	_ADC_DATA11_VECTOR	70	OFF070<17:1>	IFS2<6>	IEC2<6>	IPC17<20:18>	IPC17<17:16>	Yes
ADC Data 12	_ADC_DATA12_VECTOR	71	OFF071<17:1>	IFS2<7>	IEC2<7>	IPC17<28:26>	IPC17<25:24>	Yes
ADC Data 13	_ADC_DATA13_VECTOR	72	OFF072<17:1>	IFS2<8>	IEC2<8>	IPC18<4:2>	IPC18<1:0>	Yes
ADC Data 14	_ADC_DATA14_VECTOR	73	OFF073<17:1>	IFS2<9>	IEC2<9>	IPC18<12:10>	IPC18<9:8>	Yes
ADC Data 15	_ADC_DATA15_VECTOR	74	OFF074<17:1>	IFS2<10>	IEC2<10>	IPC18<20:18>	IPC18<17:16>	Yes
ADC Data 16	_ADC_DATA16_VECTOR	75	OFF075<17:1>	IFS2<11>	IEC2<11>	IPC18<28:26>	IPC18<25:24>	Yes
ADC Data 17	_ADC_DATA17_VECTOR	76	OFF076<17:1>	IFS2<12>	IEC2<12>	IPC19<4:2>	IPC19<1:0>	Yes
ADC Data 18	_ADC_DATA18_VECTOR	77	OFF077<17:1>	IFS2<13>	IEC2<13>	IPC19<12:10>	IPC19<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MZ EF Family Features"** for the list of available peripherals.
2: This interrupt source is not available on 64-pin devices.
3: This interrupt source is not available on 100-pin devices.
4: This interrupt source is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
06EC	OFF107(7)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06F4	OFF109	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06F8	OFF110	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06FC	OFF111	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0700	OFF112	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0704	OFF113	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0708	OFF114	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
070C	OFF115	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0710	OFF116	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0714	OFF117	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0718	OFF118(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
071C	OFF119	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0720	OFF120	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0724	OFF121	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0728	OFF122	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

2: This bit or register is not available on 64-pin devices.

3: This bit or register is not available on devices without a CAN module.

4: This bit or register is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.

7: This bit or register is not available on devices without a Crypto module.

8: This bit or register is not available on 124-pin devices.

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI7SS<3:0>(1)				PRI6SS<3:0>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI5SS<3:0>(1)				PRI4SS<3:0>(1)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI3SS<3:0>				PRI2SS<3:0>(1)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	PRI1SS<3:0>(1)				—	—	—	SS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **PRI7SS<3:0>:** Interrupt with Priority Level 7 Shadow Set bits(1)

`1xxx` = Reserved (by default, an interrupt with a priority level of 7 uses Shadow Set 0)
`0111` = Interrupt with a priority level of 7 uses Shadow Set 7
`0110` = Interrupt with a priority level of 7 uses Shadow Set 6
•
•
•
`0001` = Interrupt with a priority level of 7 uses Shadow Set 1
`0000` = Interrupt with a priority level of 7 uses Shadow Set 0

bit 27-24 **PRI6SS<3:0>:** Interrupt with Priority Level 6 Shadow Set bits(1)

`1xxx` = Reserved (by default, an interrupt with a priority level of 6 uses Shadow Set 0)
`0111` = Interrupt with a priority level of 6 uses Shadow Set 7
`0110` = Interrupt with a priority level of 6 uses Shadow Set 6
•
•
•
`0001` = Interrupt with a priority level of 6 uses Shadow Set 1
`0000` = Interrupt with a priority level of 6 uses Shadow Set 0

bit 23-20 **PRI5SS<3:0>:** Interrupt with Priority Level 5 Shadow Set bits(1)

`1xxx` = Reserved (by default, an interrupt with a priority level of 5 uses Shadow Set 0)
`0111` = Interrupt with a priority level of 5 uses Shadow Set 7
`0110` = Interrupt with a priority level of 5 uses Shadow Set 6
•
•
•
`0001` = Interrupt with a priority level of 5 uses Shadow Set 1
`0000` = Interrupt with a priority level of 5 uses Shadow Set 0

bit 19-16 **PRI4SS<3:0>:** Interrupt with Priority Level 4 Shadow Set bits(1)

`1xxx` = Reserved (by default, an interrupt with a priority level of 4 uses Shadow Set 0)
`0111` = Interrupt with a priority level of 4 uses Shadow Set 7
`0110` = Interrupt with a priority level of 4 uses Shadow Set 6
•
•
•
`0001` = Interrupt with a priority level of 4 uses Shadow Set 1
`0000` = Interrupt with a priority level of 4 uses Shadow Set 0

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = `0`.

REGISTER 11-5: USBIE0CSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 0) (CONTINUED)

bit 21 **SENDSTALL:** Send Stall Control bit (*Device mode*)
1 = Terminate the current transaction and transmit a STALL handshake. This bit is automatically cleared.
0 = Do not send STALL handshake.

REQPKT: IN transaction Request Control bit (*Host mode*)
1 = Request an IN transaction. This bit is cleared when the RXPKTRDY bit is set.
0 = Do not request an IN transaction

bit 20 **SETUPEND:** Early Control Transaction End Status bit (*Device mode*)
1 = A control transaction ended before the DATAEND bit has been set. An interrupt will be generated and the FIFO flushed at this time.
0 = Normal operation

This bit is cleared by writing a '1' to the SVCSETEND bit in this register.

ERROR: No Response Error Status bit (*Host mode*)
1 = Three attempts have been made to perform a transaction with no response from the peripheral. An interrupt is generated.
0 = Clear this flag. Software must write a '0' to this bit to clear it.

bit 19 **DATAEND:** End of Data Control bit (*Device mode*)
The software sets this bit when:
- Setting TXPKTRDY for the last data packet
- Clearing RXPKTRDY after unloading the last data packet
- Setting TXPKTRDY for a zero length data packet

Hardware clears this bit.

SETUPPKT: Send a SETUP token Control bit (*Host mode*)
1 = When set at the same time as the TXPKTRDY bit is set, the module sends a SETUP token instead of an OUT token for the transaction
0 = Normal OUT token operation

Setting this bit also clears the Data Toggle.

bit 18 **SENTSTALL:** STALL sent status bit (*Device mode*)
1 = STALL handshake has been transmitted
0 = Software clear of bit

RXSTALL: STALL handshake received Status bit (*Host mode*)
1 = STALL handshake was received
0 = Software clear of bit

bit 17 **TXPKTRDY:** TX Packet Ready Control bit
1 = Data packet has been loaded into the FIFO. It is cleared automatically.
0 = No data packet is ready for transmit

bit 16 **RXPKTRDY:** RX Packet Ready Status bit
1 = Data packet has been received. Interrupt is generated (when enabled) when this bit is set.
0 = No data packet has been received

This bit is cleared by setting the SVCRPR bit.

bit 15-0 **Unimplemented:** Read as '0'

TABLE 12-22: PERIPHERAL PIN SELECT INPUT REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1404	INT1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT1R<3:0>				0000
1408	INT2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT2R<3:0>				0000
140C	INT3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT3R<3:0>				0000
1410	INT4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT4R<3:0>				0000
1418	T2CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T2CKR<3:0>				0000
141C	T3CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T3CKR<3:0>				0000
1420	T4CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T4CKR<3:0>				0000
1424	T5CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T5CKR<3:0>				0000
1428	T6CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T6CKR<3:0>				0000
142C	T7CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T7CKR<3:0>				0000
1430	T8CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T8CKR<3:0>				0000
1434	T9CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T9CKR<3:0>				0000
1438	IC1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC1R<3:0>				0000
143C	IC2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC2R<3:0>				0000
1440	IC3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC3R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

2: This register is not available on devices without a CAN module.

The timer source for each Input Capture module depends on the setting of the ICACLK bit in the CFGCON register. The available configurations are shown in Table 17-1.

TABLE 17-1: TIMER SOURCE CONFIGURATIONS

Input Capture Module	Timerx	Timery
ICACLK (CFGCON<17>) = 0		
IC1 • • • IC9	Timer2 • • • Timer2	Timer3 • • • Timer3
ICACLK (CFGCON<17>) = 1		
IC1	Timer4	Timer5
IC2	Timer4	Timer5
IC3	Timer4	Timer5
IC4	Timer2	Timer3
IC5	Timer2	Timer3
IC6	Timer2	Timer3
IC7	Timer6	Timer7
IC8	Timer6	Timer7
IC9	Timer6	Timer7

REGISTER 20-9: SQI1INTSTAT: SQI INTERRUPT STATUS REGISTER (CONTINUED)

bit 2 **TXTHRIF:** Transmit Buffer Threshold Interrupt Flag bit
1 = Transmit buffer has more than TXINTTHR words of space available
0 = Transmit buffer has less than TXINTTHR words of space available

bit 1 **TXFULLIF:** Transmit Buffer Full Interrupt Flag bit
1 = The transmit buffer is full
0 = The transmit buffer is not full

bit 0 **TXEMPTYIF:** Transmit Buffer Empty Interrupt Flag bit
1 = The transmit buffer is empty
0 = The transmit buffer has content

Note 1: In Boot/XIP mode, the POR value of the receive buffer threshold is zero. Therefore, this bit will be set to a ‘1’, immediately after a POR until a read request on the System Bus is received.

Note: The bits in the register are cleared by writing a '1' to the corresponding bit position.

REGISTER 20-18: SQI1BDPOLLCON: SQI BUFFER DESCRIPTOR POLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLLCON<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLLCON<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **POLLCON<15:0>:** Buffer Descriptor Processor Poll Status bits

These bits indicate the number of cycles the BDP would wait before refetching the descriptor control word if the previous descriptor fetched was disabled.

REGISTER 20-19: SQI1BDTXDSTAT: SQI BUFFER DESCRIPTOR DMA TRANSMIT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-x	R-x	R-x	R-x	U-0
	—	—	—	TXSTATE<3:0>				—
23:16	U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
	—	—	—	TXBUFCNT<4:0>				
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	TXCURBUFLEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28-25 **TXSTATE<3:0>:** Current DMA Transmit State Status bits

These bits provide information on the current DMA receive states.

bit 24-21 **Unimplemented:** Read as ‘0’

bit 20-16 **TXBUFCNT<4:0>:** DMA Buffer Byte Count Status bits

These bits provide information on the internal FIFO space.

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **TXCURBUFLEN<7:0>:** Current DMA Transmit Buffer Length Status bits

These bits provide the length of the current DMA transmit buffer.

REGISTER 23-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

bit 7-6 **CSF<1:0>:** Chip Select Function bits[1]
- 11 = Reserved
- 10 = PMCS1 and PMCS2 function as Chip Select
- 01 = PMCS2 functions as Chip Select and PMCS1 functions as address bit 14
- 00 = PMCS1 and PMCS2 function as address bit 14 and address bit 15

bit 5 **ALP:** Address Latch Polarity bit[1]
- 1 = Active-high (PMALL and PMALH)
- 0 = Active-low (PMALL and PMALH)

bit 4 **CS2P:** Chip Select 2 Polarity bit[1]
- 1 = Active-high (PMCS2)
- 0 = Active-low (PMCS2)

bit 3 **CS1P:** Chip Select 1 Polarity bit[1]
- 1 = Active-high (PMCS1)
- 0 = Active-low (PMCS1)

bit 2 **Unimplemented:** Read as '0'

bit 1 **WRSP:** Write Strobe Polarity bit

For Slave Modes and Master mode 2 (MODE<1:0> = 00,01,10):
- 1 = Write strobe active-high (PMWR)
- 0 = Write strobe active-low (PMWR)

For Master mode 1 (MODE<1:0> = 11):
- 1 = Enable strobe active-high (PMENB)
- 0 = Enable strobe active-low (PMENB)

bit 0 **RDSP:** Read Strobe Polarity bit

For Slave modes and Master mode 2 (MODE<1:0> = 00,01,10):
- 1 = Read Strobe active-high (PMRD)
- 0 = Read Strobe active-low (PMRD)

For Master mode 1 (MODE<1:0> = 11):
- 1 = Read/write strobe active-high (PMRD/PMWR)
- 0 = Read/write strobe active-low (PMRD/PMWR)

Note 1: These bits have no effect when their corresponding pins are used as address lines.

REGISTER 23-8: PMWADDR: PARALLEL PORT WRITE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WCS2(1)	WCS1(3)	WADDR<13:8>					
	WADDR15(2)	WADDR14(4)						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **WCS2:** Chip Select 2 bit(1)
1 = Chip Select 2 is active
0 = Chip Select 2 is inactive

bit 15 **WADDR<15>:** Target Address bit 15(2)

bit 14 **WCS1:** Chip Select 1 bit(3)
1 = Chip Select 1 is active
0 = Chip Select 1 is inactive

bit 14 **WADDR<14>:** Target Address bit 14(4)

bit 13-0 **WADDR<13:0>:** Address bits

Note 1: When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.
2: When the CSF<1:0> bits (PMCON<7:6>) = 00.
3: When the CSF<1:0> bits (PMCON<7:6>) = 10.
4: When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

Note: This register is only used when the DUALBUF bit (PMCON<17>) is set to ‘1’.

25.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

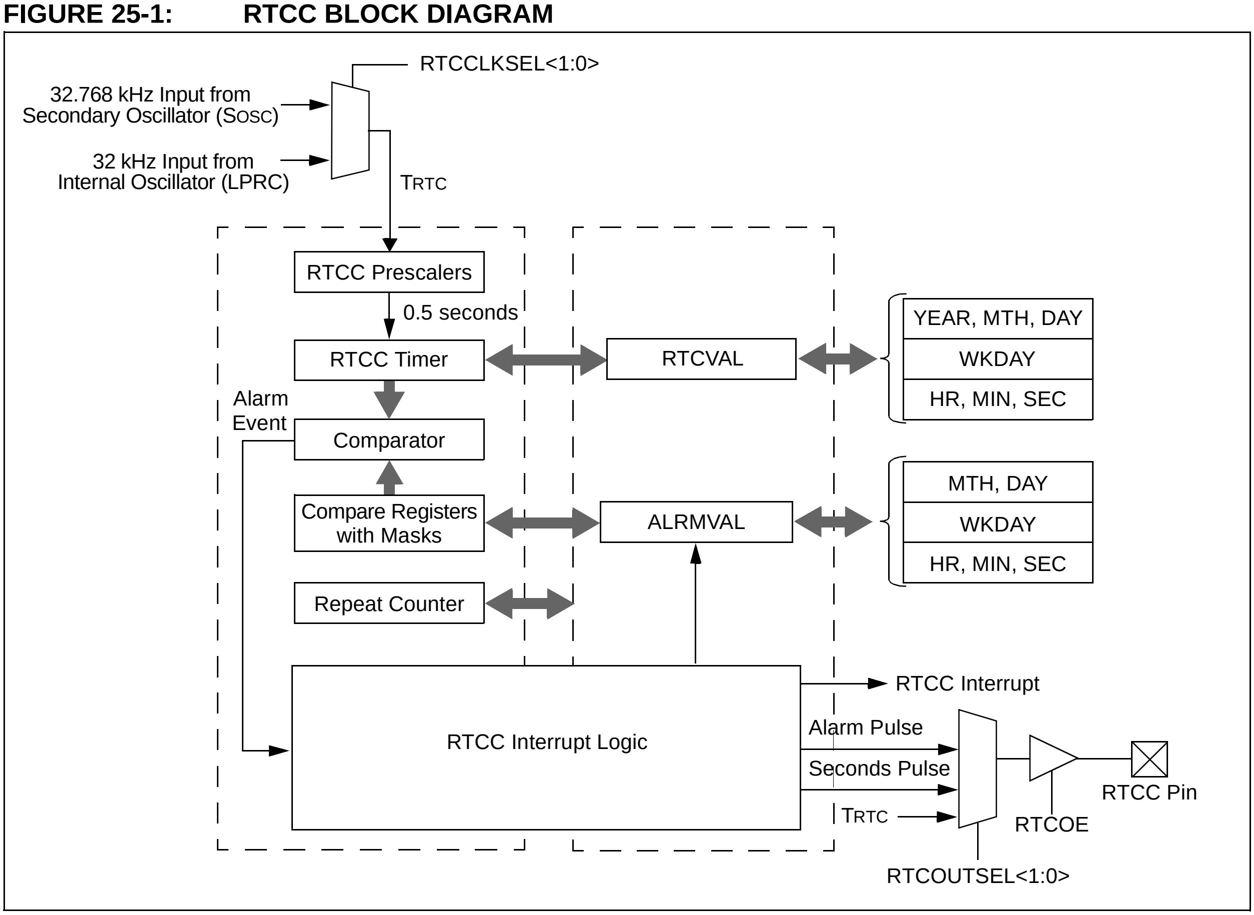
Note:	This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

The following are key features of the RTCC module:

- Time: hours, minutes, and seconds
- 24-hour format (military time)
- Visibility of one-half second period
- Provides calendar: Weekday, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month, and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Uses external 32.768 kHz crystal or 32 kHz internal oscillator
- Alarm pulse, seconds clock, or internal clock output on RTCC pin

FIGURE 25-1: RTCC BLOCK DIAGRAM



REGISTER 26-5: CESTAT: CRYPTO ENGINE STATUS REGISTER (CONTINUED)

bit 16 **ACTIVE:** Buffer Descriptor Processor Status bit

1 = BDP is active
0 = BDP is idle

bit 15-0 **BDCTRL<15:0>:** Descriptor Control Word Status bits

These bits contain the Control Word for the current Buffer Descriptor.

REGISTER 28-11: ADCCSS2: ADC COMMON SCAN SELECT REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	CSS44	CSS43	CSS42(2)	CSS41(2)	CSS40(2)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS39(2)	CSS38(2)	CSS37(2)	CSS36(2)	CSS35(2)	CSS34(1)	CSS33(1)	CSS32(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as ‘0’

bit 12-0 **CSS44:CSS32:** Analog Common Scan Select bits
Analog inputs 44 to 32 are always Class 3, as there are only 32 triggers available.
1 = Select AN*x* for input scan
0 = Skip AN*x* for input scan

Note 1: This bit is not available on 64-pin devices.
2: This bit is not available on 64-pin and 100-pin devices.

REGISTER 28-32: ADCANCON: ADC ANALOG WARM-UP CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	WKUPCLKCNT<3:0>			
23:16	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WKIEN7	—	—	WKIEN4	WKIEN3	WKIEN2	WKIEN1	WKIEN0
15:8	R-0, HS, HC	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	WKRDY7	—	—	WKRDY4	WKRDY3	WKRDY2	WKRDY1	WKRDY0
7:0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ANEN7	—	—	ANEN4	ANEN3	ANEN2	ANEN1	ANEN0

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as ‘0’

bit 27-24 **WKUPCLKCNT<3:0>:** Wake-up Clock Count bits

These bits represent the number of ADC clocks required to warm-up the ADC module before it can perform conversion. Although the clocks are specific to each ADC, the WKUPCLKCNT bit is common to all ADC modules.

1111 = 2^{15} = 32,768 clocks
•
•
•
0110 = 2^6 = 64 clocks
0101 = 2^5 = 32 clocks
0100 = 2^4 = 16 clocks
0011 = 2^4 = 16 clocks
0010 = 2^4 = 16 clocks
0001 = 2^4 = 16 clocks
0000 = 2^4 = 16 clocks

bit 23 **WKIEN7:** Shared ADC (ADC7) Wake-up Interrupt Enable bit

1 = Enable interrupt and generate interrupt when the WKRDY7 status bit is set
0 = Disable interrupt

bit 22-21 **Unimplemented:** Read as ‘0’

bit 20-16 **WKIEN4:WKIEN0:** ADC4-ADC0 Wake-up Interrupt Enable bit

1 = Enable interrupt and generate interrupt when the WKRDYx status bit is set
0 = Disable interrupt

bit 15 **WKRDY7:** Shared ADC (ADC7) Wake-up Status bit

1 = ADC7 Analog and Bias circuitry ready after the wake-up count number $2^{WKUPEXP}$ clocks after setting ANEN7 to ‘1’
0 = ADC7 Analog and Bias circuitry is not ready

Note: This bit is cleared by hardware when the ANEN7 bit is cleared

bit 14-13 **Unimplemented:** Read as ‘0’

bit 12-8 **WKRDY4:WKRDY0:** ADC4-ADC0 Wake-up Status bit

1 = ADCx Analog and Bias circuitry ready after the wake-up count number $2^{WKUPEXP}$ clocks after setting ANEN*x* to ‘1’
0 = ADCx Analog and Bias circuitry is not ready

Note: These bits are cleared by hardware when the ANEN*x* bit is cleared

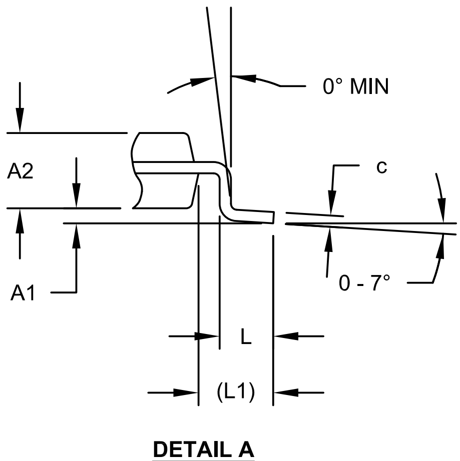
REGISTER 29-13: CiFLTCON3: CAN FILTER CONTROL REGISTER 3 (CONTINUED)

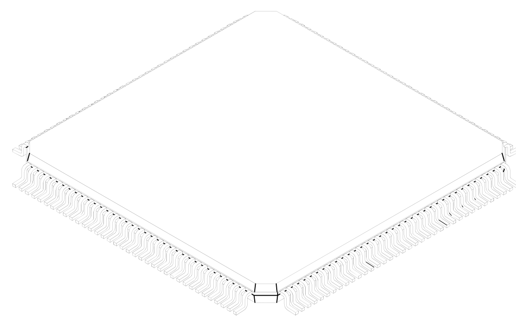
bit 15	**FLTEN13:** Filter 13 Enable bit 1 = Filter is enabled 0 = Filter is disabled
bit 14-13	**MSEL13<1:0>:** Filter 13 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected
bit 12-8	**FSEL13<4:0>:** FIFO Selection bits 11111 = Message matching filter is stored in FIFO buffer 31 11110 = Message matching filter is stored in FIFO buffer 30 • • • 00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0
bit 7	**FLTEN12:** Filter 12 Enable bit 1 = Filter is enabled 0 = Filter is disabled
bit 6-5	**MSEL12<1:0>:** Filter 12 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected
bit 4-0	**FSEL12<4:0>:** FIFO Selection bits 11111 = Message matching filter is stored in FIFO buffer 31 11110 = Message matching filter is stored in FIFO buffer 30 • • • 00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is ‘0’.

144-Lead Plastic Thin Quad Flatpack (PH)-16x16x1mm Body, 2.00 mm Footprint [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	144		
Lead Pitch	e	0.40 BSC		
Overall Height	A	-	-	1.20
Molded PackageThickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Overall Width	D	18.00 BSC		
Overall Length	E	18.00 BSC		
Molded Body Width	D1	16.00 BSC		
Molded Body Length	E1	16.00 BSC		
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.13	-	0.23

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-155B Sheet 2 of 2

A.3 CPU

The CPU in the PIC32MZ EF family of devices has been changed to the MIPS32 M-Class MPU architecture. This CPU includes DSP ASE, internal data and instruction L1 caches, and a TLB-based MMU.

Table A-4 summarizes some of the key differences (indicated by **Bold** type) in the internal CPU registers.

TABLE A-4: CPU DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
L1 Data and Instruction Cache and Prefetch Wait States	
On PIC32MX devices, the cache was included in the prefetch module outside the CPU.	On PIC32MZ EF devices, the CPU has a separate L1 instruction and data cache in the core. The PREFEN<1:0> bits still enable the prefetch module; however, the K0<2:0> bits in the CP0 registers controls the internal L1 cache for the designated regions.
PREFEN<1:0> (**CHECON**<5:4>) **11 = Enable predictive prefetch for both cacheable and non-cacheable regions** **10 = Enable predictive prefetch for non-cacheable regions only** **01 = Enable predictive prefetch for cacheable regions only** 00 = Disable predictive prefetch	PREFEN<1:0> (**PRECON**<5:4>) **11 = Enable predictive prefetch for any address** **10 = Enable predictive prefetch for CPU instructions and CPU data** **01 = Enable predictive prefetch for CPU instructions only** 00 = Disable predictive prefetch
DCSZ<1:0> (CHECON<9:8>) Changing these bits causes all lines to be reinitialized to the "invalid" state. 11 = Enable data caching with a size of 4 lines 10 = Enable data caching with a size of 2 lines 01 = Enable data caching with a size of 1 line 00 = Disable data caching CHECOH (CHECON<16>) 1 = Invalidate all data and instruction lines 0 = Invalidate all data and instruction lines that are not locked	**K0<2:0> (CP0 Reg 16, Select 0)** **011 = Cacheable, non-coherent, write-back, write allocate** **010 = Uncached** **001 = Cacheable, non-coherent, write-through, write allocate** **000 = Cacheable, non-coherent, write-through, no write allocate**
	The Program Flash Memory read wait state frequency points have changed in PIC32MZ EF devices. The register for accessing the PFMWS field has changed from CHECON to PRECON.
PFMWS<2:0> (**CHECON**<2:0>) 111 = Seven Wait states 110 = Six Wait states 101 = Five Wait states 100 = Four Wait states 011 = Three Wait states 010 = Two Wait states **(61-80 MHz)** 001 = One Wait state **(31-60 MHz)** 000 = Zero Wait state **(0-30 MHz)**	PFMWS<2:0> (**PRECON**<2:0>) 111 = Seven Wait states • • • 100 = Four Wait states **(200-252 MHz)** 011 = Reserved 010 = Two Wait states **(133-200 MHz)** 001 = One Wait state **(66-133 MHz)** 000 = Zero Wait states **(0-66 MHz)** **Note:** Wait states listed are for ECC enabled.
Core Instruction Execution	
On PIC32MX devices, the CPU can execute MIPS16e instructions and uses a 16-bit instruction set, which reduces memory size.	On PIC32MZ EF devices, the CPU can operate a mode called microMIPS. microMIPS mode is an enhanced MIPS32® instruction set that uses both 16-bit and 32-bit opcodes. This mode of operation reduces memory size with minimum performance impact.
MIPS16e®	**microMIPS™** The BOOTISA (DEVCFG0<6>) Configuration bit controls the MIPS32 and microMIPS modes for boot and exception code. 1 = Boot code and Exception code is MIPS32® (ISAONEXC bit is set to '0' and the ISA<1:0> bits are set to '10' in the CP0 Config3 register) 0 = Boot code and Exception code is microMIPS™ (ISAONEXC bit is set to '1' and the ISA<1:0> bits are set to '11' in the CP0 Config3 register)

B.3 CPU

The CPU in PIC32MZ EC devices is the microAptiv™ MPU architecture. The CPU in the PIC32MZ EF devices is the Series 5 Warrior M-Class M5150 MPU architecture. Most PIC32MZ EF M-Class core features are identical to the microAptiv™ core in PIC32MZ EC devices. The main differences are that in PIC32MZ EF devices, a floating-point unit (FPU) is included for improved math performance, and PC Sampling for performance measurement.

B.4 System Bus

The system bus on PIC32MZ EF devices is similar to the system bus on PIC32MZ EC devices. There are two key differences listed in Table B-3.

TABLE B-3: SYSTEM BUS DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
Permission Groups during NMI	
On PIC32MZ EC devices, the permission group in which the CPU is part of is lost during NMI handling, and must be manually restored.	On PIC32MZ EF devices, the prior permission group is preserved, and is restored when the CPU returns from the NMI handler.
DMA Access	
The DMA can access the peripheral registers on Peripheral Bus 1.	On PIC32MZ EF devices, the DMA no longer has access to registers on Peripheral Bus 1. Refer to Table 4-4 for details on which peripherals are now excluded.

B.5 Flash Controller

The Flash controller on PIC32MZ EF devices adds the ability both to control boot Flash aliasing, and for locking the current swap settings. Table B-4 lists theses differences.

TABLE B-4: FLASH CONTROLLER DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
Boot Flash Aliasing	
On PIC32MZ EC devices, Boot Flash aliasing is done through the DEVSEQ0 register, but no further changes are possible without rebooting the processor.	On PIC32MZ EF devices, the initial Boot Flash aliasing is determined by the DEVSEQ3 register, but the BFSWAP bit (NVMCON<6>) reflects the state of the aliasing, and can be modified to change it during run-time. BFSWAP (NVMCON<6>) 1 = Boot Flash Bank 2 is mapped to the lower boot alias, and Boot Flash bank 1 is mapped to the upper boot alias 0 = Boot Flash Bank 1 is mapped to the lower boot alias, and Boot Flash Bank 2 is mapped to the upper boot alias
PFM and BFM Swap Locking	
On PIC32MZ EC devices, the swapping of PFM is always available.	On PIC32MZ EF devices, a new control, SWAPLOCK<1:0> (NVMCON2<7:6>) allows the locking of PFSWAP and BFSWAP bits, and can restrict any further changes. SWAPLOCK<1:0> (NVMCON2<7:6>) 11 = PFSWAP and BFSWAP are not writable and SWAPLOCK is not writable 10 = PFSWAP and BFSWAP are not writable and SWAPLOCK is writable 01 = PFSWAP and BFSWAP are not writable and SWAPLOCK is writable 00 = PFSWAP and BFSWAP are writable and SWAPLOCK is writable