Microchip Technology - PIC32MZ0512EFF144T-I/PL Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512eff144t-i-pl

TABLE 3: PIN NAMES FOR 100-PIN DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)100
PIC32MZ1024EF(G/H/M)100
PIC32MZ1024EF(E/F/K)100
PIC32MZ2048EF(G/H/M)100

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
71	EMDIO/AEMDIO/RPD0/RTCC/INT0/RD0	86	EBID10/ETXD0/RPF1/PMD10/RF1
72	SOSCI/RPC13/RC13	87	EBID9/ETXERR/RPG1/PMD9/RG1
73	SOSCO/RPC14/T1CK/RC14	88	EBID8/RPG0/PMD8/RG0
74	VDD	89	TRCLK/SQICLK/RA6
75	VSS	90	TRD3/SQID3/RA7
76	RPD1/SCK1/RD1	91	EBID0/PMD0/RE0
77	EBID14/ETXEN/RPD2/PMD14/RD2	92	VSS
78	EBID15/ETXCLK/RPD3/PMD15/RD3	93	VDD
79	EBID12/ETXD2/RPD12/PMD12/RD12	94	EBID1/PMD1/RE1
80	EBID13/ETXD3/PMD13/RD13	95	TRD2/SQID2/RG14
81	$\overline{\text{SQICS0}}$/RPD4/RD4	96	TRD1/SQID1/RG12
82	$\overline{\text{SQICS1}}$/RPD5/RD5	97	TRD0/SQID0/RG13
83	VDD	98	EBID2/PMD2/RE2
84	VSS	99	EBID3/RPE3/PMD3/RE3
85	EBID11/ETXD1/RPF0/PMD11/RF0	100	EBID4/AN18/PMD4/RE4

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

TABLE 1-1: ADC PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
AN36	—	—	B4	8	I	Analog	Analog Input Channels
AN37	—	—	B12	27	I	Analog	
AN38	—	—	B17	43	I	Analog	
AN39	—	—	A22	44	I	Analog	
AN40	—	—	A30	65	I	Analog	
AN41	—	—	B26	66	I	Analog	
AN42	—	—	A31	67	I	Analog	
AN45	11	20	B11	25	I	Analog	
AN46	17	26	B14	37	I	Analog	
AN47	18	27	A19	38	I	Analog	
AN48	21	32	B18	47	I	Analog	
AN49	22	33	A23	48	I	Analog	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

3.7 M-Class Core Configuration

Register 3-1 through Register 3-4 show the default configuration of the M-Class core, which is included on the PIC32MZ EF family of devices.

REGISTER 3-1: CONFIG: CONFIGURATION REGISTER; CP0 REGISTER 16, SELECT 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	ISP
23:16	R-0	R-0	R-1	R-0	U-0	R-1	R-0	R-0
	DSP	UDI	SB	MDU	—	MM<1:0>		BM
15:8	R-0	R-0	R-0	R-0	R-0	R-1	R-0	R-0
	BE	AT<1:0>		AR<2:0>			MT<2:1>	
7:0	R-1	U-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-0
	MT<0>	—	—	—	—	K0<2:0>		

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to '1' to indicate the presence of the Config1 register.

bit 30-25 **Unimplemented:** Read as '0'

bit 24 **ISP:** Instruction Scratch Pad RAM bit
0 = Instruction Scratch Pad RAM is not implemented

bit 23 **DSP:** Data Scratch Pad RAM bit
0 = Data Scratch Pad RAM is not implemented

bit 22 **UDI:** User-defined bit
0 = CorExtend User-Defined Instructions are not implemented

bit 21 **SB:** SimpleBE bit
1 = Only Simple Byte Enables are allowed on the internal bus interface

bit 20 **MDU:** Multiply/Divide Unit bit
0 = Fast, high-performance MDU

bit 19 **Unimplemented:** Read as '0'

bit 18-17 **MM<1:0>:** Merge Mode bits
10 = Merging is allowed

bit 16 **BM:** Burst Mode bit
0 = Burst order is sequential

bit 15 **BE:** Endian Mode bit
0 = Little-endian

bit 14-13 **AT<1:0>:** Architecture Type bits
00 = MIPS32

bit 12-10 **AR<2:0>:** Architecture Revision Level bits
001 = MIPS32 Release 2

bit 9-7 **MT<2:0>:** MMU Type bits
001 = M-Class MPU Microprocessor core uses a TLB-based MMU

bit 6-3 **Unimplemented:** Read as '0'

bit 2-0 **K0<2:0>:** Kseg0 Coherency Algorithm bits
011 = Cacheable, non-coherent, write-back, write allocate
010 = Uncached
001 = Cacheable, non-coherent, write-through, write allocate
000 = Cacheable, non-coherent, write-through, no write allocate
All other values are not used and mapped to other values. 100, 101, and 110 are mapped to 010. 111 is mapped to 010.

TABLE 4-11: SYSTEM BUS TARGET 3 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8C20	SBT3ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8C24	SBT3ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8C28	SBT3ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8C30	SBT3ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C38	SBT3ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C40	SBT3REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C50	SBT3RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C58	SBT3WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C60	SBT3REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C70	SBT3RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C78	SBT3WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C80	SBT3REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C90	SBT3RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C98	SBT3WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

7.2 Interrupts

The PIC32MZ EF family uses variable offsets for vector spacing. This allows the interrupt vector spacing to be configured according to application needs. A unique interrupt vector offset can be set for each vector using its associated OFFx register.

For details on the Variable Offset feature, refer to **8.5.2 "Variable Offset"** in **Section 8. "Interrupt Controller"** (DS60001108) of the *"PIC32 Family Reference Manual"*.

Table 7-2 provides the Interrupt IRQ, vector and bit location information.

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Highest Natural Order Priority								
Core Timer Interrupt	_CORE_TIMER_VECTOR	0	OFF000<17:1>	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
Core Software Interrupt 0	_CORE_SOFTWARE_0_VECTOR	1	OFF001<17:1>	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
Core Software Interrupt 1	_CORE_SOFTWARE_1_VECTOR	2	OFF002<17:1>	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
External Interrupt 0	_EXTERNAL_0_VECTOR	3	OFF003<17:1>	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
Timer1	_TIMER_1_VECTOR	4	OFF004<17:1>	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
Input Capture 1 Error	_INPUT_CAPTURE_1_ERROR_VECTOR	5	OFF005<17:1>	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes
Input Capture 1	_INPUT_CAPTURE_1_VECTOR	6	OFF006<17:1>	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>	Yes
Output Compare 1	_OUTPUT_COMPARE_1_VECTOR	7	OFF007<17:1>	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>	No
External Interrupt 1	_EXTERNAL_1_VECTOR	8	OFF008<17:1>	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>	No
Timer2	_TIMER_2_VECTOR	9	OFF009<17:1>	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>	No
Input Capture 2 Error	_INPUT_CAPTURE_2_ERROR_VECTOR	10	OFF010<17:1>	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>	Yes
Input Capture 2	_INPUT_CAPTURE_2_VECTOR	11	OFF011<17:1>	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>	Yes
Output Compare 2	_OUTPUT_COMPARE_2_VECTOR	12	OFF012<17:1>	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>	No
External Interrupt 2	_EXTERNAL_2_VECTOR	13	OFF013<17:1>	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>	No
Timer3	_TIMER_3_VECTOR	14	OFF014<17:1>	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>	No
Input Capture 3 Error	_INPUT_CAPTURE_3_ERROR_VECTOR	15	OFF015<17:1>	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>	Yes
Input Capture 3	_INPUT_CAPTURE_3_VECTOR	16	OFF016<17:1>	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>	Yes
Output Compare 3	_OUTPUT_COMPARE_3_VECTOR	17	OFF017<17:1>	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>	No
External Interrupt 3	_EXTERNAL_3_VECTOR	18	OFF018<17:1>	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>	No
Timer4	_TIMER_4_VECTOR	19	OFF019<17:1>	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>	No
Input Capture 4 Error	_INPUT_CAPTURE_4_ERROR_VECTOR	20	OFF020<17:1>	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>	Yes
Input Capture 4	_INPUT_CAPTURE_4_VECTOR	21	OFF021<17:1>	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MZ EF Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

4: This interrupt source is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
01F0	IPC11	31:16	—	—	—	ADCDC2IP<2:0>			ADCDC2IS<1:0>		—	—	—	ADCDC1IP<2:0>			ADCDC1IS<1:0>		0000
		15:0	—	—	—	ADCFIFOIP<2:0>			ADCFIFOIS<1:0>		—	—	—	ADCIP<2:0>			ADCIS<1:0>		0000
0200	IPC12	31:16	—	—	—	ADCDC6IP<2:0>			ADCDC6IS<1:0>		—	—	—	ADCDC5IP<2:0>			ADCDC5IS<1:0>		0000
		15:0	—	—	—	ADCDC4IP<2:0>			ADCDC4IS<1:0>		—	—	—	ADCDC3IP<2:0>			ADCDC3IS<1:0>		0000
0210	IPC13	31:16	—	—	—	ADCDF4IP<2:0>			ADCDF4IS<1:0>		—	—	—	ADCDF3IP<2:0>			ADCDF3IS<1:0>		0000
		15:0	—	—	—	ADCDF2IP<2:0>			ADCDF2IS<1:0>		—	—	—	ADCDF1IP<2:0>			ADCDF1IS<1:0>		0000
0220	IPC14	31:16	—	—	—	ADCD0IP<2:0>			ADCD0IS<1:0>		—	—	—	ADCDFLTIP<2:0>			ADCDFLTIS<1:0>		0000
		15:0	—	—	—	ADCDF6IP<2:0>			ADCDF6IS<1:0>		—	—	—	ADCDF5IP<2:0>			ADCDF5IS<1:0>		0000
0230	IPC15	31:16	—	—	—	ADCD4IP<2:0>			ADCD4IS<1:0>		—	—	—	ADCD3IP<2:0>			ADCD3IS<1:0>		0000
		15:0	—	—	—	ADCD2IP<2:0>			ADCD2IS<1:0>		—	—	—	ADCD1IP<2:0>			ADCD1IS<1:0>		0000
0240	IPC16	31:16	—	—	—	ADCD8IP<2:0>			ADCD8IS<1:0>		—	—	—	ADCD7IP<2:0>			ADCD7IS<1:0>		0000
		15:0	—	—	—	ADCD6IP<2:0>			ADCD6IS<1:0>		—	—	—	ADCD5IP<2:0>			ADCD5IS<1:0>		0000
0250	IPC17	31:16	—	—	—	ADCD12IP<2:0>			ADCD12IS<1:0>		—	—	—	ADCD11IP<2:0>			ADCD11IS<1:0>		0000
		15:0	—	—	—	ADCD10IP<2:0>			ADCD10IS<1:0>		—	—	—	ADCD9IP<2:0>			ADCD9IS<1:0>		0000
0260	IPC18	31:16	—	—	—	ADCD16IP<2:0>			ADCD16IS<1:0>		—	—	—	ADCD15IP<2:0>			ADCD15IS<1:0>		0000
		15:0	—	—	—	ADCD14IP<2:0>			ADCD14IS<1:0>		—	—	—	ADCD13IP<2:0>			ADCD13IS<1:0>		0000
0270	IPC19	31:16	—	—	—	ADCD20IP<2:0>(2)			ADCD20IS<1:0>(2)		—	—	—	ADCD19IP<2:0>(2)			ADCD19IS<1:0>(2)		0000
		15:0	—	—	—	ADCD18IP<2:0>			ADCD18IS<1:0>		—	—	—	ADCD17IP<2:0>			ADCD17IS<1:0>		0000
0280	IPC20	31:16	—	—	—	ADCD24IP<2:0>(2)			ADCD24IS<1:0>(2)		—	—	—	ADCD23IP<2:0>(2)			ADCD23IS<1:0>(2)		0000
		15:0	—	—	—	ADCD22IP<2:0>(2)			ADCD22IS<1:0>(2)		—	—	—	ADCD21IP<2:0>(2)			ADCD21IS<1:0>(2)		0000
0290	IPC21	31:16	—	—	—	ADCD28IP<2:0>(2)			ADCD28IS<1:0>(2)		—	—	—	ADCD27IP<2:0>(2)			ADCD27IS<1:0>(2)		0000
		15:0	—	—	—	ADCD26IP<2:0>(2)			ADCD26IS<1:0>(2)		—	—	—	ADCD25IP<2:0>(2)			ADCD25IS<1:0>(2)		0000
02A0	IPC22	31:16	—	—	—	ADCD32IP<2:0>(2)			ADCD32IS<1:0>(2)		—	—	—	ADCD31IP<2:0>(2)			ADCD31IS<1:0>(2)		0000
		15:0	—	—	—	ADCD30IP<2:0>(2)			ADCD30IS<1:0>(2)		—	—	—	ADCD29IP<2:0>(2)			ADCD29IS<1:0>(2)		0000
02B0	IPC23	31:16	—	—	—	ADCD36IP<2:0>(2,4)			ADCD36IS<1:0>(2,4)		—	—	—	ADCD35IP<2:0>(2,4)			ADCD35IS<1:0>(2,4)		0000
		15:0	—	—	—	ADCD34IP<2:0>(2)			ADCD34IS<1:0>(2)		—	—	—	ADCD33IP<2:0>(2)			ADCD33IS<1:0>(2)		0000
02C0	IPC24	31:16	—	—	—	ADCD40IP<2:0>(2,4)			ADCD40IS<1:0>(2,4)		—	—	—	ADCD39IP<2:0>(2,4)			ADCD39IS<1:0>(2,4)		0000
		15:0	—	—	—	ADCD38IP<2:0>(2,4)			ADCD38IS<1:0>(2,4)		—	—	—	ADCD37IP<2:0>(2,4)			ADCD37IS<1:0>(2,4)		0000
02D0	IPC25	31:16	—	—	—	ADCD44IP<2:0>			ADCD44IS<1:0>		—	—	—	ADCD43IP<2:0>			ADCD43IS<1:0>		0000
		15:0	—	—	—	ADCD42IP<2:0>(2,4)			ADCD42IS<1:0>(2,4)		—	—	—	ADCD41IP<2:0>(2,4)			ADCD41IS<1:0>(2,4)		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

16.1 Watchdog Timer Control Registers

TABLE 16-1: WATCHDOG TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0800	WDTCON(1)	31:16	WDTCLRKEY<15:0>																0000
		15:0	ON	—	—	RUNDIV<4:0>					—	—	—	—	—	—	—	WDTWINEN	xx00

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **12.0 "I/O Ports"** for more information.

18.0 OUTPUT COMPARE

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. "Output Compare"** (DS60001111) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

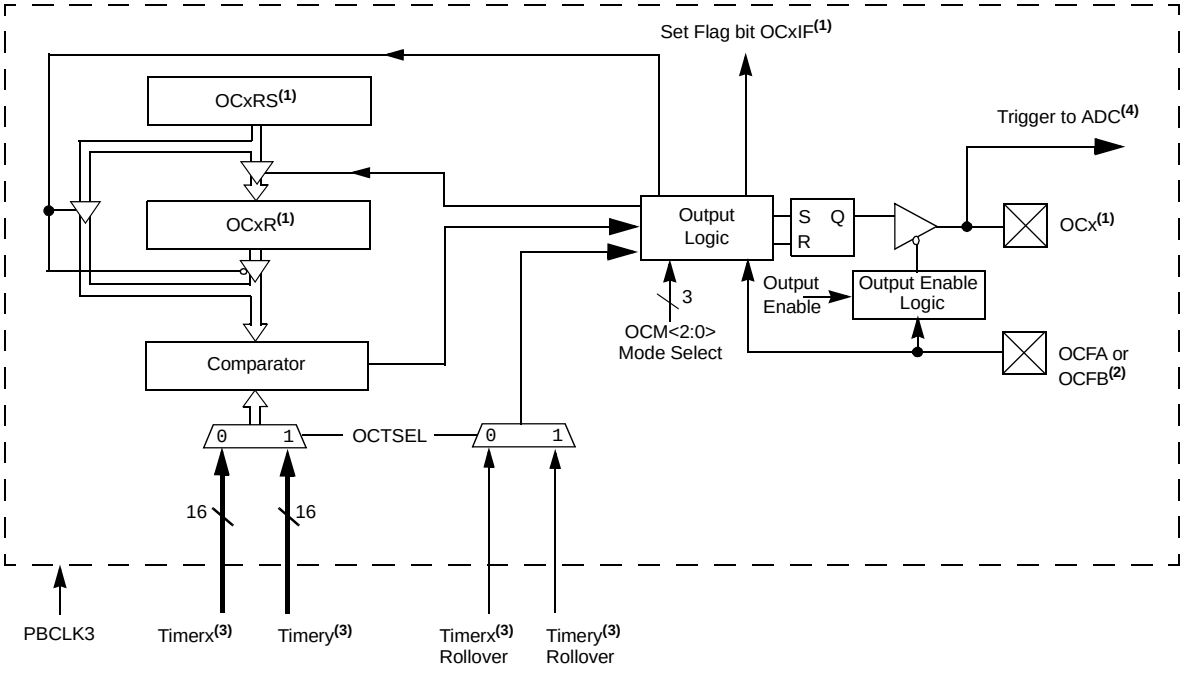
The Output Compare module is used to generate a single pulse or a train of pulses in response to selected time base events.

For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are key features of the Output Compare module:

- Multiple Output Compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Programmable selection of 16-bit or 32-bit time bases
- Can operate from either of two available 16-bit time bases or a single 32-bit time base
- ADC event trigger

FIGURE 18-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



Note 1: Where 'x' is shown, reference is made to the registers associated with the respective output compare channels, 1 through 9.

2: The OCFA pin controls the OC1, OC3, and OC7-OC9 channels. The OCFB pin controls the OC4-OC6 channels.

3: Refer to Table 18-1 for Timerx and Timery selections.

4: The ADC event trigger is only available on OC1, OC3, and OC 5.

20.0 SERIAL QUAD INTERFACE (SQI)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 46. "Serial Quad Interface (SQI)"** (DS60001244) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

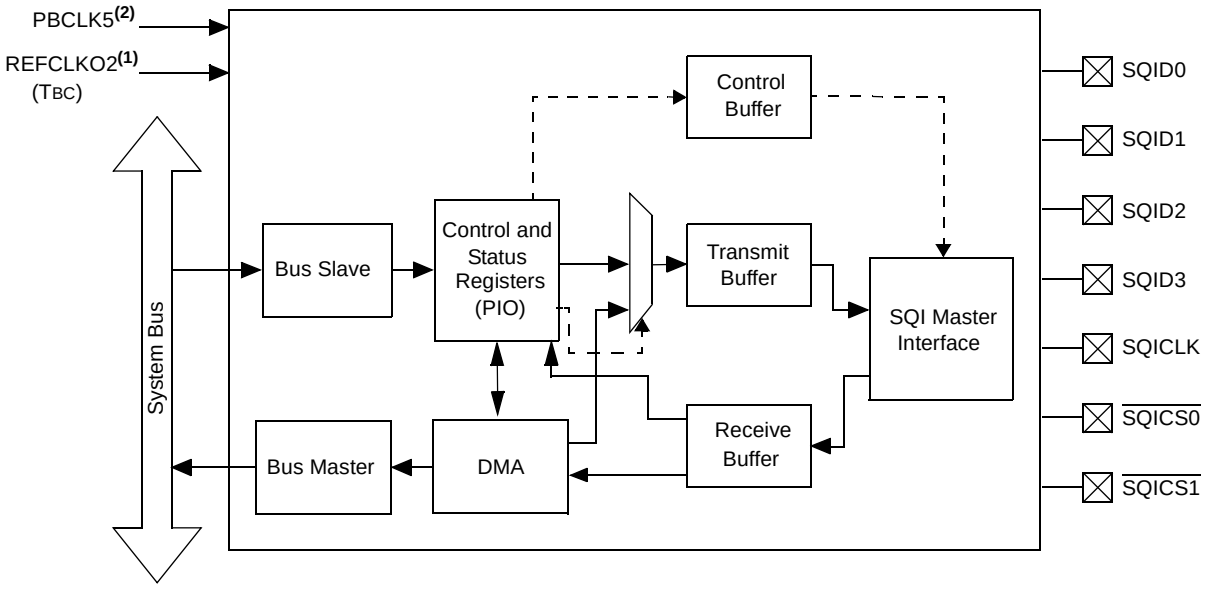
The SQI module is a synchronous serial interface that provides access to serial Flash memories and other serial devices. The SQI module supports Single Lane (identical to SPI), Dual Lane, and Quad Lane modes.

The following are key feature of the SQI module:

- Supports Single, Dual, and Quad Lane modes
- Supports Single Data Rate (SDR) mode
- Programmable command sequence
- eXecute-In-Place (XIP)
- Data transfer:
  - Programmed I/O mode (PIO)
  - Buffer descriptor DMA
- Supports SPI Mode 0 and Mode 3
- Programmable Clock Polarity (CPOL) and Clock Phase (CPHA) bits
- Supports up to two Chip Selects
- Supports up to four bytes of Flash address
- Programmable interrupt thresholds
- 32-byte transmit data buffer
- 32-byte receive data buffer
- 4-word controller buffer

Note: Once the SQI module is configured, external devices are memory mapped into KSEG2 and KSEG3 (see Figure 4-1 through Figure 4-4 in **Section 4.0 "Memory Organization"** for more information). The MMU must be enabled and the TLB must be set up to access this memory (refer to **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) of the *"PIC32 Family Reference Manual"* for more information).

FIGURE 20-1: SQI MODULE BLOCK DIAGRAM



Note 1: When configuring the REFCLKO2 clock source, a value of '0' for the ROTRIM<8:0> bits must be selected.
2: This clock source is only used for SQI Special Function Register (SFR) access.

21.1 I²C Control Registers

TABLE 21-1: I2C1 THROUGH I2C5 REGISTER MAP

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	I2C1CON	31:16	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
0010	I2C1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
0020	I2C1ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	Address Register										0000
0030	I2C1MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	Address Mask Register										0000
0040	I2C1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Register																0000
0050	I2C1TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Transmit Register								0000
0060	I2C1RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Receive Register								0000
0200	I2C2CON(2)	31:16	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
0210	I2C2STAT(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
0220	I2C2ADD(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	Address Register										0000
0230	I2C2MSK(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	Address Mask Register										0000
0240	I2C2BRG(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Register																0000
0250	I2C2TRN(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Transmit Register								0000
0260	I2C2RCV(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	Receive Register								0000
0400	I2C3CON	31:16	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
0410	I2C3STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
0420	I2C3ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	Address Register										0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

2: This register is not available on 64-pin devices.

REGISTER 26-3: CEBDADDR: CRYPTO ENGINE BUFFER DESCRIPTOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BDPADDR<31:0>:** Current Buffer Descriptor Process Address Status bits

These bits contain the current descriptor address that is being processed by the Buffer Descriptor Processor (BDP).

REGISTER 26-4: CEBDPADDR: CRYPTO ENGINE BUFFER DESCRIPTOR PROCESSOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BASEADDR<31:0>:** Buffer Descriptor Base Address bits

These bits contain the physical address of the first Buffer Descriptor in the Buffer Descriptor chain. When enabled, the Crypto DMA begins fetching Buffer Descriptors from this address.

TABLE 26-4: CRYPTO ENGINE SECURITY ASSOCIATION STRUCTURE (CONTINUED)

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SA_ENCIV1	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV2	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV3	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV4	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							

REGISTER 27-5: RNGSEEDx: TRUE RANDOM NUMBER GENERATOR SEED REGISTER 'x' ('x' = 1 OR 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **SEED<31:0>:** TRNG MSb/LSb Value bits (RNGSEED1 = LSb, RNGSEED2 = MSb)

REGISTER 27-6: RNGCNT: TRUE RANDOM NUMBER GENERATOR COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RCNT<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-7 **Unimplemented:** Read as '0'

bit 6-0 **RCNT<6:0>:** Number of Valid TRNG MSB 32 bits

TABLE 28-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B04C	ADCCMP3	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B050	ADCCMPEN4	31:16	CMPE31(1)	CMPE30(1)	CMPE29(1)	CMPE28(1)	CMPE27(1)	CMPE26(1)	CMPE25(1)	CMPE24(1)	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19(1)	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B054	ADCCMP4	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B058	ADCCMPEN5	31:16	CMPE31(1)	CMPE30(1)	CMPE29(1)	CMPE28(1)	CMPE27(1)	CMPE26(1)	CMPE25(1)	CMPE24(1)	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19(1)	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B05C	ADCCMP5	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B060	ADCCMPEN6	31:16	CMPE31(1)	CMPE30(1)	CMPE29(1)	CMPE28(1)	CMPE27(1)	CMPE26(1)	CMPE25(1)	CMPE24(1)	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19(1)	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B064	ADCCMP6	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B068	ADCFLTR1	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B06C	ADCFLTR2	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B070	ADCFLTR3	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B074	ADCFLTR4	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B078	ADCFLTR5	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B07C	ADCFLTR6	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B080	ADCTRG1	31:16	—	—	—	TRGSRC3<4:0>					—	—	—	TRGSRC2<4:0>					0000
		15:0	—	—	—	TRGSRC1<4:0>					—	—	—	TRGSRC0<4:0>					0000
B084	ADCTRG2	31:16	—	—	—	TRGSRC7<4:0>					—	—	—	TRGSRC6<4:0>					0000
		15:0	—	—	—	TRGSRC5<4:0>					—	—	—	TRGSRC4<4:0>					0000
B088	ADCTRG3	31:16	—	—	—	TRGSRC11<4:0>					—	—	—	TRGSRC10<4:0>					0000
		15:0	—	—	—	TRGSRC9<4:0>					—	—	—	TRGSRC8<4:0>					0000
B0A0	ADCCMPCON1	31:16	CVDDATA<15:0>																0000
		15:0	—	—	AINID<5:0>						ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0A4	ADCCMPCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0A8	ADCCMPCON3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000

Note 1: This bit or register is not available on 64-pin devices.
2: This bit or register is not available on 64-pin and 100-pin devices.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

TABLE 28-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B0AC	ADCCMPCON4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0B0	ADCCMPCON5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0B4	ADCCMPCON6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0B8	ADCFSTAT	31:16	FEN	—	—	ADC4EN	ADC3EN	ADC2EN	ADC1EN	ADC0EN	FIEN	FRDY	FWROVERR	—	—	—	—	—	0000
		15:0	FCNT<7:0>								FSIGN	—	—	—	—	ADCID<2:0>			0000
B0BC	ADCFIFO	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B0C0	ADCBASE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADCBASE<15:0>																0000
B0D0	ADCTRGSNS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LVL11	LVL10	LVL9	LVL8	LVL7	LVL6	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0	0000
B0D4	ADC0TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		—	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
B0D8	ADC1TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		—	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
B0DC	ADC2TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		—	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
B0E0	ADC3TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		—	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
B0E4	ADC4TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		—	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
B0F0	ADCEIEN1	31:16	EIEN31(1)	EIEN30(1)	EIEN29(1)	EIEN28(1)	EIEN27(1)	EIEN26(1)	EIEN25(1)	EIEN24(1)	EIEN23(1)	EIEN22(1)	EIEN21(1)	EIEN20(1)	EIEN19(1)	EIEN18	EIEN17	EIEN16	0000
		15:0	EIEN15	EIEN14	EIEN13	EIEN12	EIEN11	EIEN10	EIEN9	EIEN8	EIEN7	EIEN6	EIEN5	EIEN4	EIEN3	EIEN2	EIEN1	EIEN0	0000
B0F4	ADCEIEN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	EIEN44	EIEN43	EIEN42(2)	EIEN41(2)	EIEN40(2)	EIEN39(2)	EIEN38(2)	EIEN37(2)	EIEN36(2)	EIEN35(2)	EIEN34(1)	EIEN33(1)	EIEN32(1)	0000
B0F8	ADCEISTAT1	31:16	EIRDY31(1)	EIRDY30(1)	EIRDY29(1)	EIRDY28(1)	EIRDY27(1)	EIRDY26(1)	EIRDY25(1)	EIRDY24(1)	EIRDY23(1)	EIRDY22(1)	EIRDY21(1)	EIRDY20(1)	EIRDY19(1)	EIRDY18	EIRDY17	EIRDY16	0000
		15:0	EIRDY15	EIRDY14	EIRDY13	EIRDY12	EIRDY11	EIRDY10	EIRDY9	EIRDY8	EIRDY7	EIRDY6	EIRDY5	EIRDY4	EIRDY3	EIRDY2	EIRDY1	EIRDY0	0000
B0FC	ADCEISTAT2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	EIRDY44	EIRDY43	EIRDY42(2)	EIRDY41(2)	EIRDY40(2)	EIRDY39(2)	EIRDY38(2)	EIRDY37(2)	EIRDY36(2)	EIRDY35(2)	EIRDY34(1)	EIRDY33(1)	EIRDY32(1)	0000
B100	ADCANCON	31:16	—	—	—	—	WKUPCLKCNT<3:0>				WKIEN7	—	—	WKIEN4	WKIEN3	WKIEN2	WKIEN1	WKIEN0	0000
		15:0	WKRDY7	—	—	WKRDY4	WKRDY3	WKRDY2	WKRDY1	WKRDY0	ANEN7	—	—	ANEN4	ANEN3	ANEN2	ANEN1	ANEN0	0000
B180	ADC0CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
B184	ADC1CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000

Note **1:** This bit or register is not available on 64-pin devices.
2: This bit or register is not available on 64-pin and 100-pin devices.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

REGISTER 29-15: CiFLTCON5: CAN FILTER CONTROL REGISTER 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN23	MSEL23<1:0>		FSEL23<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN22	MSEL22<1:0>		FSEL22<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN21	MSEL21<1:0>		FSEL21<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN20	MSEL20<1:0>		FSEL20<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN23:** Filter 23 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL23<1:0>:** Filter 23 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL23<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN22:** Filter 22 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL22<1:0>:** Filter 22 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL22<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-20: ETHFRMRXOK: ETHERNET CONTROLLER FRAMES RECEIVED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FRMRXOKCNT<15:0>:** Frames Received OK Count bits

Increment count for frames received successfully by the RX Filter. This count will not be incremented if there is a Frame Check Sequence (FCS) or Alignment error.

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

NOTES:

TABLE 37-38: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.1	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module VSS Supply	VSS	—	VSS + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	VREFL + 1.8	—	AVDD	V	**(Note 1)**
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 1.8	V	**(Note 1)**
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	1.8	—	AVDD	V	**(Note 2)**
AD08	IREF	Current Drain	—	102	—	µA	Per ADCx ('x' = 0-4, 7)
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS	—	VREFL	V	—
AD14	VINH	Absolute VINH Input Voltage	AVSS	—	VREFH	V	—
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	6	—	12	bits	Selectable 6, 8, 10, 12 Resolution Ranges
AD21c	INL	Integral Nonlinearity	—	±3	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Nonlinearity	—	±1	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD23c	GERR	Gain Error	—	±8	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24c	EOFF	Offset Error	—	±2	—	LSb	VINL = AVSS = 0V, AVDD = 3.3V
Dynamic Performance							
AD31b	SINAD	Signal to Noise and Distortion	—	67	—	dB	Single-ended **(Notes 2,3)**
AD34b	ENOB	Effective Number of bits	—	10.5	—	bits	**(Notes 2,3)**

Note 1: These parameters are not characterized or tested in manufacturing.

2: These parameters are characterized, but not tested in manufacturing.

3: Characterized with a 1 kHz sine wave.

4: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

A.7 Interrupts and Exceptions

The key difference between Interrupt Controllers in PIC32MX5XX/6XX/7XX devices and PIC32MZ EF devices concerns vector spacing. Previous PIC32MX devices had fixed vector spacing, which is adjustable in set increments, and every interrupt had the same amount of space. PIC32MZ EF devices replace this with a variable offset spacing, where each interrupt has an offset register to determine where to begin execution.

In addition, the IFSx, IECx, and IPCx registers for old peripherals have shifted to different registers due to new peripherals. Please refer to **7.0 "CPU Exceptions and Interrupt Controller"** to determine where the interrupts are now located.

Table A-8 lists differences (indicated by **Bold** type) in the registers that will affect software migration.

TABLE A-8: INTERRUPT DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Vector Spacing	
On PIC32MX devices, the vector spacing was determined by the VS field in the CPU core. **VS<4:0> (IntCtl<9:5>: CP0 Register 12, Select 1)** **10000 = 512-byte vector spacing** **01000 = 256-byte vector spacing** **00100 = 128-byte vector spacing** **00010 = 64-byte vector spacing** **00001 = 32-byte vector spacing** **00000 = 0-byte vector spacing**	On PIC32MZ EF devices, the vector spacing is variable and determined by the Interrupt controller. The VOFFx<17:1> bits in the OFFx register are set to the offset from EBASE where the interrupt service routine is located. **VOFFx<17:1> (OFFx<17:1>)** **Interrupt Vector 'x' Address Offset bits**
Shadow Register Sets	
On PIC32MX devices, there was one shadow register set which could be used during interrupt processing. Which interrupt priority could use the shadow register set was determined by the FSRSSEL field in DEVCFG3 and SS0 on INTCON. **FSRSSEL<2:0> (DEVCFG3<18:16>)** **111 = Assign Interrupt Priority 7 to a shadow register set** **110 = Assign Interrupt Priority 6 to a shadow register set** • • • **001 = Assign Interrupt Priority 1 to a shadow register set** **000 = All interrupt priorities are assigned to a shadow register set** SS0 (**INTCON<16>**) 1 = Single vector is presented with a shadow register set 0 = Single vector is not presented with a shadow register set	On PIC32MZ EF devices, there are seven shadow register sets, and each priority level can be assigned a shadow register set to use via the PRIxSS<3:0> bits in the PRISS register. The SS0 bit is also moved to PRISS<0>. **PRIxSS<3:0> PRISS<y:z>** **1xxx = Reserved (by default, an interrupt with a priority level of x uses Shadow Set 0)** **0111 = Interrupt with a priority level of x uses Shadow Set 7** **0110 = Interrupt with a priority level of x uses Shadow Set 6** • • • **0001 = Interrupt with a priority level of x uses Shadow Set 1** **0000 = Interrupt with a priority level of x uses Shadow Set 0** SS0 (**PRISS<0>**) 1 = Single vector is presented with a shadow register set 0 = Single vector is not presented with a shadow register set
Status	
PIC32MX devices, the VEC<5:0> bits show which interrupt is being serviced. **VEC<5:0> (INTSTAT<5:0>)** 11111-00000 = The interrupt vector that is presented to the CPU	On PIC32MZ EF devices, the SIRQ<7:0> bits show the IRQ number of the interrupt last serviced. **SIRQ<7:0> (INTSTAT<7:0>)** 11111111-00000000 = The last interrupt request number serviced by the CPU