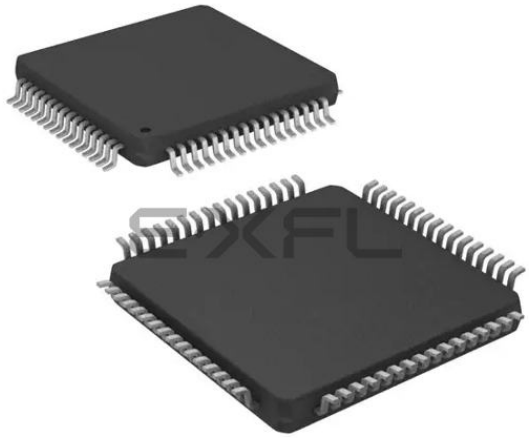

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Number of I/O	46
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
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Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
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Supplier Device Package	64-TQFP (10x10)
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TABLE 1-8: UART1 THROUGH UART6 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Universal Asynchronous Receiver Transmitter 1							
U1RX	PPS	PPS	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	PPS	PPS	O	—	UART1 Transmit
U1CTS	PPS	PPS	PPS	PPS	I	ST	UART1 Clear to Send
U1RTS	PPS	PPS	PPS	PPS	O	—	UART1 Ready to Send
Universal Asynchronous Receiver Transmitter 2							
U2RX	PPS	PPS	PPS	PPS	I	ST	UART2 Receive
U2TX	PPS	PPS	PPS	PPS	O	—	UART2 Transmit
U2CTS	PPS	PPS	PPS	PPS	I	ST	UART2 Clear To Send
U2RTS	PPS	PPS	PPS	PPS	O	—	UART2 Ready To Send
Universal Asynchronous Receiver Transmitter 3							
U3RX	PPS	PPS	PPS	PPS	I	ST	UART3 Receive
U3TX	PPS	PPS	PPS	PPS	O	—	UART3 Transmit
U3CTS	PPS	PPS	PPS	PPS	I	ST	UART3 Clear to Send
U3RTS	PPS	PPS	PPS	PPS	O	—	UART3 Ready to Send
Universal Asynchronous Receiver Transmitter 4							
U4RX	PPS	PPS	PPS	PPS	I	ST	UART4 Receive
U4TX	PPS	PPS	PPS	PPS	O	—	UART4 Transmit
U4CTS	PPS	PPS	PPS	PPS	I	ST	UART4 Clear to Send
U4RTS	PPS	PPS	PPS	PPS	O	—	UART4 Ready to Send
Universal Asynchronous Receiver Transmitter 5							
U5RX	PPS	PPS	PPS	PPS	I	ST	UART5 Receive
U5TX	PPS	PPS	PPS	PPS	O	—	UART5 Transmit
U5CTS	PPS	PPS	PPS	PPS	I	ST	UART5 Clear to Send
U5RTS	PPS	PPS	PPS	PPS	O	—	UART5 Ready to Send
Universal Asynchronous Receiver Transmitter 6							
U6RX	PPS	PPS	PPS	PPS	I	ST	UART6 Receive
U6TX	PPS	PPS	PPS	PPS	O	—	UART6 Transmit
U6CTS	PPS	PPS	PPS	PPS	I	ST	UART6 Clear to Send
U6RTS	PPS	PPS	PPS	PPS	O	—	UART6 Ready to Send

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

REGISTER 3-10: FCSR: FLOATING POINT CONTROL AND STATUS REGISTER; CP1 REGISTER 31

bit 16	**V:** Invalid Operation bit
bit 15	**Z:** Divide-by-Zero bit
bit 14	**O:** Overflow bit
bit 13	**U:** Underflow bit
bit 12	**I:** Inexact bit
bit 11-7	**ENABLES<4:0>:** FPU Exception Enable bits These bits control whether or not a trap is taken when an IEEE exception condition occurs for any of the five conditions. The trap occurs when both an enable bit and its corresponding cause bit are set either during an FPU arithmetic operation or by moving a value to the FCSR or one of its alternative representations.
bit 11	**V:** Invalid Operation bit
bit 10	**Z:** Divide-by-Zero bit
bit 9	**O:** Overflow bit
bit 8	**U:** Underflow bit
bit 7	**I:** Inexact bit
bit 6-2	**FLAGS<4:0>:** FPU Flags bits These bits show any exception conditions that have occurred for completed instructions since the flag was last reset by software.
bit 6	**V:** Invalid Operation bit
bit 5	**Z:** Divide-by-Zero bit
bit 4	**O:** Overflow bit
bit 3	**U:** Underflow bit
bit 2	**I:** Inexact bit
bit 1-0	**RM<1:0>:** Rounding Mode control bits 11 = Round towards Minus Infinity ($-\infty$) 10 = Round towards Plus Infinity ($+\infty$) 01 = Round toward Zero (0) 00 = Round to Nearest

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source.For detailed information, refer to **Section 48. "Memory Organization and Permissions"** in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MZ EF microcontrollers provide 4 GB of unified virtual memory address space. All memory regions, including program, data memory, SFRs and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, PIC32MZ EF devices allow execution from data memory.

Key features include:

- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/ KSEG1/KSEG2/KSEG3) mode address space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Cacheable (KSEG0/KSEG2) and non-cacheable (KSEG1/KSEG3) address regions
- Read/write permission access to predefined memory regions

4.1 Memory Layout

PIC32MZ EF microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The main memory maps for the PIC32MZ EF devices are illustrated in Figure 4-1 through Figure 4-4. Figure 4-5 provides memory map information for boot Flash and boot alias. Table 4-1 provides memory map information for Special Function Registers (SFRs).

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1170	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
11A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
11B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
11C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
11D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
11E0	DCH2CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
11F0	DCH2ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1200	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1210	DCH2SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
1220	DCH2DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
1230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1260	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1270	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 11-14: USBFIFOA: USB FIFO ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RXFIFOAD<12:8>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXFIFOAD<7:0>							
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TXFIFOAD<12:8>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXFIFOAD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-16 **RXFIFOAD<12:0>:** Receive Endpoint FIFO Address bits

Start address of the endpoint FIFO in units of 8 bytes as follows:

1111111111111 = 0xFFF8
•
•
•
0000000000010 = 0x0010
0000000000001 = 0x0008
0000000000000 = 0x0000

bit 15-13 **Unimplemented:** Read as '0'

bit 12-0 **TXFIFOAD<12:0>:** Transmit Endpoint FIFO Address bits

Start address of the endpoint FIFO in units of 8 bytes as follows:

1111111111111 = 0xFFF8
•
•
•
0000000000010 = 0x0010
0000000000001 = 0x0008
0000000000000 = 0x0000

TABLE 12-2: INPUT PIN SELECTION

Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT3	INT3R	INT3R<3:0>	0000 = RPD2 0001 = RPG8 0010 = RPF4 0011 = RPD10 0100 = RPF1 0101 = RPB9 0110 = RPB10 0111 = RPC14 1000 = RPB5 1001 = Reserved 1010 = RPC1(1) 1011 = RPD14(1) 1100 = RPG1(1) 1101 = RPA14(1) 1110 = RPD6(2) 1111 = Reserved
T2CK	T2CKR	T2CKR<3:0>	
T6CK	T6CKR	T6CKR<3:0>	
IC3	IC3R	IC3R<3:0>	
IC7	IC7R	IC7R<3:0>	
U1RX	U1RXR	U1RXR<3:0>	
$\overline{\text{U2CTS}}$	U2CTSR	U2CTSR<3:0>	
U5RX	U5RXR	U5RXR<3:0>	
$\overline{\text{U6CTS}}$	U6CTSR	U6CTSR<3:0>	
SDI1	SDI1R	SDI1R<3:0>	
SDI3	SDI3R	SDI3R<3:0>	
SDI5(1)	SDI5R(1)	SDI5R<3:0>(1)	
SS6(1)	SS6R(1)	SS6R<3:0>(1)	
REFCLKI1	REFCLKI1R	REFCLKI1R<3:0>	
INT4	INT4R	INT4R<3:0>	0000 = RPD3 0001 = RPG7 0010 = RPF5 0011 = RPD11 0100 = RPF0 0101 = RPB1 0110 = RPE5 0111 = RPC13 1000 = RPB3 1001 = Reserved 1010 = RPC4(1) 1011 = RPD15(1) 1100 = RPG0(1) 1101 = RPA15(1) 1110 = RPD7(2) 1111 = Reserved
T5CK	T5CKR	T5CKR<3:0>	
T7CK	T7CKR	T7CKR<3:0>	
IC4	IC4R	IC4R<3:0>	
IC8	IC8R	IC8R<3:0>	
U3RX	U3RXR	U3RXR<3:0>	
$\overline{\text{U4CTS}}$	U4CTSR	U4CTSR<3:0>	
SDI2	SDI2R	SDI2R<3:0>	
SDI4	SDI4R	SDI4R<3:0>	
C1RX(3)	C1RXR(3)	C1RXR<3:0>(3)	
REFCLKI4	REFCLKI4R	REFCLKI4R<3:0>	
INT2	INT2R	INT2R<3:0>	0000 = RPD9 0001 = RPG6 0010 = RPB8 0011 = RPB15 0100 = RPD4 0101 = RPB0 0110 = RPE3 0111 = RPB7 1000 = Reserved 1001 = RPF12(1) 1010 = RPD12(1) 1011 = RPF8(1) 1100 = RPC3(1) 1101 = RPE9(1) 1110 = Reserved 1111 = Reserved
T3CK	T3CKR	T3CKR<3:0>	
T8CK	T8CKR	T8CKR<3:0>	
IC2	IC2R	IC2R<3:0>	
IC5	IC5R	IC5R<3:0>	
IC9	IC9R	IC9R<3:0>	
$\overline{\text{U1CTS}}$	U1CTSR	U1CTSR<3:0>	
U2RX	U2RXR	U2RXR<3:0>	
$\overline{\text{U5CTS}}$	U5CTSR	U5CTSR<3:0>	
$\overline{\text{SS1}}$	SS1R	SS1R<3:0>	
$\overline{\text{SS3}}$	SS3R	SS3R<3:0>	
$\overline{\text{SS4}}$	SS4R	SS4R<3:0>	
$\overline{\text{SS5}}$(1)	SS5R(1)	SS5R<3:0>(1)	
C2RX(3)	C2RXR(3)	C2RXR<3:0>(3)	

Note 1: This selection is not available on 64-pin devices.

2: This selection is not available on 64-pin or 100-pin devices.

3: This selection is not available on devices without a CAN module.

TABLE 12-22: PERIPHERAL PIN SELECT INPUT REGISTER MAP

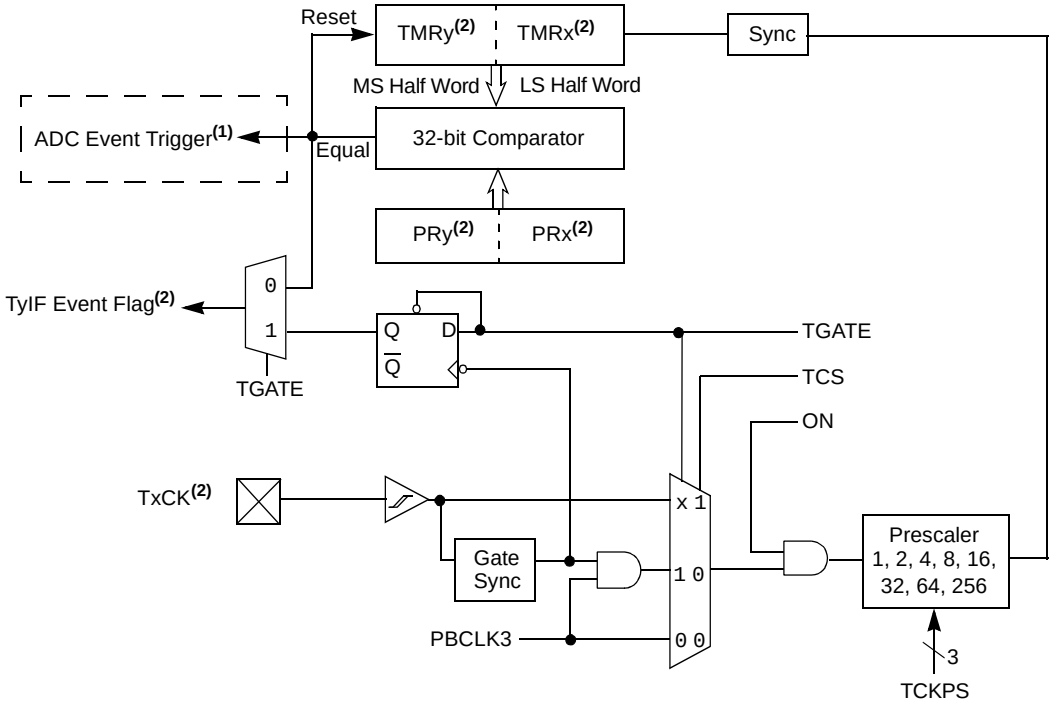
Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1404	INT1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT1R<3:0>				0000
1408	INT2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT2R<3:0>				0000
140C	INT3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT3R<3:0>				0000
1410	INT4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT4R<3:0>				0000
1418	T2CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T2CKR<3:0>				0000
141C	T3CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T3CKR<3:0>				0000
1420	T4CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T4CKR<3:0>				0000
1424	T5CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T5CKR<3:0>				0000
1428	T6CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T6CKR<3:0>				0000
142C	T7CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T7CKR<3:0>				0000
1430	T8CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T8CKR<3:0>				0000
1434	T9CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T9CKR<3:0>				0000
1438	IC1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC1R<3:0>				0000
143C	IC2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC2R<3:0>				0000
1440	IC3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC3R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

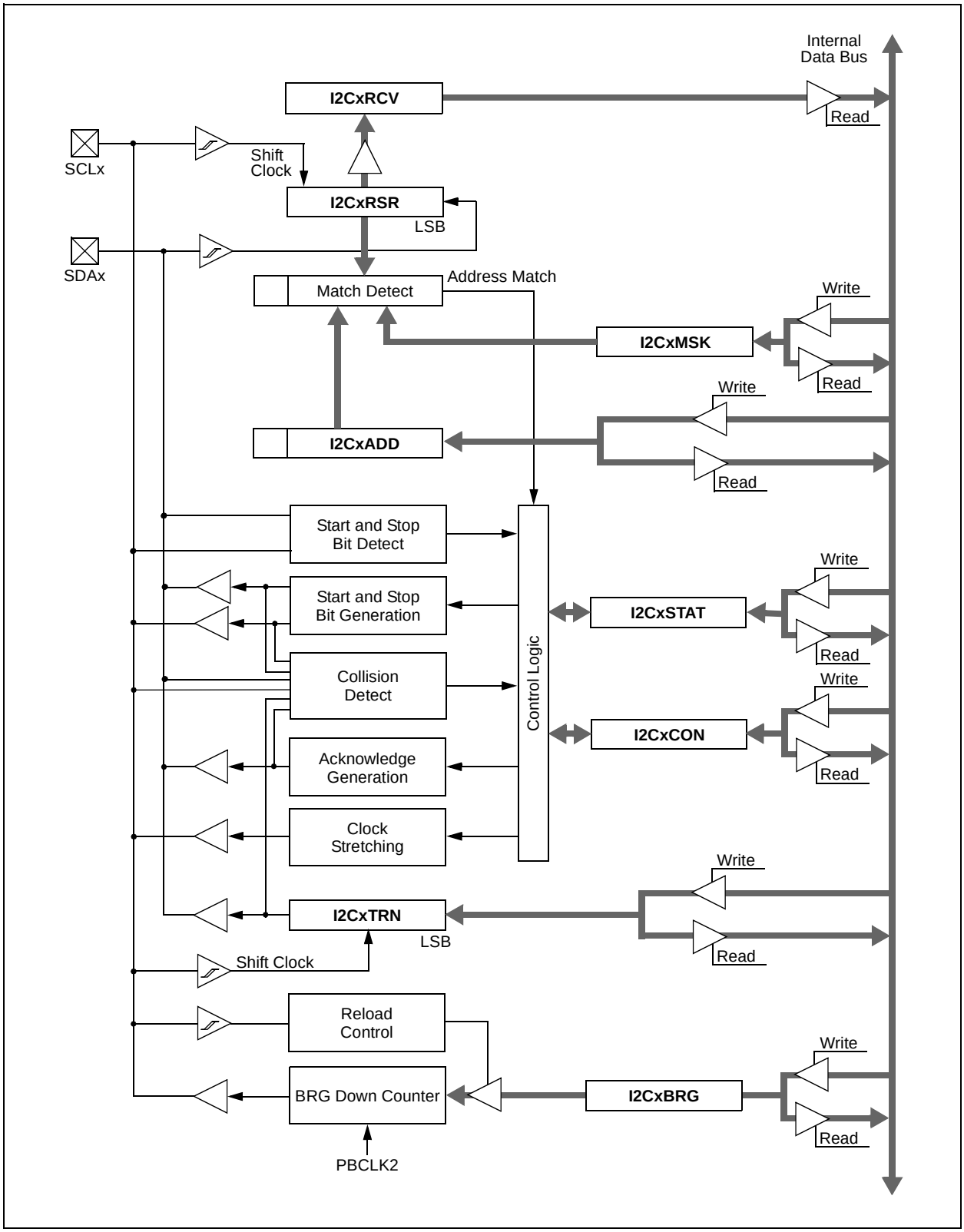
2: This register is not available on devices without a CAN module.

FIGURE 14-2: TIMER2/3, TIMER4/5, TIMER6/7, AND TIMER8/9 BLOCK DIAGRAM (32-BIT)



Note 1: ADC event trigger is available only on the Timer2/3 and TImer4/5 pairs.
2: In this diagram, 'x' represents Timer2, 4, 6, or 8, and 'y' represents Timer3, 5, 7, or 9.

FIGURE 21-1: I²C BLOCK DIAGRAM



REGISTER 21-2: I2CxSTAT: I^{2}C STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0, HS, HC	R-0, HS, HC	R/C-0, HS, HC	U-0	U-0	R/C-0, HS	R-0, HS, HC	R-0, HS, HC
	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10
7:0	R/C-0, HS, SC	R/C-0, HS, SC	R-0, HS, HC	R/C-0, HS, HC	R/C-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF

Legend:	HS = Hardware Set	HC = Hardware Cleared	SC = Software Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	C = Clearable bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I^{2}C master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware set or clear at end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I^{2}C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

bit 13 **ACKTIM:** Acknowledge Time Status bit (Valid in I^{2}C Slave mode only)
1 = I^{2}C bus is in an Acknowledge sequence, set on the eight falling edge of SCL clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCL clock

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware set at detection of bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 **ADD10:** 10-bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I^{2}C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

REGISTER 28-6: ADCIMCON2: ADC INPUT MODE CONTROL REGISTER 2 (CONTINUED)

bit 6 **SIGN19:** AN19 Signed Data Mode bit(1)
1 = AN19 is using Signed Data mode
0 = AN19 is using Unsigned Data mode

bit 5 **DIFF18:** AN18 Mode bit
1 = AN18 is using Differential mode
0 = AN18 is using Single-ended mode

bit 4 **SIGN18:** AN18 Signed Data Mode bit
1 = AN18 is using Signed Data mode
0 = AN18 is using Unsigned Data mode

bit 3 **DIFF17:** AN17 Mode bit
1 = AN17 is using Differential mode
0 = AN17 is using Single-ended mode

bit 2 **SIGN17:** AN17 Signed Data Mode bit
1 = AN17 is using Signed Data mode
0 = AN17 is using Unsigned Data mode

bit 1 **DIFF16:** AN16 Mode bit
1 = AN16 is using Differential mode
0 = AN16 is using Single-ended mode

bit 0 **SIGN16:** AN16 Signed Data Mode bit
1 = AN16 is using Signed Data mode
0 = AN16 is using Unsigned Data mode

Note 1: This bit is not available on 64-pin devices.

REGISTER 28-20: ADCCMPCON1: ADC DIGITAL COMPARATOR 1 CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	CVDDATA<15:8>							
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	CVDDATA<7:0>							
15:8	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	AINID<5:0>					
7:0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **CVDDATA<15:0>:** CVD Data Status bits

In CVD mode, these bits obtain the CVD differential output data (subtraction of CVD positive and negative measurement), whenever a Digital Comparator interrupt is generated. The value in these bits is compliant with the FRACT bit (ADCCON1<23>) and is always signed.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **AINID<5:0>:** Digital Comparator 0 Analog Input Identification (ID) bits

When a digital comparator event occurs (DCMPED = 1), these bits identify the analog input being monitored by Digital Comparator 0.

Note: In normal ADC mode, only analog inputs <31:0> can be processed by the Digital Comparator 0. The Digital Comparator 0 also supports the CVD mode, in which all Class 2 and Class 3 analog inputs may be stored in the AINID<5:0> bits.

111111 = Reserved
•
•
•
101101 = Reserved
101100 = AN44 is being monitored
101011 = AN43 is being monitored
•
•
•
000001 = AN1 is being monitored
000000 = AN0 is being monitored

bit 7 **ENDCMP:** Digital Comparator 0 Enable bit

1 = Digital Comparator 0 is enabled

0 = Digital Comparator 0 is not enabled, and the DCMPED status bit (ADCCMP0CON<5>) is cleared

bit 6 **DCMPGIEN:** Digital Comparator 0 Global Interrupt Enable bit

1 = A Digital Comparator 0 interrupt is generated when the DCMPED status bit (ADCCMP0CON<5>) is set

0 = A Digital Comparator 0 interrupt is disabled

bit 5 **DCMPED:** Digital Comparator 0 "Output True" Event Status bit

The logical conditions under which the digital comparator gets "True" are defined by the IEBTWN, IEHIHI, IEHILO, IELOHI, and IELOLO bits.

Note: This bit is cleared by reading the AINID<5:0> bits or by disabling the Digital Comparator module (by setting ENDCMP to '0').

1 = Digital Comparator 0 output true event has occurred (output of Comparator is '1')

0 = Digital Comparator 0 output is false (output of comparator is '0')

bit 4 **IEBTWN:** Between Low/High Digital Comparator 0 Event bit

1 = Generate a digital comparator event when DCMPLO<15:0> ≤ DATA<31:0> < DCMPHI<15:0>

0 = Do not generate a digital comparator event

REGISTER 29-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	WAKFIL	—	—	—	SEG2PH<2:0>(1,4)		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SEG2PHTS(1)	SAM(2)	SEG1PH<2:0>			PRSEG<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SJW<1:0>(3)		BRP<5:0>					

Legend:	HC = Hardware Clear	S = Settable bit	
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-23 **Unimplemented:** Read as ‘0’

bit 22 **WAKFIL:** CAN Bus Line Filter Enable bit
1 = Use CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 21-19 **Unimplemented:** Read as ‘0’

bit 18-16 **SEG2PH<2:0>:** Phase Buffer Segment 2 bits(1,4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 15 **SEG2PHTS:** Phase Segment 2 Time Select bit(1)
1 = Freely programmable
0 = Maximum of SEG1PH or Information Processing Time, whichever is greater

bit 14 **SAM:** Sample of the CAN Bus Line bit(2)
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 13-11 **SEG1PH<2:0>:** Phase Buffer Segment 1 bits(4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
2: 3 Time bit sampling is not allowed for BRP < 2.
3: SJW ≤ SEG2PH.
4: The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

TABLE 30-5: ETHERNET CONTROLLER REGISTER SUMMARY (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
22B0	EMAC1 MWTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MWTD<15:0>																0000
22C0	EMAC1 MRDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MRDD<15:0>																0000
22D0	EMAC1 MIND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	LINKFAIL	NOTVALID	SCAN	MIIMBUSY	0000
2300	EMAC1 SA0(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	STNADDR6<7:0>								STNADDR5<7:0>								xxxx
2310	EMAC1 SA1(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	STNADDR4<7:0>								STNADDR3<7:0>								xxxx
2320	EMAC1 SA2(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	STNADDR2<7:0>								STNADDR1<7:0>								xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

2: Reset values default to the factory programmed value.

34.2 Registers

TABLE 34-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FFC0	DEVCFG3	31:16	—	FUSBIDIO	IOL1WAY	PMDL1WAY	PGL1WAY	—	FETHIO	FMIIEN	—	—	—	—	—	—	—	—	xxxx
		15:0	USERID<15:0>																xxxx
FFC4	DEVCFG2	31:16	—	UPLLFSEL	—	—	—	—	—	—	—	—	—	—	—	FPLLODIV<2:0>			xxxx
		15:0	—	FPLLMULT<6:0>							FPLLICLK	FPLLRNG<2:0>			—	FPLLIDIV<2:0>			xxxx
FFC8	DEVCFG1	31:16	FDMTEN	DMTCNT<4:0>					FWDTWINSZ<1:0>		FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>					xxxx
		15:0	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMOD<1:0>		IESO	FSOSCEN	DMTINTV<2:0>			FNOSC<2:0>			xxxx
FFCC	DEVCFG0	31:16	—	EJTAGBEN	—	—	—	—	—	—	—	—	POSCBOOST	POSCGAIN<1:0>		SOSCBOOST	SOSCGAIN<1:0>		xxxx
		15:0	SMCLR	DBGPER<2:0>			—	FSLEEP	FECCCON<1:0>		—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN	DEBUG<1:0>		xxxx
FFD0	DEVCP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFD4	DEVCP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFD8	DEVCP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFDC	DEVCP0	31:16	—	—	—	CP	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE0	DEVSIGN3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE4	DEVSIGN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE8	DEVSIGN1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFEC	DEVSIGN0	31:16	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

37.1 DC Characteristics

TABLE 37-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts) (Note 1)	Temp. Range (in °C)	Max. Frequency	Comment
			PIC32MZ EF Devices	
DC5	2.1V-3.6V	-40°C to +85°C	200 MHz	—

Note 1: Overall functional device operation at $V_{BORMIN} < V_{DD} < V_{DDMIN}$ is guaranteed, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below V_{DDMIN}. Refer to parameter BO10 in Table 37-5 for BOR values.

TABLE 37-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typical	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	T_J	-40	—	+125	°C
Operating Ambient Temperature Range	T_A	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	T_J	-40	—	+140	°C
Operating Ambient Temperature Range	T_A	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - S\ I_{OH})$ I/O Pin Power Dissipation: $P_{I/O} = S\ (\{V_{DD} - V_{OH}\} \times I_{OH}) + S\ (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 37-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 64-pin QFN (9x9x0.9 mm)	θ_{JA}	28	—	°C/W	**1**
Package Thermal Resistance, 64-pin TQFP (10x10x1 mm)	θ_{JA}	49	—	°C/W	**1**
Package Thermal Resistance, 100-pin TQFP (12x12x1 mm)	θ_{JA}	43	—	°C/W	**1**
Package Thermal Resistance, 100-pin TQFP (14x14x1 mm)	θ_{JA}	40	—	°C/W	**1**
Package Thermal Resistance, 124-pin VTLA (9x9x0.9 mm)	θ_{JA}	30	—	°C/W	**1**
Package Thermal Resistance, 144-pin TQFP (16x16x1 mm)	θ_{JA}	42	—	°C/W	**1**
Package Thermal Resistance, 144-pin LQFP (20x20x1.4 mm)	θ_{JA}	39	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

TABLE 38-3: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for Extended	
Parameter No.	**Typical(2)**	**Maximum(4)**	**Units**	**Conditions**
Idle Current (IIDLE): Core Off, Clock on Base Current (Note 1)				
EDC30a	7	52	mA	4 MHz **(Note 3)**
EDC31a	8	56	mA	10 MHz
EDC32a	13	66	mA	60 MHz **(Note 3)**
EDC33a	21	86	mA	130 MHz **(Note 3)**
EDC34	26	96	mA	180 MHz **(Note 3)**

Note 1: The test conditions for IIDLE current measurements are as follows:

- Oscillator mode is EC+PLL with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBPMD = 1), VUSB3V3 is connected to VSS, PBCLKx divisor = 1:128 ('x' ≠ 7)
- CPU is in Idle mode (CPU core Halted)
- L1 Cache and Prefetch modules are disabled
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared (except USBPMD)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD
- RTCC and JTAG are disabled

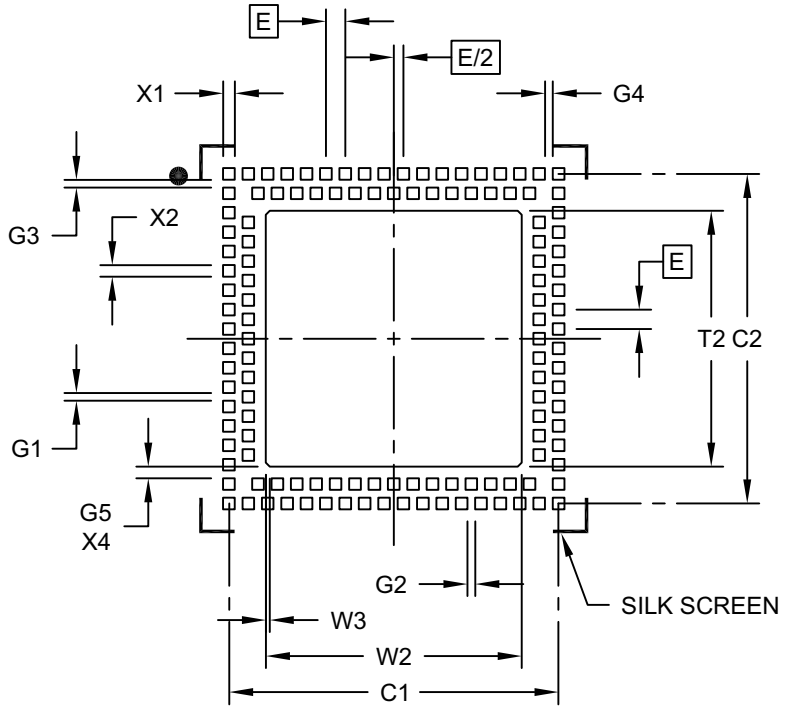
2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: This parameter is characterized, but not tested in manufacturing.

4: Data in the "Maximum" column is at 3.3V, +125ºC at specified operating frequency. Parameters are for design guidance only and are not tested.

124-Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Pad Clearance	G1	0.20		
Pad Clearance	G2	0.20		
Pad Clearance	G3	0.20		
Pad Clearance	G4	0.20		
Contact to Center Pad Clearance (X4)	G5	0.30		
Optional Center Pad Width	T2			6.60
Optional Center Pad Length	W2			6.60
Optional Center Pad Chamfer (X4)	W3		0.10	
Contact Pad Spacing	C1		8.50	
Contact Pad Spacing	C2		8.50	
Contact Pad Width (X124)	X1			0.30
Contact Pad Length (X124)	X2			0.30

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2193A

A.7 Interrupts and Exceptions

The key difference between Interrupt Controllers in PIC32MX5XX/6XX/7XX devices and PIC32MZ EF devices concerns vector spacing. Previous PIC32MX devices had fixed vector spacing, which is adjustable in set increments, and every interrupt had the same amount of space. PIC32MZ EF devices replace this with a variable offset spacing, where each interrupt has an offset register to determine where to begin execution.

In addition, the IFSx, IECx, and IPCx registers for old peripherals have shifted to different registers due to new peripherals. Please refer to **7.0 "CPU Exceptions and Interrupt Controller"** to determine where the interrupts are now located.

Table A-8 lists differences (indicated by **Bold** type) in the registers that will affect software migration.

TABLE A-8: INTERRUPT DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Vector Spacing	
On PIC32MX devices, the vector spacing was determined by the VS field in the CPU core. **VS<4:0> (IntCtl<9:5>: CP0 Register 12, Select 1)** **10000 = 512-byte vector spacing** **01000 = 256-byte vector spacing** **00100 = 128-byte vector spacing** **00010 = 64-byte vector spacing** **00001 = 32-byte vector spacing** **00000 = 0-byte vector spacing**	On PIC32MZ EF devices, the vector spacing is variable and determined by the Interrupt controller. The VOFFx<17:1> bits in the OFFx register are set to the offset from EBASE where the interrupt service routine is located. **VOFFx<17:1> (OFFx<17:1>)** **Interrupt Vector 'x' Address Offset bits**
Shadow Register Sets	
On PIC32MX devices, there was one shadow register set which could be used during interrupt processing. Which interrupt priority could use the shadow register set was determined by the FSRSSEL field in DEVCFG3 and SS0 on INTCON. **FSRSSEL<2:0> (DEVCFG3<18:16>)** **111 = Assign Interrupt Priority 7 to a shadow register set** **110 = Assign Interrupt Priority 6 to a shadow register set** • • • **001 = Assign Interrupt Priority 1 to a shadow register set** **000 = All interrupt priorities are assigned to a shadow register set** SS0 (**INTCON<16>**) 1 = Single vector is presented with a shadow register set 0 = Single vector is not presented with a shadow register set	On PIC32MZ EF devices, there are seven shadow register sets, and each priority level can be assigned a shadow register set to use via the PRIxSS<3:0> bits in the PRISS register. The SS0 bit is also moved to PRISS<0>. **PRIxSS<3:0> PRISS<y:z>** **1xxx = Reserved (by default, an interrupt with a priority level of x uses Shadow Set 0)** **0111 = Interrupt with a priority level of x uses Shadow Set 7** **0110 = Interrupt with a priority level of x uses Shadow Set 6** • • • **0001 = Interrupt with a priority level of x uses Shadow Set 1** **0000 = Interrupt with a priority level of x uses Shadow Set 0** SS0 (**PRISS<0>**) 1 = Single vector is presented with a shadow register set 0 = Single vector is not presented with a shadow register set
Status	
PIC32MX devices, the VEC<5:0> bits show which interrupt is being serviced. **VEC<5:0> (INTSTAT<5:0>)** 11111-00000 = The interrupt vector that is presented to the CPU	On PIC32MZ EF devices, the SIRQ<7:0> bits show the IRQ number of the interrupt last serviced. **SIRQ<7:0> (INTSTAT<7:0>)** 11111111-00000000 = The last interrupt request number serviced by the CPU

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