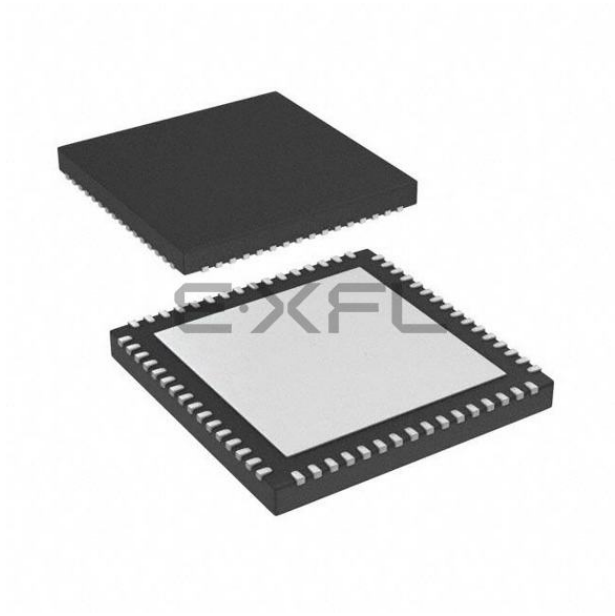
Microchip Technology - PIC32MZ0512EFK064T-I/MR Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	46
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512efk064t-i-mr

Device Pin Tables

TABLE 2: PIN NAMES FOR 64-PIN DEVICES

64-PIN QFN(4) AND TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)064
PIC32MZ1024EF(G/H/M)064
PIC32MZ1024EF(E/F/K)064
PIC32MZ2048EF(G/H/M)064

64 1 **QFN(4)** 64 1 **TQFP**

Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN17/ETXEN/RPE5/PMD5/RE5	33	VBUS
2	AN16/ETXD0/PMD6/RE6	34	VUSB3V3
3	AN15/ETXD1/PMD7/RE7	35	VSS
4	AN14/C1IND/RPG6/SCK2/PMA5/RG6	36	D-
5	AN13/C1INC/RPG7/SDA4/PMA4/RG7	37	D+
6	AN12/C2IND/RPG8/SCL4/PMA3/RG8	38	RPF3/USBID/RF3
7	VSS	39	VDD
8	VDD	40	VSS
9	$\overline{\text{MCLR}}$	41	RPF4/SDA5/PMA9/RF4
10	AN11/C2INC/RPG9/PMA2/RG9	42	RPF5/SCL5/PMA8/RF5
11	AN45/C1INA/RPB5/RB5	43	AERXD0/ETXD2/RPD9/SDA1/PMCS2/PMA15/RD9
12	AN4/C1INB/RB4	44	ECOL/RPD10/SCL1/SCK4/RD10
13	AN3/C2INA/RPB3/RB3	45	AERXCLK/AEREFCLK/ECRS/RPD11/PMCS1/PMA14/RD11
14	AN2/C2INB/RPB2/RB2	46	AERXD1/ETXD3/RPD0/RTCC/INT0/RD0
15	PGEC1/VREF-/CVREF-/AN1/RPB1/RB1	47	SOSCI/RPC13/RC13
16	PGED1/VREF+/CVREF+/AN0/RPB0/PMA6/RB0	48	SOSCO/RPC14/T1CK/RC14
17	PGEC2/AN46/RPB6/RB6	49	EMDIO/AEMDIO/RPD1/SCK1/RD1
18	PGED2/AN47/RPB7/RB7	50	ETXERR/AETXEN/RPD2/SDA3/RD2
19	AVDD	51	AERXERR/ETXCLK/RPD3/SCL3/RD3
20	AVSS	52	$\overline{\text{SQICS0}}$/RPD4/PMWR/RD4
21	AN48/RPB8/PMA10/RB8	53	$\overline{\text{SQICS1}}$/RPD5/PMRD/RD5
22	AN49/RPB9/PMA7/RB9	54	VDD
23	TMS/CVREFOUT/AN5/RPB10/PMA13/RB10	55	VSS
24	TDO/AN6/PMA12/RB11	56	ERXD3/AETXD1/RPF0/RF0
25	VSS	57	TRCLK/SQICLK/ERXD2/AETXD0/RPF1/RF1
26	VDD	58	TRD0/SQID0/ERXD1/PMD0/RE0
27	TCK/AN7/PMA11/RB12	59	VSS
28	TDI/AN8/RB13	60	VDD
29	AN9/RPB14/SCK3/PMA1/RB14	61	TRD1/SQID1/ERXD0/PMD1/RE1
30	AN10/EMDC/AEMDC/RPB15/OCFB/PMA0/RB15	62	TRD2/SQID2/ERXDV/ECRSDV/AECRSDV/PMD2/RE2
31	OSC1/CLKI/RC12	63	TRD3/SQID3/ERXCLK/EREFCLK/RPE3/PMD3/RE3
32	OSC2/CLKO/RC15	64	AN18/ERXERR/PMD4/RE4

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

TABLE 1-12: PMP PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PMA0	30	44	B24	30	I/O	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)
PMA1	29	43	A28	51	I/O	TTL/ST	Parallel Master Port Address bit 1 Input (Buffered Slave modes) and Output (Master modes)
PMA2	10	16	B9	21	O	—	Parallel Master Port Address (Demultiplexed Master modes)
PMA3	6	12	B7	52	O	—	
PMA4	5	11	A8	68	O	—	
PMA5	4	2	B1	2	O	—	
PMA6	16	6	B3	6	O	—	
PMA7	22	33	A23	48	O	—	
PMA8	42	65	A44	91	O	—	
PMA9	41	64	B36	90	O	—	
PMA10	21	32	B18	47	O	—	
PMA11	27	41	A27	29	O	—	
PMA12	24	7	A6	11	O	—	
PMA13	23	34	B19	28	O	—	
PMA14	45	61	A42	87	O	—	
PMA15	43	68	B38	97	O	—	
PMCS1	45	61	A42	87	O	—	Parallel Master Port Chip Select 1 Strobe
PMCS2	43	68	B38	97	O	—	Parallel Master Port Chip Select 2 Strobe
PMD0	58	91	B52	135	I/O	TTL/ST	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMD1	61	94	A64	138	I/O	TTL/ST	
PMD2	62	98	A66	142	I/O	TTL/ST	
PMD3	63	99	B56	143	I/O	TTL/ST	
PMD4	64	100	A67	144	I/O	TTL/ST	
PMD5	1	3	A3	3	I/O	TTL/ST	
PMD6	2	4	B2	4	I/O	TTL/ST	
PMD7	3	5	A4	5	I/O	TTL/ST	
PMD8	—	88	B50	128	I/O	TTL/ST	
PMD9	—	87	A60	127	I/O	TTL/ST	
PMD10	—	86	B49	125	I/O	TTL/ST	
PMD11	—	85	A59	124	I/O	TTL/ST	
PMD12	—	79	B43	112	I/O	TTL/ST	
PMD13	—	80	A54	113	I/O	TTL/ST	
PMD14	—	77	B42	110	I/O	TTL/ST	
PMD15	—	78	A53	111	I/O	TTL/ST	
PMALL	30	44	B24	30	O	—	Parallel Master Port Address Latch Enable Low Byte (Multiplexed Master modes)
PMALH	29	43	A28	51	O	—	Parallel Master Port Address Latch Enable High Byte (Multiplexed Master modes)
PMRD	53	9	A7	13	O	—	Parallel Master Port Read Strobe
PMWR	52	8	B5	12	O	—	Parallel Master Port Write Strobe

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 4-14: SYSTEM BUS TARGET 6 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9820	SBT6ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
9824	SBT6ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
9828	SBT6ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9830	SBT6ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9838	SBT6ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9840	SBT6REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9850	SBT6RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9858	SBT6WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9860	SBT6REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9870	SBT6RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9878	SBT6WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

TABLE 4-16: SYSTEM BUS TARGET 8 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A020	SBT8ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
A024	SBT8ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
A028	SBT8ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
A030	SBT8ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A038	SBT8ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A040	SBT8REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
A050	SBT8RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A058	SBT8WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A060	SBT8REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
A070	SBT8RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A078	SBT8WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MZ EF devices contain an internal Flash program memory for executing user code, which includes the following features:

- Two Flash banks for live update support
- Dual boot support
- Write protection for program and boot Flash
- ECC support

There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193) in the *"PIC32 Family Reference Manual".*

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the *"PIC32 Flash Programming Specification"* (DS60001145), which is available for download from the Microchip web site (www.microchip.com).

Note: In PIC32MZ EF devices, the Flash page size is 16 KB (4K IW) and the row size is 2 KB (512 IW).

REGISTER 10-1: DMACON: DMA CONTROLLER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
	ON	—	—	SUSPEND	DMABUSY	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** DMA On bit
- 1 = DMA module is enabled
- 0 = DMA module is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **SUSPEND:** DMA Suspend bit
- 1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
- 0 = DMA operates normally

bit 11 **DMABUSY:** DMA Module Busy bit
- 1 = DMA module is active and is transferring data
- 0 = DMA module is disabled and not actively transferring data

bit 10-0 **Unimplemented:** Read as '0'

REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

bit 6 **CRCAPP:** CRC Append Mode bit(1)
1 = The DMA transfers data from the source into the CRC but NOT to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA
0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination

bit 5 **CRCTYP:** CRC Type Selection bit
1 = The CRC module will calculate an IP header checksum
0 = The CRC module will calculate a LFSR CRC

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **CRCCH<2:0>:** CRC Channel Select bits
111 = CRC is assigned to Channel 7
110 = CRC is assigned to Channel 6
101 = CRC is assigned to Channel 5
100 = CRC is assigned to Channel 4
011 = CRC is assigned to Channel 3
010 = CRC is assigned to Channel 2
001 = CRC is assigned to Channel 1
000 = CRC is assigned to Channel 0

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

REGISTER 10-9: DCHxINT: DMA CHANNEL x INTERRUPT CONTROL REGISTER (CONTINUED)

bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit
1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
0 = No interrupt is pending

bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
0 = No interrupt is pending

bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
0 = No interrupt is pending

bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
0 = No interrupt is pending

bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
0 = No interrupt is pending

bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
1 = A channel address error has been detected
Either the source or the destination address is invalid.
0 = No interrupt is pending

12.4.3 CONTROLLING PPS

PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

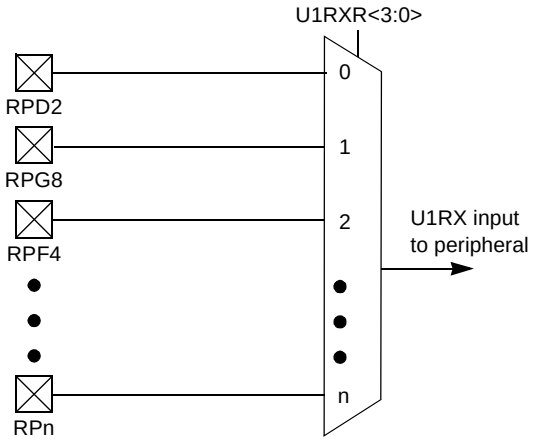
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

12.4.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [*pin name*]R registers, where [*pin name*] refers to the peripheral pins listed in Table 12-2, are used to configure peripheral input mapping (see Register 12-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 12-2.

For example, Figure 12-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 12-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

TABLE 12-21: PORTK REGISTER MAP FOR 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0910	TRISK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRISK7	TRISK6	TRISK5	TRISK4	TRISK3	TRISK2	TRISK1	TRISK0	00FF
0920	PORTK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	RK7	RK6	RK5	RK4	RK3	RK2	RK1	RK0	xxxx
0930	LATK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LATK7	LATK6	LATK5	LATK4	LATK3	LATK2	LATK1	LATK0	xxxx
0940	ODCK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ODCK7	ODCK6	ODCK5	ODCK4	ODCK3	ODCK2	ODCK1	ODCK0	0000
0950	CNPUK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPUK7	CNPUK6	CNPUK5	CNPUK4	CNPUK3	CNPUK2	CNPUK1	CNPUK0	0000
0960	CNPDK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPDK7	CNPDK6	CNPDK5	CNPDK4	CNPDK3	CNPDK2	CNPDK1	CNPDK0	0000
0970	CNCONK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0980	CNENK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNENK7	CNENK6	CNENK5	CNENK4	CNENK3	CNENK2	CNENK1	CNENK0	0000
0990	CNSTATK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CN STATK7	CN STATK6	CN STATK5	CN STATK4	CN STATK3	CN STATK2	CN STATK1	CN STATK0	0000
09A0	CNNEK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNNEK7	CNNEK6	CNNEK5	CNNEK4	CNNEK3	CNNEK2	CNNEK1	CNNEK0	0000
09B0	CNFK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNFK7	CNFK6	CNFK5	CNFK4	CNFK3	CNFK2	CNFK1	CNFK0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

17.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin.

Capture events are caused by the following:

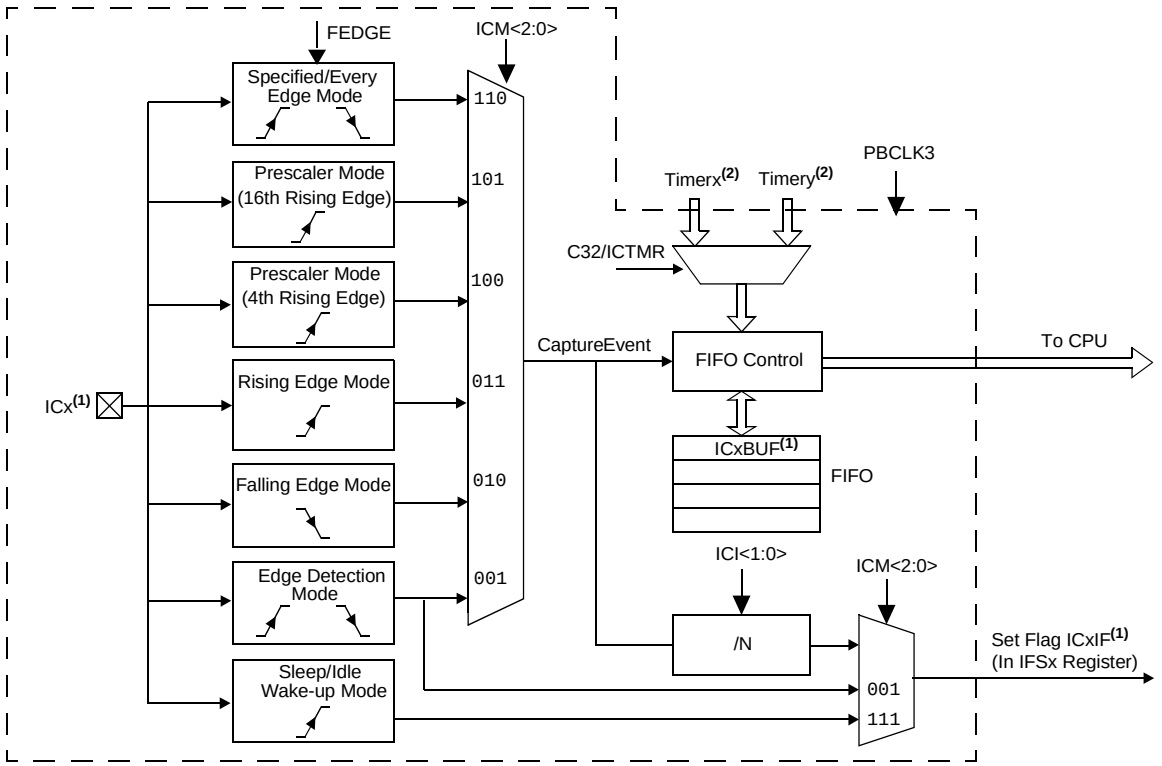
- Capture timer value on every edge (rising and falling), specified edge first
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of six 16-bit timers for the time base, or two of six 16-bit timers together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values; Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

FIGURE 17-1: INPUT CAPTURE BLOCK DIAGRAM



Note 1: An 'x' in a signal, register or bit name denotes the number of the capture channel.

2: See Table 17-1 for Timerx and Timery selections.

21.0 INTER-INTEGRATED CIRCUIT (I^2C)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. "Inter-Integrated Circuit (I^2C)"** (DS60001116) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The I^2C module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard.

Each I^2C module has a 2-pin interface:

- SCLx pin is clock
- SDAx pin is data

Each I^2C module offers the following key features:

- I^2C interface supporting both master and slave operation
- I^2C Slave mode supports 7-bit and 10-bit addressing
- I^2C Master mode supports 7-bit and 10-bit addressing
- I^2C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I^2C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I^2C supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking
- SMBus support

Figure 21-1 illustrates the I^2C module block diagram.

REGISTER 24-2: EBIMSKx: EXTERNAL BUS INTERFACE ADDRESS MASK REGISTER ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	REGSEL<2:0>		
7:0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MEMTYPE<2:0>			MEMSIZE<4:0>(1)				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **REGSEL<2:0>:** Timing Register Set for Chip Select 'x' bits
111 = Reserved
•
•
•
011 = Reserved
010 = Use EBISMT2
001 = Use EBISMT1
000 = Use EBISMT0

bit 7-5 **MEMTYPE<2:0>:** Select Memory Type for Chip Select 'x' bits
111 = Reserved
•
•
•
011 = Reserved
010 = NOR-Flash
001 = SRAM
000 = Reserved

bit 4-0 **MEMSIZE<4:0>:** Select Memory Size for Chip Select 'x' bits(1)
11111 = Reserved
•
•
•
01010 = Reserved
01001 = 16 MB
01000 = 8 MB
00111 = 4 MB
00110 = 2 MB
00101 = 1 MB
00100 = 512 KB
00011 = 256 KB
00010 = 128 KB
00001 = 64 KB (smaller memories alias within this range)
00000 = Chip Select is not used

Note 1: The specified value for these bits depends on the number of available address lines. Refer to the specific device pin table (Table 2 through Table 5) for the available address lines.

REGISTER 25-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN(1,2)	CHIME(2)	PIV(2)	ALRMSYNC	AMASK<3:0>(2)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARPT<7:0>(2)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ALRMEN:** Alarm Enable bit(1,2)
- 1 = Alarm is enabled
- 0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit(2)
- 1 = Chime is enabled – ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
- 0 = Chime is disabled – ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit(2)

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse.
When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 **ALRMSYNC:** Alarm Sync bit
- 1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing.
- 0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is more than 32 real-time clocks away from a half-second rollover

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits(2)
- 0000 = Every half-second
- 0001 = Every second
- 0010 = Every 10 seconds
- 0011 = Every minute
- 0100 = Every 10 minutes
- 0101 = Every hour
- 0110 = Once a day
- 0111 = Once a week
- 1000 = Once a month
- 1001 = Once a year (except when configured for February 29, once every four years)
- 1010 = Reserved
- 1011 = Reserved
- 11xx = Reserved

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

Note: This register is reset only on a Power-on Reset (POR).

REGISTER 28-6: ADCIMCON2: ADC INPUT MODE CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF31(1)	SIGN31(1)	DIFF30(1)	SIGN30(1)	DIFF29(1)	SIGN29(1)	DIFF28(1)	SIGN28(1)
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF27(1)	SIGN27(1)	DIFF26(1)	SIGN26(1)	DIFF25(1)	SIGN25(1)	DIFF24(1)	SIGN24(1)
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF23(1)	SIGN23(1)	DIFF22(1)	SIGN22(1)	DIFF21(1)	SIGN21(1)	DIFF20(1)	SIGN20(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF19(1)	SIGN19(1)	DIFF18	SIGN18	DIFF17	SIGN17	DIFF16	SIGN16

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **DIFF31:** AN31 Mode bit(1)
1 = AN31 is using Differential mode
0 = AN31 is using Single-ended mode

bit 30 **SIGN31:** AN31 Signed Data Mode bit(1)
1 = AN31 is using Signed Data mode
0 = AN31 is using Unsigned Data mode

bit 29 **DIFF30:** AN30 Mode bit(1)
1 = AN30 is using Differential mode
0 = AN30 is using Single-ended mode

bit 28 **SIGN30:** AN30 Signed Data Mode bit(1)
1 = AN30 is using Signed Data mode
0 = AN30 is using Unsigned Data mode

bit 27 **DIFF29:** AN29 Mode bit(1)
1 = AN29 is using Differential mode
0 = AN29 is using Single-ended mode

bit 26 **SIGN29:** AN29 Signed Data Mode bit(1)
1 = AN29 is using Signed Data mode
0 = AN29 is using Unsigned Data mode

bit 25 **DIFF28:** AN28 Mode bit(1)
1 = AN28 is using Differential mode
0 = AN28 is using Single-ended mode

bit 24 **SIGN28:** AN28 Signed Data Mode bit(1)
1 = AN28 is using Signed Data mode
0 = AN28 is using Unsigned Data mode

bit 23 **DIFF27:** AN27 Mode bit(1)
1 = AN27 is using Differential mode
0 = AN27 is using Single-ended mode

bit 22 **SIGN27:** AN27 Signed Data Mode bit(1)
1 = AN27 is using Signed Data mode
0 = AN27 is using Unsigned Data mode

Note 1: This bit is not available on 64-pin devices.

REGISTER 30-16: ETHRXOVFLOW: ETHERNET CONTROLLER RECEIVE OVERFLOW STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXOVFLWCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXOVFLWCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RXOVFLWCNT<15:0>:** Dropped Receive Frames Count bits

Increment counter for frames accepted by the RX filter and subsequently dropped due to internal receive error (RXFIFO overrun). This event also sets the RXOVFLW bit (ETHIRQ<0>) interrupt flag.

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 34-4: DEVCFG1/ADEVCFG1: DEVICE CONFIGURATION WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FDMTEN	DMTCNT<4:0>					FWDTWINSZ<1:0>	
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>				
15:8	R/P	R/P	r-1	r-1	r-1	R/P	R/P	R/P
	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	IESO	FSOSCEN	DMTINTV<2:0>			FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FDMTEN:** Deadman Timer enable bit
1 = Deadman Timer is enabled and *cannot* be disabled by software
0 = Deadman Timer is disabled and *can* be enabled by software

bit 30-26 **DMTCNT<4:0>:** Deadman Timer Count Select bits
11111 = Reserved
•
•
•
11000 = Reserved
10111 = 2^{31} (2147483648)
10110 = 2^{30} (1073741824)
10101 = 2^{29} (536870912)
10100 = 2^{28} (268435456)
•
•
•
00001 = 2^{9} (512)
00000 = 2^{8} (256)

bit 25-24 **FWDTWINSZ<1:0>:** Watchdog Timer Window Size bits
11 = Window size is 25%
10 = Window size is 37.5%
01 = Window size is 50%
00 = Window size is 75%

bit 23 **FWDTEN:** Watchdog Timer Enable bit
1 = Watchdog Timer is enabled and cannot be disabled by software
0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS:** Watchdog Timer Window Enable bit
1 = Watchdog Timer is in non-Window mode
0 = Watchdog Timer is in Window mode

bit 21 **WDTSPGM:** Watchdog Timer Stop During Flash Programming bit
1 = Watchdog Timer stops during Flash programming
0 = Watchdog Timer runs during Flash programming (for read/execute while programming Flash applications)

REGISTER 34-9: CFGEBIC: EXTERNAL BUS INTERFACE CONTROL PIN CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0
	EBI RDYINV3	EBI RDYINV2	EBI RDYIN1	—	EBI RDYEN3	EBI RDYEN2	EBI RDYEN1	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	EBIRDYLVL	EBIRPEN
15:8	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	—	EBIWEEN	EBIOEEN	—	—	EBIBSEN1	EBIBSEN0
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	EBICSEN3	EBICSEN2	EBICSEN1	EBICSEN0	—	—	EBIDEN1	EBIDEN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **EBIRDYINV3:** EBIRDY3 Inversion Control bit
1 = Invert EBIRDY3 pin before use
0 = Do not invert EBIRDY3 pin before use

bit 30 **EBIRDYINV2:** EBIRDY2 Inversion Control bit
1 = Invert EBIRDY2 pin before use
0 = Do not invert EBIRDY2 pin before use

bit 29 **EBIRDYINV1:** EBIRDY1 Inversion Control bit
1 = Invert EBIRDY1 pin before use
0 = Do not invert EBIRDY1 pin before use

bit 28 **Unimplemented:** Read as '0'

bit 27 **EBIRDYEN3:** EBIRDY3 Pin Enable bit
1 = EBIRDY3 pin is enabled for use by the EBI module
0 = EBIRDY3 pin is available for general use

bit 26 **EBIRDYEN2:** EBIRDY2 Pin Enable bit
1 = EBIRDY2 pin is enabled for use by the EBI module
0 = EBIRDY2 pin is available for general use

bit 25 **EBIRDYEN1:** EBIRDY1 Pin Enable bit
1 = EBIRDY1 pin is enabled for use by the EBI module
0 = EBIRDY1 pin is available for general use

bit 24-18 **Unimplemented:** Read as '0'

bit 17 **EBIRDYLVL:** EBIRDYx Pin Sensitivity Control bit
1 = Use level detect for EBIRDYx pins
0 = Use edge detect for EBIRDYx pins

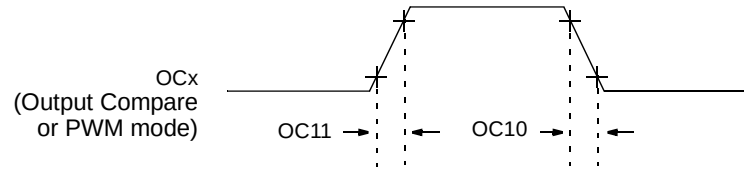
bit 16 **EBIRPEN:** $\overline{\text{EBIRP}}$ Pin Sensitivity Control bit
1 = $\overline{\text{EBIRP}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIRP}}$ pin is available for general use

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **EBIWEEN:** $\overline{\text{EBIWE}}$ Pin Enable bit
1 = $\overline{\text{EBIWE}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIWE}}$ pin is available for general use

Note: When EBIMD = 1, the bits in this register are ignored and the pins are available for general use.

FIGURE 37-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS



Note: Refer to Figure 37-1 for load conditions.

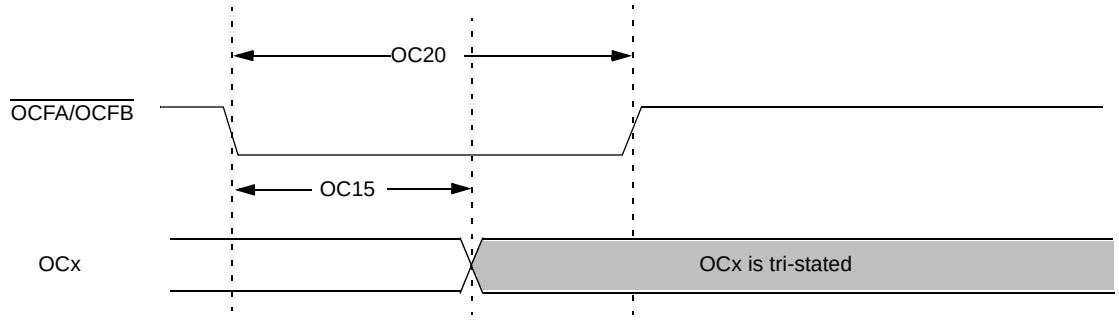
TABLE 37-28: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See parameter DO31

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 37-9: OCx/PWM MODULE TIMING CHARACTERISTICS



Note: Refer to Figure 37-1 for load conditions.

TABLE 37-29: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Typical(2)**	**Max**	**Units**	**Conditions**
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	—
OC20	TFLT	Fault Input Pulse Width	50	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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