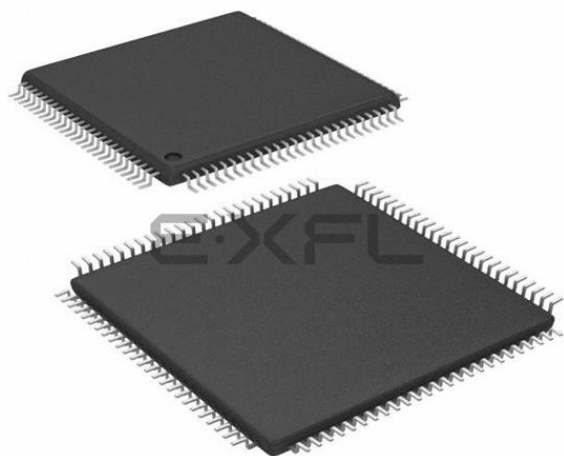




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Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512efk100-i-pf

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTA							
RA0	—	17	A11	22	I/O	ST	PORTA is a bidirectional I/O port
RA1	—	38	B21	56	I/O	ST	
RA2	—	59	A41	85	I/O	ST	
RA3	—	60	B34	86	I/O	ST	
RA4	—	61	A42	87	I/O	ST	
RA5	—	2	B1	2	I/O	ST	
RA6	—	89	A61	129	I/O	ST	
RA7	—	90	B51	130	I/O	ST	
RA9	—	28	B15	39	I/O	ST	
RA10	—	29	A20	40	I/O	ST	
RA14	—	66	B37	95	I/O	ST	
RA15	—	67	A45	96	I/O	ST	
PORTB							
RB0	16	25	A18	36	I/O	ST	PORTB is a bidirectional I/O port
RB1	15	24	A17	35	I/O	ST	
RB2	14	23	A16	34	I/O	ST	
RB3	13	22	A14	31	I/O	ST	
RB4	12	21	A13	26	I/O	ST	
RB5	11	20	B11	25	I/O	ST	
RB6	17	26	B14	37	I/O	ST	
RB7	18	27	A19	38	I/O	ST	
RB8	21	32	B18	47	I/O	ST	
RB9	22	33	A23	48	I/O	ST	
RB10	23	34	B19	49	I/O	ST	
RB11	24	35	A24	50	I/O	ST	
RB12	27	41	A27	59	I/O	ST	
RB13	28	42	B23	60	I/O	ST	
RB14	29	43	A28	61	I/O	ST	
RB15	30	44	B24	62	I/O	ST	
PORTC							
RC1	—	6	B3	6	I/O	ST	PORTC is a bidirectional I/O port
RC2	—	7	A6	11	I/O	ST	
RC3	—	8	B5	12	I/O	ST	
RC4	—	9	A7	13	I/O	ST	
RC12	31	49	B28	71	I/O	ST	
RC13	47	72	B41	105	I/O	ST	
RC14	48	73	A49	106	I/O	ST	
RC15	32	50	A33	72	I/O	ST	

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

2.10 Typical Application Connection Examples

TABLE 4-9: SYSTEM BUS TARGET 1 REGISTER MAP (CONTINUED)

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
84E0	SBT1REG5	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>					PRI	—	SIZE<4:0>					—	—	—	xxxx
84F0	SBT1RD5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84F8	SBT1WR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8500	SBT1REG6	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>					PRI	—	SIZE<4:0>					—	—	—	xxxx
8510	SBT1RD6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8518	SBT1WR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8520	SBT1REG7	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>					PRI	—	SIZE<4:0>					—	—	—	xxxx
8530	SBT1RD7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8538	SBT1WR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8540	SBT1REG8	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>					PRI	—	SIZE<4:0>					—	—	—	xxxx
8550	SBT1RD8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8558	SBT1WR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
UART6 Transfer Done	_UART6_TX_VECTOR	190	OFF190<17:1>	IFS5<30>	IEC5<30>	IPC47<20:18>	IPC47<17:16>	Yes
Reserved	—	191	—	—	—	—	—	—
ADC End of Scan Ready	_ADC_EOS_VECTOR	192	OFF192<17:1>	IFS6<0>	IEC6<0>	IPC48<4:2>	IPC48<1:0>	Yes
ADC Analog Circuits Ready	_ADC_ARDY_VECTOR	193	OFF193<17:1>	IFS6<1>	IEC6<1>	IPC48<12:10>	IPC48<9:8>	Yes
ADC Update Ready	_ADC_URDY_VECTOR	194	OFF194<17:1>	IFS6<2>	IEC6<2>	IPC48<20:18>	IPC48<17:16>	Yes
Reserved	—	195	—	—	—	—	—	—
ADC Group Early Interrupt Request	_ADC_EARLY_VECTOR	196	OFF196<17:1>	IFS6<4>	IEC6<4>	IPC49<4:2>	IPC49<1:0>	Yes
Reserved	—	197	—	—	—	—	—	—
ADC0 Early Interrupt	_ADC0_EARLY_VECTOR	198	OFF198<17:1>	IFS6<6>	IEC6<6>	IPC49<20:18>	IPC49<17:16>	Yes
ADC1 Early Interrupt	_ADC1_EARLY_VECTOR	199	OFF199<17:1>	IFS6<7>	IEC6<7>	IPC49<28:26>	IPC49<25:24>	Yes
ADC2 Early Interrupt	_ADC2_EARLY_VECTOR	200	OFF200<17:1>	IFS6<8>	IEC6<8>	IPC50<4:2>	IPC50<1:0>	Yes
ADC3 Early Interrupt	_ADC2_EARLY_VECTOR	201	OFF201<17:1>	IFS6<9>	IEC6<9>	IPC50<12:10>	IPC50<9:8>	Yes
ADC4 Early Interrupt	_ADC4_EARLY_VECTOR	202	OFF202<17:1>	IFS6<10>	IEC6<10>	IPC50<20:18>	IPC50<17:16>	Yes
Reserved	—	203	—	—	—	—	—	—
Reserved	—	204	—	—	—	—	—	—
ADC7 Early Interrupt	_ADC7_EARLY_VECTOR	205	OFF205<17:1>	IFS6<13>	IEC6<13>	IPC51<12:10>	IPC51<9:8>	Yes
ADC0 Warm Interrupt	_ADC0_WARM_VECTOR	206	OFF206<17:1>	IFS6<14>	IEC6<14>	IPC51<20:18>	IPC51<17:16>	Yes
ADC1 Warm Interrupt	_ADC1_WARM_VECTOR	207	OFF207<17:1>	IFS6<15>	IEC6<15>	IPC51<28:26>	IPC51<25:24>	Yes
ADC2 Warm Interrupt	_ADC2_WARM_VECTOR	208	OFF208<17:1>	IFS6<16>	IEC6<16>	IPC52<4:2>	IPC52<1:0>	Yes
ADC3 Warm Interrupt	_ADC3_WARM_VECTOR	209	OFF209<17:1>	IFS6<17>	IEC6<17>	IPC52<12:10>	IPC52<9:8>	Yes
ADC4 Warm Interrupt	_ADC4_WARM_VECTOR	210	OFF210<17:1>	IFS6<18>	IEC6<18>	IPC52<20:18>	IPC52<17:16>	Yes
Reserved	—	211	—	—	—	—	—	—
Reserved	—	212	—	—	—	—	—	—
ADC7 Warm Interrupt	_ADC7_WARM_VECTOR	213	OFF213<17:1>	IFS6<21>	IEC6<21>	IPC53<12:10>	IPC53<9:8>	Yes
Lowest Natural Order Priority								

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MZ EF Family Features”** for the list of available peripherals.

- 2:** This interrupt source is not available on 64-pin devices.
3: This interrupt source is not available on 100-pin devices.
4: This interrupt source is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0584	OFF017	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
0588	OFF018	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
058C	OFF019	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
0590	OFF020	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
0594	OFF021	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
0598	OFF022	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
059C	OFF023	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05A0	OFF024	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05A4	OFF025	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05A8	OFF026	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05AC	OFF027	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05B0	OFF028	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05B4	OFF029	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05B8	OFF030	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05BC	OFF031	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.
 - 2: This bit or register is not available on 64-pin devices.
 - 3: This bit or register is not available on devices without a CAN module.
 - 4: This bit or register is not available on 100-pin devices.
 - 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
 - 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
 - 7: This bit or register is not available on devices without a Crypto module.
 - 8: This bit or register is not available on 124-pin devices.

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REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

.

.

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

.

.

.

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-2 for the exact bit definitions.

8.0 OSCILLATOR CONFIGURATION

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 42. “Oscillators with Enhanced PLL”** (DS60001250) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32MZ EF oscillator system has the following modules and features:

- A total of five external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown with dedicated Back-up FRC (BFRC)
- Dedicated On-Chip PLL for USB peripheral
- Flexible reference clock output
- Multiple clock branches for peripherals for better performance flexibility
- Clock switch/slew control with output divider

A block diagram of the oscillator system is shown in Figure 8-1. The clock distribution is provided in Table 8-1.

Note: Devices that support 252 MHz operation should be configured for $\text{SYSCLK} \leq 200 \text{ MHz}$ operation. Adjust the dividers of the PBCLKs, and then increase the SYSCLK to the desired speed.

REGISTER 11-1: USBCSR0: USB CONTROL STATUS REGISTER 0 (CONTINUED)

- bit 10 **RESUME:** Resume from Suspend control bit
 1 = Generate Resume signaling when the device is in Suspend mode
 0 = Stop Resume signaling
- In *Device mode*, the software should clear this bit after 10 ms (a maximum of 15 ms) to end Resume signaling. In *Host mode*, the software should clear this bit after 20 ms.
- bit 9 **SUSPMODE:** Suspend Mode status bit
 1 = The USB module is in Suspend mode
 0 = The USB module is in Normal operations
- This bit is read-only in *Device mode*. In *Host mode*, it can be set by software, and is cleared by hardware.
- bit 8 **SUSPEN:** Suspend Mode Enable bit
 1 = Suspend mode is enabled
 0 = Suspend mode is not enabled
- bit 7 **Unimplemented:** Read as '0'
- bit 6-0 **FUNC<6:0>:** Device Function Address bits
- These bits are only available in *Device mode*. This field is written with the address received through a SET_ADDRESS command, which will then be used for decoding the function address in subsequent token packets.

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REGISTER 11-3: USBCSR2: USB CONTROL STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 VBUSERRIE	R/W-0 SESSRQIE	R/W-0 DISCONIE	R/W-0 CONNIE	R/W-0 SOFIE	R/W-1 RESETIE	R/W-1 RESUMEIE	R/W-0 SUSPIE
23:16	R-0, HS VBUSERRIF	R-0, HS SESSRQIF	R-0, HS DISCONIF	R-0, HS CONNIF	R-0, HS SOFIF	R-0, HS RESETIF	R-0, HS RESUMEIF	R-0, HS SUSPIF
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	R/W-1 EP7RXIE	R/W-1 EP6RXIE	R/W-1 EP5RXIE	R/W-1 EP4RXIE	R/W-1 EP3RXIE	R/W-1 EP2RXIE	R/W-1 EP1RXIE	U-0 —

Legend:

R = Readable bit

-n = Value at POR

HS = Hardware Set

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

- bit 31 **VBUSERRIE:** VBUS Error Interrupt Enable bit
1 = VBUS error interrupt is enabled
0 = VBUS error interrupt is disabled
- bit 30 **SESSRQIE:** Session Request Interrupt Enable bit
1 = Session request interrupt is enabled
0 = Session request interrupt is disabled
- bit 29 **DISCONIE:** Device Disconnect Interrupt Enable bit
1 = Device disconnect interrupt is enabled
0 = Device disconnect interrupt is disabled
- bit 28 **CONNIE:** Device Connection Interrupt Enable bit
1 = Device connection interrupt is enabled
0 = Device connection interrupt is disabled
- bit 27 **SOFIE:** Start of Frame Interrupt Enable bit
1 = Start of Frame event interrupt is enabled
0 = Start of Frame event interrupt is disabled
- bit 26 **RESETIE:** Reset/Babble Interrupt Enable bit
1 = Interrupt when reset (*Device mode*) or Babble (*Host mode*) is enabled
0 = Reset/Babble interrupt is disabled
- bit 25 **RESUMEIE:** Resume Interrupt Enable bit
1 = Resume signaling interrupt is enabled
0 = Resume signaling interrupt is disabled
- bit 24 **SUSPIE:** Suspend Interrupt Enable bit
1 = Suspend signaling interrupt is enabled
0 = Suspend signaling interrupt is disabled
- bit 23 **VBUSERRIF:** VBUS Error Interrupt bit
1 = VBUS has dropped below the VBUS valid threshold during a session
0 = No interrupt
- bit 22 **SESSRQIF:** Session Request Interrupt bit
1 = Session request signaling has been detected
0 = No session request detected
- bit 21 **DISCONIF:** Device Disconnect Interrupt bit
1 = In *Host mode*, indicates when a device disconnect is detected. In *Device mode*, indicates when a session ends.
0 = No device disconnect detected
- bit 20 **CONNIF:** Device Connection Interrupt bit
1 = In *Host mode*, indicates when a device connection is detected
0 = No device connection detected

TABLE 12-6: PORTC REGISTER MAP FOR 100-PIN, 124-PIN, AND 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	ANSELC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	ANSC4	ANSC3	ANSC2	ANSC1	—	001E
0210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	TRISC4	TRISC3	TRISC2	TRISC1	—	F01E
0220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	RC4	RC3	RC2	RC1	—	xxxx
0230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	LATC4	LATC3	LATC2	LATC1	—	xxxx
0240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	ODCC4	ODCC3	ODCC2	ODCC1	—	0000
0250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUC15	CNPUC14	CNPUC13	CNPUC12	—	—	—	—	—	—	—	CNPUC4	CNPUC3	CNPUC2	CNPUC1	—	0000
0260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDC15	CNPDC14	CNPDC13	CNPDC12	—	—	—	—	—	—	—	CNPDC4	CNPDC3	CNPDC2	CNPDC1	—	0000
0270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0280	CNENC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNENC15	CNENC14	CNENC13	CNENC12	—	—	—	—	—	—	—	CNENC4	CNENC3	CNENC2	CNENC1	—	0000
0290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATC15	CNSTATC14	CNSTATC13	CNSTATC12	—	—	—	—	—	—	—	CNSTATC4	CNSTATC3	CNSTATC2	CNSTATC1	—	0000
02A0	CNNEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEC15	CNNEC14	CNNEC13	CNNEC12	—	—	—	—	—	—	—	CNNEC4	CNNEC3	CNNEC2	CNNEC1	—	0000
02B0	CNFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFC15	CNFC14	CNFC13	CNFC12	—	—	—	—	—	—	—	CNFC4	CNFC3	CNFC2	CNFC1	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

TABLE 12-8: PORTD REGISTER MAP FOR 124-PIN AND 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0300	ANSELD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSD15	ANSD14	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C000
0310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	—	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FEFF
0320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	—	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
0330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	—	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
0340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	—	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
0350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUD15	CNPUD14	CNPUD13	CNPUD12	CNPUD11	CNPUD10	CNPUD9	—	CNPUD7	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
0360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDD15	CNPDD14	CNPDD13	CNPDD12	CNPDD11	CNPDD10	CNPDD9	—	CNPDD7	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
0370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNEND15	CNEND14	CNEND13	CNEND12	CNEND11	CNEND10	CNEND9	—	CNEND7	CNEND6	CNEND5	CNEND4	CNEND3	CNEND2	CNEND1	CNEND0	0000
0390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATD15	CN STATD14	CN STATD13	CN STATD12	CN STATD11	CN STATD10	CN STATD9	—	CN STATD7	CN STATD6	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	CN STATD0	0000
03A0	CNNED	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNED15	CNNED14	CNNED13	CNNED12	CNNED11	CNNED10	CNNED9	—	CNNED7	CNNED6	CNNED5	CNNED4	CNNED3	CNNED2	CNNED1	CNNED0	0000
03B0	CNFD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFD15	CNFD14	CNFD13	CNFD12	CNFD11	CNFD10	CNFD9	—	CNFD7	CNFD6	CNFD5	CNFD4	CNFD3	CNFD2	CNFD1	CNFD0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9) (CONTINUED)

- bit 2 **Unimplemented:** Read as '0'
- bit 1 **TCS:** Timer Clock Source Select bit⁽¹⁾
 1 = External clock from TxCK pin
 0 = Internal peripheral clock
- bit 0 **Unimplemented:** Read as '0'

- Note 1:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, Timer5, Timer7, and Timer9). All timer functions are set through the even numbered timers.
- 2:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.
- 3:** This bit is available only on even numbered timers (Timer2, Timer4, Timer6, and Timer8).

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 19-3: SPIxSTAT: SPI STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	RXBUFELM<4:0>				
23:16	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	TXBUFELM<4:0>				
15:8	U-0	U-0	U-0	R/C-0, HS	R-0	U-0	U-0	R-0
	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR
7:0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0
	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF

Legend:	C = Clearable bit	HS = Set in hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **RXBUFELM<4:0>**: Receive Buffer Element Count bits (valid only when ENHBUF = 1)

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFELM<4:0>**: Transmit Buffer Element Count bits (valid only when ENHBUF = 1)

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **FRMERR**: SPI Frame Error status bit

1 = Frame error is detected

0 = No Frame error is detected

This bit is only valid when FRMEN = 1.

bit 11 **SPIBUSY**: SPI Activity Status bit

1 = SPI peripheral is currently busy with some transactions

0 = SPI peripheral is currently idle

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPITUR**: Transmit Under Run bit

1 = Transmit buffer has encountered an underrun condition

0 = Transmit buffer has no underrun condition

This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling/re-enabling the module.

bit 7 **SRMT**: Shift Register Empty bit (valid only when ENHBUF = 1)

1 = When SPI module shift register is empty

0 = When SPI module shift register is not empty

bit 6 **SPIROV**: Receive Overflow Flag bit

1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.

0 = No overflow has occurred

This bit is set in hardware; can only be cleared (= 0) in software.

bit 5 **SPIRBE**: RX FIFO Empty bit (valid only when ENHBUF = 1)

1 = RX FIFO is empty (CRPTR = SWPTR)

0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 **Unimplemented:** Read as '0'

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REGISTER 23-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

- bit 7-6 **CSF<1:0>**: Chip Select Function bits⁽¹⁾
11 = Reserved
10 = PMCS1 and PMCS2 function as Chip Select
01 = PMCS2 functions as Chip Select and PMCS1 functions as address bit 14
00 = PMCS1 and PMCS2 function as address bit 14 and address bit 15
- bit 5 **ALP**: Address Latch Polarity bit⁽¹⁾
1 = Active-high (PMALL and PMALH)
0 = Active-low (PMALL and PMALH)
- bit 4 **CS2P**: Chip Select 2 Polarity bit⁽¹⁾
1 = Active-high (PMCS2)
0 = Active-low (PMCS2)
- bit 3 **CS1P**: Chip Select 1 Polarity bit⁽¹⁾
1 = Active-high (PMCS1)
0 = Active-low (PMCS1)
- bit 2 **Unimplemented**: Read as '0'
- bit 1 **WRSP**: Write Strobe Polarity bit
For Slave Modes and Master mode 2 (MODE<1:0> = 00,01,10):
1 = Write strobe active-high (PMWR)
0 = Write strobe active-low (PMWR)
For Master mode 1 (MODE<1:0> = 11):
1 = Enable strobe active-high (PMENB)
0 = Enable strobe active-low (PMENB)
- bit 0 **RDSP**: Read Strobe Polarity bit
For Slave modes and Master mode 2 (MODE<1:0> = 00,01,10):
1 = Read Strobe active-high (PMRD)
0 = Read Strobe active-low (PMRD)
For Master mode 1 (MODE<1:0> = 11):
1 = Read/write strobe active-high (PMRD/PMWR)
0 = Read/write strobe active-low (PMRD/PMWR)

Note 1: These bits have no effect when their corresponding pins are used as address lines.

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REGISTER 28-12: ADCDSTAT1: ADC DATA READY STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC ARDY31 ⁽¹⁾	R-0, HS, HC ARDY30 ⁽¹⁾	R-0, HS, HC ARDY29 ⁽¹⁾	R-0, HS, HC ARDY28 ⁽¹⁾	R-0, HS, HC ARDY27 ⁽¹⁾	R-0, HS, HC ARDY26 ⁽¹⁾	R-0, HS, HC ARDY25 ⁽¹⁾	R-0, HS, HC ARDY24 ⁽¹⁾
23:16	R-0, HS, HC ARDY23 ⁽¹⁾	R-0, HS, HC ARDY22 ⁽¹⁾	R-0, HS, HC ARDY21 ⁽¹⁾	R-0, HS, HC ARDY20 ⁽¹⁾	R-0, HS, HC ARDY19 ⁽¹⁾	R-0, HS, HC ARDY18	R-0, HS, HC ARDY17	R-0, HS, HC ARDY16
15:8	R-0, HS, HC ARDY15	R-0, HS, HC ARDY14	R-0, HS, HC ARDY13	R-0, HS, HC ARDY12	R-0, HS, HC ARDY11	R-0, HS, HC ARDY10	R-0, HS, HC ARDY9	R-0, HS, HC ARDY8
7:0	R-0, HS, HC ARDY7	R-0, HS, HC ARDY6	R-0, HS, HC ARDY5	R-0, HS, HC ARDY4	R-0, HS, HC ARDY3	R-0, HS, HC ARDY2	R-0, HS, HC ARDY1	R-0, HS, HC ARDY0

Legend: HS = Hardware Set HC = Hardware Cleared
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **ARDY31:ARDY0:** Conversion Data Ready for Corresponding Analog Input Ready bits
1 = This bit is set when converted data is ready in the data register
0 = This bit is cleared when the associated data register is read

Note 1: This bit is not available on 64-pin devices.

REGISTER 28-13: ADCDSTAT2: ADC DATA READY STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	U-0 —	U-0 —	U-0 —	R-0, HS, HC ARDY44	R-0, HS, HC ARDY43	R-0, HS, HC ARDY42 ⁽²⁾	R-0, HS, HC ARDY41 ⁽²⁾	R-0, HS, HC ARDY40 ⁽²⁾
7:0	R-0, HS, HC ARDY39 ⁽²⁾	R-0, HS, HC ARDY38 ⁽²⁾	R-0, HS, HC ARDY37 ⁽²⁾	R-0, HS, HC ARDY36 ⁽²⁾	R-0, HS, HC ARDY35 ⁽²⁾	R-0, HS, HC ARDY34 ⁽¹⁾	R-0, HS, HC ARDY33 ⁽¹⁾	R-0, HS, HC ARDY32 ⁽¹⁾

Legend: HS = Hardware Set HC = Hardware Cleared
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'
bit 12-0 **ARDY44:ARDY32:** Conversion Data Ready for Corresponding Analog Input Ready bits
1 = This bit is set when converted data is ready in the data register
0 = This bit is cleared when the associated data register is read

Note 1: This bit is not available on 64-pin devices.

2: This bit is not available on 64-pin and 100-pin devices.

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REGISTER 28-34: ADCSYSCFG1: ADC SYSTEM CONFIGURATION REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R-y
	AN<31:23>							
23:16	R-y	R-y	R-y	R-y	R-y	R-1	R-1	R-1
	AN<23:16>							
15:8	R-1	R-1	R-1	R-1	R-1	R-1	R-1	R-1
	AN<15:8>							
7:0	R-1	R-1	R-1	R-1	R-1	R-1	R-1	R-1
	AN<7:0>							

Legend:

R = Readable bit

W = Writable bit

y = POR value is determined by the specific device

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **AN<31:0>**: ADC Analog Input bits

These bits reflect the system configuration and are updated during boot-up time. By reading these read-only bits, the user application can determine whether or not an analog input in the device is available.

AN<31:0>: Reflects the presence or absence of the respective analog input (AN31-AN0).

REGISTER 28-35: ADCSYSCFG2: ADC SYSTEM CONFIGURATION REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-1	R-1	R-y	R-y	R-y
	—	—	—	AN<44:40>				
7:0	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R-y
	AN<39:32>							

Legend:

R = Readable bit

W = Writable bit

y = POR value is determined by the specific device

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-13 **Unimplemented**: Read as '0'

bit 12-0 **AN<44:32>**: ADC Analog Input bits

These bits reflect the system configuration and are updated during boot-up time. By reading these read-only bits, the user application can determine whether or not an analog input in the device is available.

AN<63:32>: Reflects the presence or absence of the respective analog input (AN63-AN32).

30.1 Ethernet Control Registers

TABLE 30-5: ETHERNET CONTROLLER REGISTER SUMMARY

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	ETHCON1	31:16	PTV<15:0>																0000
		15:0	ON	—	SIDL	—	—	—	TXRTS	RXEN	AUTOFC	—	—	MANFC	—	—	—	BUFCDEC	0000
2010	ETHCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	RXBUFSZ<6:0>							—	—	—	—	0000
2020	ETHTXST	31:16	TXSTADDR<31:16>																0000
		15:0	TXSTADDR<15:2>													—	—	—	—
2030	ETHRXST	31:16	RXSTADDR<31:16>																0000
		15:0	RXSTADDR<15:2>													—	—	—	—
2040	ETHHT0	31:16	HT<31:0>																0000
		15:0																	0000
2050	ETHHT1	31:16	HT<63:32>																0000
		15:0																	0000
2060	ETHPMM0	31:16	PMM<31:0>																0000
		15:0																	0000
2070	ETHPMM1	31:16	PMM<63:32>																0000
		15:0																	0000
2080	ETHPMCS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PMCS<15:0>																0000
2090	ETHPMO	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PMO<15:0>																0000
20A0	ETHRXFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	HTEN	MPEN	—	NOTPM	PMMODE<3:0>				CRC ERREN	CRC OKEN	RUNT ERREN	RUNTEN	UCEN	NOT MEEN	MCEN	BCEN	0000
20B0	ETHRXWM	31:16	—	—	—	—	—	—	—	RXFWM<7:0>									0000
		15:0	—	—	—	—	—	—	—	RXEWM<7:0>									0000
20C0	ETHIEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	TX BUSEIE	RX BUSEIE	—	—	—	EW MARKIE	FW MARKIE	RX DONEIE	PK TPENDIE	RX ACTIE	—	TX DONEIE	TX ABORTIE	RX BUFNAIE	RX OVFLWIE	0000
20D0	ETHIRQ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	TXBUSE	RXBUSE	—	—	—	EWMARK	FWMARK	RXDONE	PKTPEND	RXACT	—	TXDONE	TXABORT	RXBUFNA	RXOVFLW	0000
20E0	ETHSTAT	31:16	—	—	—	—	—	—	—	BUFCNT<7:0>									0000
		15:0	—	—	—	—	—	—	—	BUSY	TXBUSY	RXBUSY	—	—	—	—	—	—	0000
2100	ETH RXOVFLOW	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RXOVFLWCNT<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

Note 2: Reset values default to the factory programmed value.

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TABLE 37-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Param.	Sym.	Characteristic	Min.	Typ.	Max.	Units	Conditions ⁽¹⁾
DO10	VOL	Output Low Voltage I/O Pins 4x Sink Driver Pins - RA3, RA9, RA10, RA14, RA15 RB0-RB2, RB4, RB6, RB7, RB11, RB13 RC12-RC15 RD0, RD6-RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8 RG15 RH0, RH1, RH4-RH6, RH8-RH13 RJ0-RJ2, RJ8, RJ9, RJ11	—	—	0.4	V	$I_{OL} \leq 10 \text{ mA}$, $V_{DD} = 3.3\text{V}$
		Output Low Voltage I/O Pins: 8x Sink Driver Pins - RA0-RA2, RA4, RA5 RB3, RB5, RB8-RB10, RB12, RB14, RB15 RC1-RC4 RD1-RD5, RD9, RD10, RD12, RD13, RD15 RE4-RE7 RF0, RF4, RF5, RF12, RF13 RG0, RG1, RG6-RG9 RH2, RH3, RH7, RH14, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	—	—	0.4	V	$I_{OL} \leq 15 \text{ mA}$, $V_{DD} = 3.3\text{V}$
		Output Low Voltage I/O Pins: 12x Sink Driver Pins - RA6, RA7 RE0-RE3 RF1 RG12-RG14	—	—	0.4	V	$I_{OL} \leq 20 \text{ mA}$, $V_{DD} = 3.3\text{V}$

Note 1: Parameters are characterized, but not tested.

38.0 EXTENDED TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MZ EF electrical characteristics for devices running up to 125°C. Additional information will be provided in future revisions of this document as it becomes available.

The specifications for Extended Temperature are identical to those shown in **37.0 “Electrical Characteristics”**, with the exception of the parameters listed in this chapter.

Parameters in this chapter begin with the letter “E”, which denotes Extended Temperature operation. For example, parameter DC28 in **37.0 “Electrical Characteristics”**, is the Extended Temperature operation equivalent for EDC28.

Absolute maximum ratings for the PIC32MZ EF devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

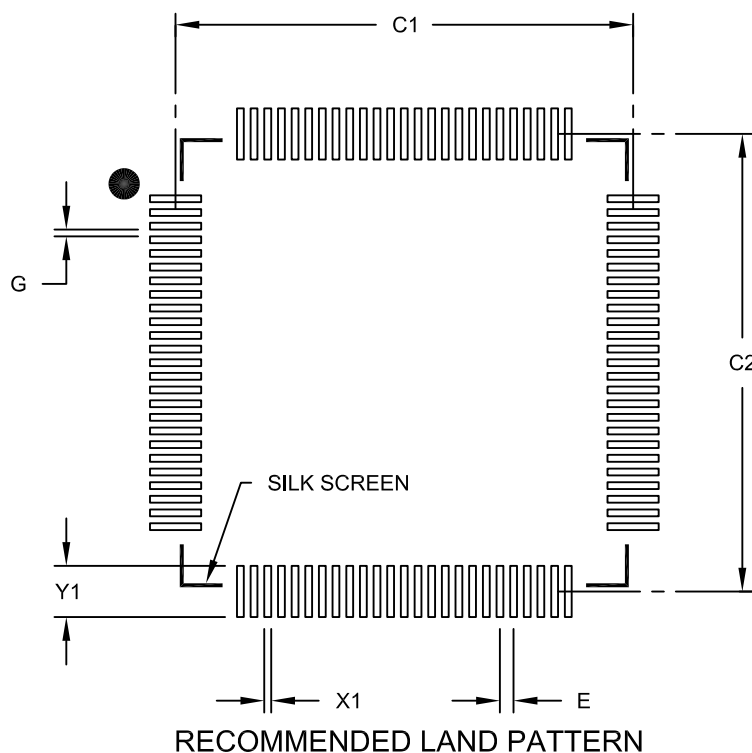
Ambient temperature under bias.....-40°C to +125°C

Note 1: Stresses above those listed under “**Absolute Maximum Ratings**” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

100-Lead Plastic Thin Quad Flatpack (PT)-12x12x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B