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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TFBGA
Supplier Device Package	144-TFBGA (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512efk144-e-jwx">https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512efk144-e-jwx</a>

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# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## 1.0 DEVICE OVERVIEW

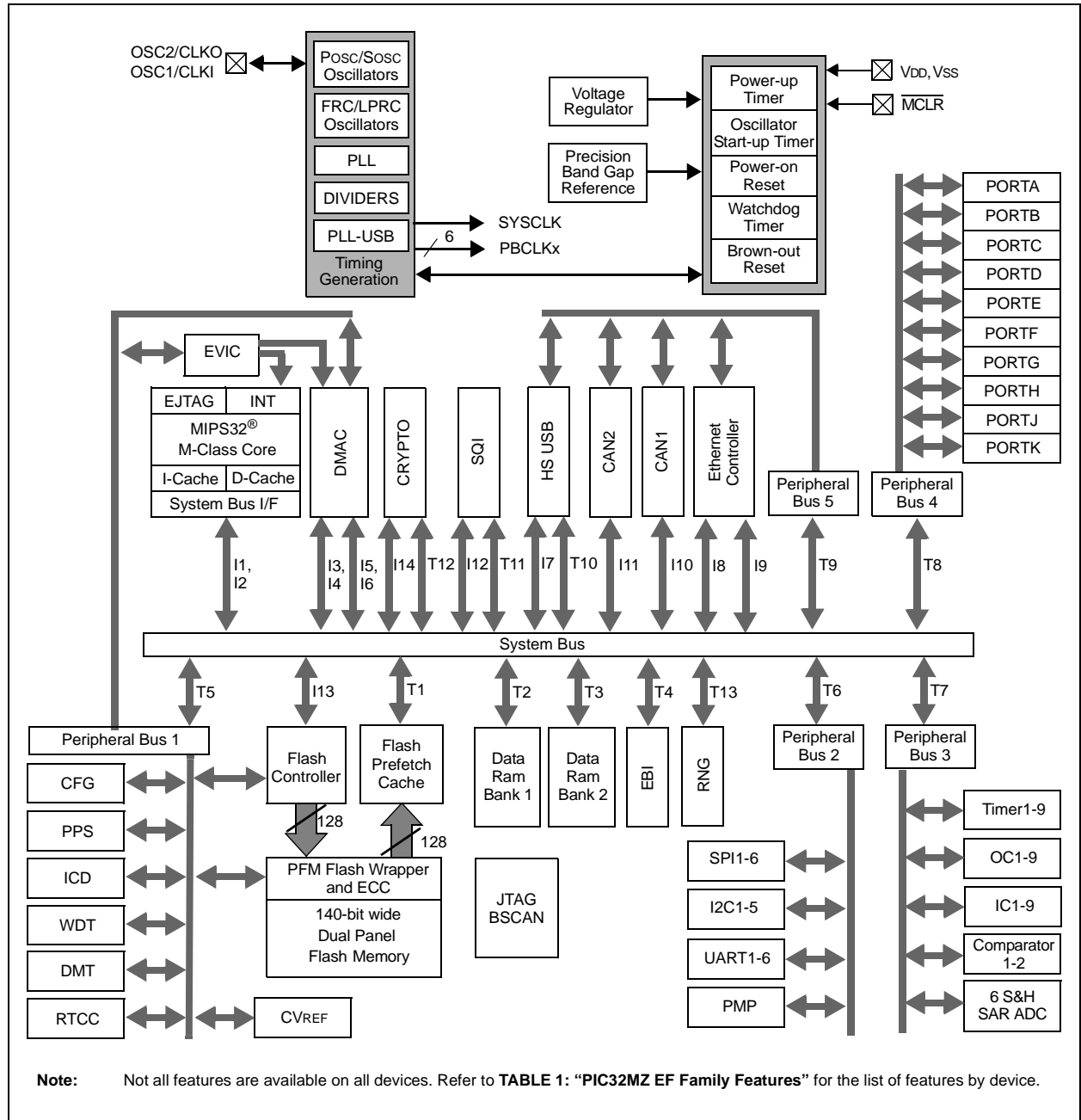
**Note:** This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “PIC32 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com/PIC32](http://www.microchip.com/PIC32)).

This data sheet contains device-specific information for PIC32MZ EF devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MZ EF family of devices.

Table 1-21 through Table 1-22 list the pinout I/O descriptions for the pins shown in the device pin tables (see Table 2 through Table 5).

**FIGURE 1-1: PIC32MZ EF FAMILY BLOCK DIAGRAM**



# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**TABLE 1-7: TIMER1 THROUGH TIMER9 AND RTCC PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Timer1 through Timer9							
T1CK	48	73	A49	106	I	ST	Timer1 External Clock Input
T2CK	PPS	PPS	PPS	PPS	I	ST	Timer2 External Clock Input
T3CK	PPS	PPS	PPS	PPS	I	ST	Timer3 External Clock Input
T4CK	PPS	PPS	PPS	PPS	I	ST	Timer4 External Clock Input
T5CK	PPS	PPS	PPS	PPS	I	ST	Timer5 External Clock Input
T6CK	PPS	PPS	PPS	PPS	I	ST	Timer6 External Clock Input
T7CK	PPS	PPS	PPS	PPS	I	ST	Timer7 External Clock Input
T8CK	PPS	PPS	PPS	PPS	I	ST	Timer8 External Clock Input
T9CK	PPS	PPS	PPS	PPS	I	ST	Timer9 External Clock Input
Real-Time Clock and Calendar							
RTCC	46	71	A48	104	O	—	Real-Time Clock Alarm/Seconds Output

**Legend:** CMOS = CMOS-compatible input or output      Analog = Analog input      P = Power  
ST = Schmitt Trigger input with CMOS levels      O = Output      I = Input  
TTL = Transistor-transistor Logic input buffer      PPS = Peripheral Pin Select

**TABLE 4-12: SYSTEM BUS TARGET 4 REGISTER MAP**

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9020	SBT4ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>				0000
9024	SBT4ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
9028	SBT4ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9030	SBT4ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9038	SBT4ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9040	SBT4REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9050	SBT4RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9058	SBT4WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9080	SBT4REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9090	SBT4RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9098	SBT4WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note:** For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

•

•

•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

•

•

•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

**Note:** This register represents a generic definition of the IPCx register. Refer to Table 7-2 for the exact bit definitions.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 8-5: REFOxTRIM: REFERENCE OSCILLATOR TRIM REGISTER ('x' = 1-4)**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROTRIM<8:1>								
23:16	R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	ROTRIM<0>	—	—	—	—	—	—	—
15:8	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-23 **ROTRIM<8:0>**: Reference Oscillator Trim bits

111111111 = 511/512 divisor added to RODIV value

111111110 = 510/512 divisor added to RODIV value

•

•

•

100000000 = 256/512 divisor added to RODIV value

•

•

•

000000010 = 2/512 divisor added to RODIV value

000000001 = 1/512 divisor added to RODIV value

000000000 = 0 divisor added to RODIV value

bit 22-0 **Unimplemented**: Read as '0'

- Note 1:** While the ON bit (REFOxCON<15>) is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.
- 2:** Do not write to this register when the ON bit (REFOxCON<15>) is not equal to the ACTIVE bit (REFOxCON<8>).
- 3:** Specified values in this register do not take effect if RODIV<14:0> (REFOxCON<30:16>) = 0.

**TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP**

Virtual Address (BF81_#)	Register Name <sup>(1)</sup>	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1060	DCH0CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1070	DCH0ECON	31:16	—	—	—	—	—	—	—	CHAIRQ<7:0>									00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1080	DCH0INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1090	DCH0SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
10A0	DCH0DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
10B0	DCH0SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSSIZ<15:0>																0000
10C0	DCH0DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDSIZ<15:0>																0000
10D0	DCH0SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSPTR<15:0>																0000
10E0	DCH0DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDPTR<15:0>																0000
10F0	DCH0CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCSIZ<15:0>																0000
1100	DCH0CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCPTR<15:0>																0000
1110	DCH0DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHPDAT<15:0>																0000
1120	DCH1CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	0000	
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1130	DCH1ECON	31:16	—	—	—	—	—	—	—	CHAIRQ<7:0>									00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1140	DCH1INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1150	DCH1SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
1160	DCH1DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.



## REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER (CONTINUED)

bit 0      **SESSION:** Active Session Control/Status bit

'A' device:

    1 = Start a session

    0 = End a session

'B' device:

    1 = (Read) Session has started or is in progress, (Write) Initiate the Session Request Protocol

    0 = When USB module is in Suspend mode, clearing this bit will cause a software disconnect

Clearing this bit when the USB module is not suspended will result in undefined behavior.

### REGISTER 11-29: USBLPMR2: USB LINK POWER MANAGEMENT CONTROL REGISTER 2 (CONTINUED)

bit 0     **LPMSTIF:** LPM STALL Interrupt Flag bit  
          When in *Device mode*:  
          1 = A LPM transaction was received and the USB Module responded with a STALL  
          0 = No Stall condition  
  
          When in *Host mode*:  
          1 = A LPM transaction was transmitted and the device responded with a STALL  
          0 = No Stall condition

## 12.4.3 CONTROLLING PPS

PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

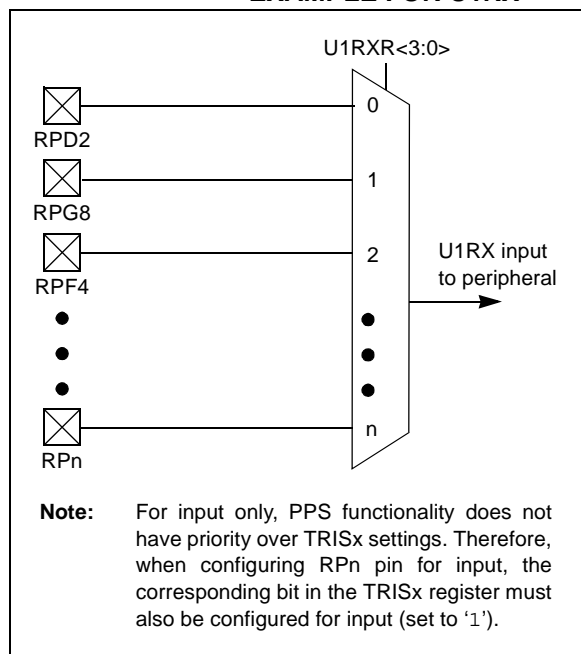
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

## 12.4.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The  $[pin\ name]R$  registers, where  $[pin\ name]$  refers to the peripheral pins listed in Table 12-2, are used to configure peripheral input mapping (see Register 12-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the  $RPn$  pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 12-2.

For example, Figure 12-2 illustrates the remappable pin selection for the U1RX input.

**FIGURE 12-2: REMAPPABLE INPUT EXAMPLE FOR U1RX**



## 14.0 TIMER2/3, TIMER4/5, TIMER6/7, AND TIMER8/9

**Note:** This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. “Timers”** (DS60001105) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com/PIC32](http://www.microchip.com/PIC32)).

The PIC32MZ EF family of devices features eight synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events.

The following modes are supported:

- Synchronous internal 16-bit timer
- Synchronous internal 16-bit gated timer
- Synchronous external 16-bit timer

Four 32-bit synchronous timers are available by combining Timer2 with Timer3, Timer4 with Timer5, Timer6 with Timer7, and Timer8 with Timer9.

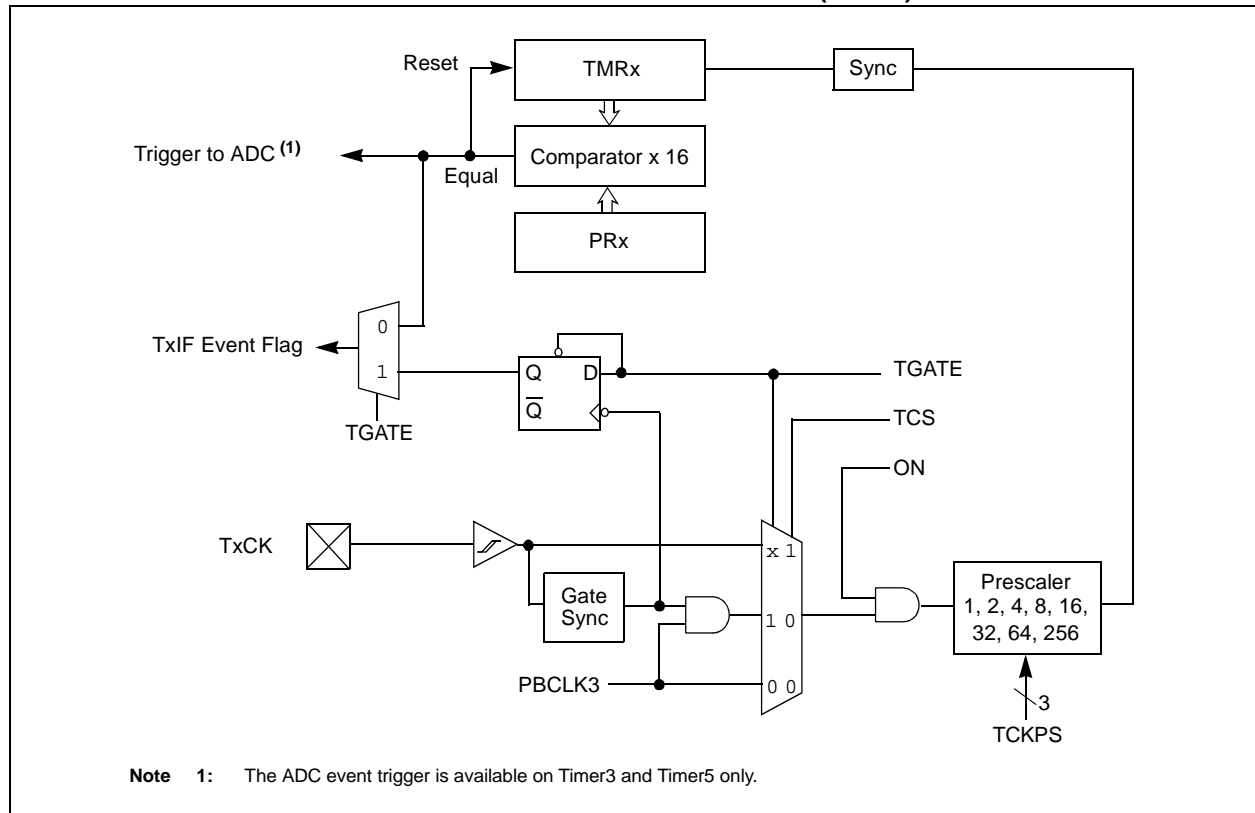
The 32-bit timers can operate in one of three modes:

- Synchronous internal 32-bit timer
- Synchronous internal 32-bit gated timer
- Synchronous external 32-bit timer

### 14.1 Additional Supported Features

- Selectable clock prescaler
- Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (Timer2 through Timer7 only)
- ADC event trigger (Timer3 and Timer5 only)
- Fast bit manipulation using CLR, SET, and INV registers

**FIGURE 14-1: TIMER2 THROUGH TIMER9 BLOCK DIAGRAM (16-BIT)**



# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

---

## REGISTER 23-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)

bit 5-2 **WAITM<3:0>**: Data Read/Write Strobe Wait States bits<sup>(1)</sup>

1111 = Wait of 16 TPBCLK2

•  
•  
•

0001 = Wait of 2 TPBCLK2

0000 = Wait of 1 TPBCLK2 (default)

bit 1-0 **WAITE<1:0>**: Data Hold After Read/Write Strobe Wait States bits<sup>(1)</sup>

11 = Wait of 4 TPBCLK2

10 = Wait of 3 TPBCLK2

01 = Wait of 2 TPBCLK2

00 = Wait of 1 TPBCLK2 (default)

For Read operations:

11 = Wait of 3 TPBCLK2

10 = Wait of 2 TPBCLK2

01 = Wait of 1 TPBCLK2

00 = Wait of 0 TPBCLK2 (default)

**Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK2 cycle for a write operation; WAITB = 1 TPBCLK2 cycle, WAITE = 0 TPBCLK2 cycles for a read operation.

**2:** Address bits 14 and 15 are not subject to auto-increment/decrement if configured as Chip Select.

**3:** The PMD<15:8> bits are not active if the MODE16 bit = 1.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 30-2: ETHCON2: ETHERNET CONTROLLER CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RXBUFSZ<6:4>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	RXBUFSZ<3:0>				—	—	—	—

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-4 **RXBUFSZ<6:0>:** RX Data Buffer Size for All RX Descriptors (in 16-byte increments) bits

1111111 = RX data Buffer size for descriptors is 2032 bytes

•  
•  
•

1100000 = RX data Buffer size for descriptors is 1536 bytes

•  
•  
•

0000011 = RX data Buffer size for descriptors is 48 bytes

0000010 = RX data Buffer size for descriptors is 32 bytes

0000001 = RX data Buffer size for descriptors is 16 bytes

0000000 = Reserved

bit 3-0 **Unimplemented:** Read as '0'

**Note 1:** This register is only used for RX operations.

**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 30-5: ETHHT0: ETHERNET CONTROLLER HASH TABLE 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HT<31:24>								
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HT<23:16>								
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HT<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HT<7:0>								

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **HT<31:0>**: Hash Table Bytes 0-3 bits

**Note 1:** This register is only used for RX operations.

**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the HTEN bit (ETHRXFC<15>) = 0.

## REGISTER 30-6: ETHHT1: ETHERNET CONTROLLER HASH TABLE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HT<63:56>								
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HT<55:48>								
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HT<47:40>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HT<39:32>								

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **HT<63:32>**: Hash Table Bytes 4-7 bits

**Note 1:** This register is only used for RX operations.

**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the HTEN bit (ETHRXFC<15>) = 0.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 30-9: ETHPMCS: ETHERNET CONTROLLER PATTERN MATCH CHECKSUM REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMCS<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMCS<7:0>							

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 31-16      **Unimplemented:** Read as '0'  
bit 15-8      **PMCS<15:8>:** Pattern Match Checksum 1 bits  
bit 7-0      **PMCS<7:0>:** Pattern Match Checksum 0 bits

**Note 1:** This register is only used for RX operations.  
**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

## REGISTER 30-10: ETHPMO: ETHERNET CONTROLLER PATTERN MATCH OFFSET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMO<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMO<7:0>							

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 31-16      **Unimplemented:** Read as '0'  
bit 15-0      **PMO<15:0>:** Pattern Match Offset 1 bits

**Note 1:** This register is only used for RX operations.  
**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.



# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 30-16: ETHRXOVFLOW: ETHERNET CONTROLLER RECEIVE OVERFLOW STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXOVFLWCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXOVFLWCNT<7:0>							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RXOVFLWCNT<15:0>:** Dropped Receive Frames Count bits

Increment counter for frames accepted by the RX filter and subsequently dropped due to internal receive error (RXFIFO overrun). This event also sets the RXOVFLW bit (ETHIRQ<0>) interrupt flag.

**Note 1:** This register is only used for RX operations.

**2:** This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

**3:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

### 36.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page ([www.microchip.com](http://www.microchip.com)) for the complete list of demonstration, development and evaluation kits.

### 36.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**TABLE 37-10: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS**

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param. No.	Symbol	Characteristics	Min.	Typical <sup>(1)</sup>	Max.	Units	Conditions
DI60a	I <sub>ICL</sub>	Input Low Injection Current	0	—	-5 <sup>(2,5)</sup>	mA	This parameter applies to all pins, with the exception of RB10. Maximum I <sub>ICH</sub> current for this exception is 0 mA.
DI60b	I <sub>ICH</sub>	Input High Injection Current	0	—	+5 <sup>(3,4,5)</sup>	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, OSCI, OSCO, SOSCI, SOSCO, D+, D- and RB10. Maximum I <sub>ICH</sub> current for these exceptions is 0 mA.
DI60c	$\Sigma I_{ICT}$	Total Input Injection Current (sum of all I/O and control pins)	-20 <sup>(6)</sup>	—	+20 <sup>(6)</sup>	mA	Absolute instantaneous sum of all $\pm$ input injection currents from all I/O pins ( $ I_{ICL}  +  I_{ICH}  $ ) $\leq \Sigma I_{ICT}$

- Note 1:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 2:** V<sub>IL</sub> source < (V<sub>SS</sub> - 0.3). Characterized but not tested.
- 3:** V<sub>IH</sub> source > (V<sub>DD</sub> + 0.3) for non-5V tolerant pins only.
- 4:** Digital 5V tolerant pins do not have an internal high side diode to V<sub>DD</sub>, and therefore, cannot tolerate any “positive” input injection current.
- 5:** Injection currents > |0| can affect the ADC results by approximately 4 to 6 counts (i.e., V<sub>IH</sub> Source > (V<sub>DD</sub> + 0.3) or V<sub>IL</sub> source < (V<sub>SS</sub> - 0.3)).
- 6:** Any number and/or combination of I/O pins not excluded under I<sub>ICL</sub> or I<sub>ICH</sub> conditions are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. If **Note 2**, I<sub>ICL</sub> = (((V<sub>SS</sub> - 0.3) - V<sub>IL</sub> source) / R<sub>S</sub>). If **Note 3**, I<sub>ICH</sub> = ((I<sub>CH</sub> source - (V<sub>DD</sub> + 0.3)) / R<sub>S</sub>). R<sub>S</sub> = Resistance between input source voltage and device pin. If (V<sub>SS</sub> - 0.3) ≤ V<sub>SOURCE</sub> ≤ (V<sub>DD</sub> + 0.3), injection current = 0.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**TABLE 37-23: I/O TIMING REQUIREMENTS (CONTINUED)**

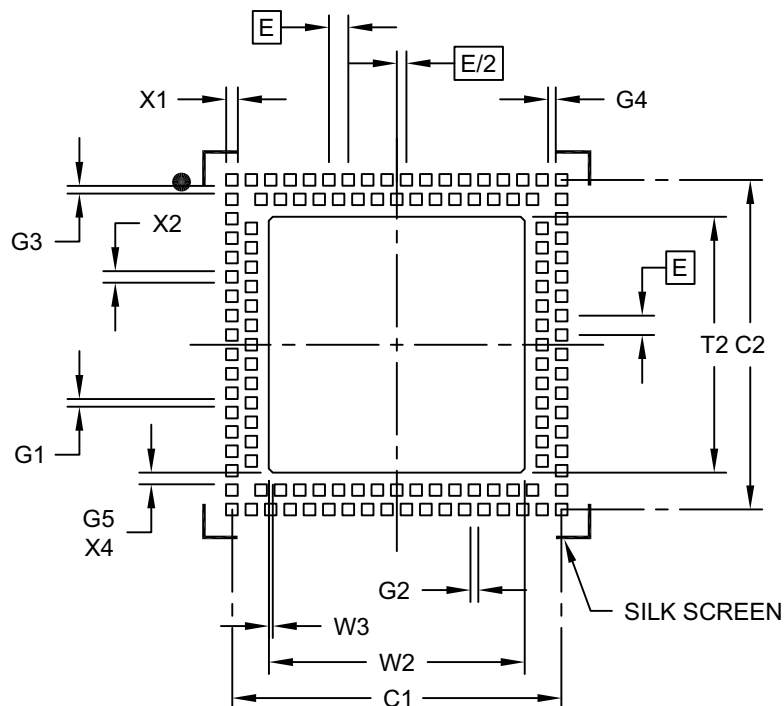
AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param. No.	Symbol	Characteristics <sup>(2)</sup>	Min.	Typ. <sup>(1)</sup>	Max.	Units	Conditions
DO32	TioF	<b>Port Output Fall Time</b> I/O Pins: 4x Source Driver Pins - RA3, RA9, RA10, RA14, RA15 RB0-RB2, RB4, RB6-RB7, RB11, RB13 RC12-RC15 RD0, RD6-RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8 RG15 RH0, RH1, RH4-RH6, RH8-RH13 RJ0-RJ2, RJ8, RJ9, RJ11	—	—	9.5	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		<b>Port Output Fall Time</b> I/O Pins: 8x Source Driver Pins - RA0-RA2, RA4, RA5 RB3, RB5, RB8-RB10, RB12, RB14, RB15 RC1-RC4 RD1-RD5, RD9, RD10, RD12, RD13, RD15 RE4-RE7 RF0, RF4, RF5, RF12, RF13 RG0, RG1, RG6-RG9 RH2, RH3, RH7, RH14, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	—	—	8	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		<b>Port Output Fall Time</b> I/O Pins: 12x Source Driver Pins - RA6, RA7 RE0-RE3 RF1 RG12-RG14	—	—	3.5	ns	CLOAD = 50 pF
			—	—	2	ns	CLOAD = 20 pF
DI35	TINP	INTx Pin High or Low Time	5	—	—	ns	—
DI40	TRBP	CNx High or Low Time (input)	5	—	—	ns	—

**Note 1:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**2:** This parameter is characterized, but not tested in manufacturing.

## 124-Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Pad Clearance	G1	0.20		
Pad Clearance	G2	0.20		
Pad Clearance	G3	0.20		
Pad Clearance	G4	0.20		
Contact to Center Pad Clearance (X4)	G5	0.30		
Optional Center Pad Width	T2			6.60
Optional Center Pad Length	W2			6.60
Optional Center Pad Chamfer (X4)	W3		0.10	
Contact Pad Spacing	C1		8.50	
Contact Pad Spacing	C2		8.50	
Contact Pad Width (X124)	X1			0.30
Contact Pad Length (X124)	X2			0.30

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2193A