Microchip Technology - PIC32MZ0512EFK144-I/PL Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512efk144-i-pl

TABLE 3-3: COPROCESSOR 0 REGISTERS (CONTINUED)

Register Number	Register Name	Function
12	Status	Processor status and control.
	IntCtl	Interrupt control of vector spacing.
	SRSCtl	Shadow register set control.
	SRSMap	Shadow register mapping control.
	View_IPL	Allows the Priority Level to be read/written without extracting or inserting that bit from/to the Status register.
	SRSMAP2	Contains two 4-bit fields that provide the mapping from a vector number to the shadow set number to use when servicing such an interrupt.
13	Cause	Describes the cause of the last exception.
	NestedExc	Contains the error and exception level status bit values that existed prior to the current exception.
	View_RIPL	Enables read access to the RIPL bit that is available in the Cause register.
14	EPC	Program counter at last exception.
	NestedEPC	Contains the exception program counter that existed prior to the current exception.
15	PRID	Processor identification and revision
	Ebase	Exception base address of exception vectors.
	CDMMBase	Common device memory map base.
16	Config	Configuration register.
	Config1	Configuration register 1.
	Config2	Configuration register 2.
	Config3	Configuration register 3.
	Config4	Configuration register 4.
	Config5	Configuration register 5.
	Config7	Configuration register 7.
17	LLAddr	Load link address (MPU only).
18	WatchLo	Low-order watchpoint address (MPU only).
19	WatchHi	High-order watchpoint address (MPU only).
20-22	Reserved	Reserved in the PIC32 core.
23	Debug	EJTAG debug register.
	TraceControl	EJTAG trace control.
	TraceControl2	EJTAG trace control 2.
	UserTraceData1	EJTAG user trace data 1 register.
	TraceBPC	EJTAG trace breakpoint register.
	Debug2	Debug control/exception status 1.
24	DEPC	Program counter at last debug exception.
	UserTraceData2	EJTAG user trace data 2 register.
25	PerfCtl0	Performance counter 0 control.
	PerfCnt0	Performance counter 0.
	PerfCtl1	Performance counter 1 control.
	PerfCnt1	Performance counter 1.
26	ErrCtl	Software test enable of way-select and data RAM arrays for I-Cache and D-Cache (MPU only).
27	Reserved	Reserved in the PIC32 core.
28	TagLo/DataLo	Low-order portion of cache tag interface (MPU only).
29	Reserved	Reserved in the PIC32 core.
30	ErrorEPC	Program counter at last error exception.
31	DeSave	Debug exception save.

TABLE 4-18: SYSTEM BUS TARGET 10 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A820	SBT10ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
A824	SBT10ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
A828	SBT10ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
A830	SBT10ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A838	SBT10ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A840	SBT10REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
A850	SBT10RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A858	SBT10WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

REGISTER 5-8: NVMBWP: FLASH BOOT (PAGE) WRITE-PROTECT REGISTER

bit 4 **UBWP4:** Upper Boot Alias Page 4 Write-protect bit(1)
1 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF enabled
0 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF disabled

bit 3 **UBWP3:** Upper Boot Alias Page 3 Write-protect bit(1)
1 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF enabled
0 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF disabled

bit 2 **UBWP2:** Upper Boot Alias Page 2 Write-protect bit(1)
1 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF enabled
0 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF disabled

bit 1 **UBWP1:** Upper Boot Alias Page 1 Write-protect bit(1)
1 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF enabled
0 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF disabled

bit 0 **UBWP0:** Upper Boot Alias Page 0 Write-protect bit(1)
1 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF enabled
0 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF disabled

Note 1: These bits are only available when the NVMKEY unlock sequence is performed and the associated Lock bit (LBWPULOCK or UBWPULOCK) is set.

Note:	The bits in this register are only writable when the NVMKEY unlock sequence is followed.

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER (CONTINUED)

bit 15-12 **PRI3SS<3:0>:** Interrupt with Priority Level 3 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 3 uses Shadow Set 0)
0111 = Interrupt with a priority level of 3 uses Shadow Set 7
0110 = Interrupt with a priority level of 3 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 3 uses Shadow Set 1
0000 = Interrupt with a priority level of 3 uses Shadow Set 0

bit 11-8 **PRI2SS<3:0>:** Interrupt with Priority Level 2 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 2 uses Shadow Set 0)
0111 = Interrupt with a priority level of 2 uses Shadow Set 7
0110 = Interrupt with a priority level of 2 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 2 uses Shadow Set 1
0000 = Interrupt with a priority level of 2 uses Shadow Set 0

bit 7-4 **PRI1SS<3:0>:** Interrupt with Priority Level 1 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 1 uses Shadow Set 0)
0111 = Interrupt with a priority level of 1 uses Shadow Set 7
0110 = Interrupt with a priority level of 1 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 1 uses Shadow Set 1
0000 = Interrupt with a priority level of 1 uses Shadow Set 0

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **SS0:** Single Vector Shadow Register Set bit
1 = Single vector is presented with a shadow set
0 = Single vector is not presented with a shadow set

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1280	DCH2CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1290	DCH2DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
12A0	DCH3CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
12B0	DCH3ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
12C0	DCH3INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
12D0	DCH3SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
12E0	DCH3DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
12F0	DCH3SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1300	DCH3DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1310	DCH3SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1320	DCH3DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1330	DCH3CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1340	DCH3CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1350	DCH3DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
1360	DCH4CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1370	DCH4ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1380	DCH4INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1390	DCH4SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
13A0	DCH4DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
13B0	DCH4SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
13C0	DCH4DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
13D0	DCH4SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
13E0	DCH4DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
13F0	DCH4CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1400	DCH4CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1410	DCH4DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
1420	DCH5CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1430	DCH5ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1440	DCH5INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1450	DCH5SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
1460	DCH5DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
1470	DCH5SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1480	DCH5DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1490	DCH5SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
15B0	DCH7ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
15C0	DCH7INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
15D0	DCH7SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
15E0	DCH7DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
15F0	DCH7SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1600	DCH7DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1610	DCH7SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1620	DCH7DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1630	DCH7CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1640	DCH7CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1650	DCH7DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

11.1 USB OTG Control Registers

TABLE 11-1: USB REGISTER MAP 1

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	USBCSR0	31:16	—	—	—	—	—	—	—	—	EP7TXIF	EP6TXIF	EP5TXIF	EP4TXIF	EP3TXIF	EP2TXIF	EP1TXIF	EP0IF	0000
		15:0	ISOUPD(1)	SOFT CONN(1)	HSEN	HSMODE	RESET	RESUME	SUSP MODE	SUSPEN	—	FUNC<6:0>(1)							2000
			—(2)	—(2)								—(2)	—(2)	—(2)	—(2)	—(2)	—(2)	—(2)	
3004	USBCSR1	31:16	—	—	—	—	—	—	—	—	EP7TXIE	EP6TXIE	EP5TXIE	EP4TXIE	EP3TXIE	EP2TXIE	EP1TXIE	EP0IE	00FF
		15:0	—	—	—	—	—	—	—	—	EP7RXIF	EP6RXIF	EP5RXIF	EP4RXIF	EP3RXIF	EP2RXIF	EP1RXIF	—	0000
3008	USBCSR2	31:16	VBUSERRIE	SESSRQIE	DISCONIE	CONNIE	SOFIE	RESETIE	RESUMEIE	SUSPIE	VBUSERRIF	SESSREQIF	DISCONIF	CONNIF	SOFIF	RESETIF	RESUMEIF	SUSPIF	0600
		15:0	—	—	—	—	—	—	—	—	EP7RXIE	EP6RXIE	EP5RXIE	EP4RXIE	EP3RXIE	EP2RXIE	EP1RXIE	—	00FE
300C	USBCSR3	31:16	FORCEHST	FIFOACC	FORCEFS	FORCEHS	PACKET	TESTK	TESTJ	NAK	—	—	—	—	ENDPOINT<3:0>				0000
		15:0	—	—	—	—	—	RFRMNUM<10:0>											0000
3010	USB IE0CSR0(3)	31:16	—	—	—	—	—(1)	—(1)	—(1)	FLSHFIFO	SVC SETEND(1)	SVCRPR(1)	SEND STALL(1)	SETUP END(1)	DATAEND(1)	SENT STALL(1)	TXPKT RDY	RXPKT RDY	0000
							DISPING(2)	DTWREN(2)	DATA TGGL(2)		NAK TMOUT(2)	STATPKT(2)	REQPKT(2)	ERROR(2)	SETUP PKT(2)	RXSTALL(2)			0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
3018	USB IE0CSR2(3)	31:16	—	—	—	NAKLIM<4:0>(2)					SPEED<1:0>(2)		—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	RXCNT<6:0>							0000
301C	USB IE0CSR3(3)	31:16	MPRXEN	MPTXEN	BIGEND	HBRXEN	HBTXEN	DYNFIFOS	SOFTCONE	UTMIDWID	—	—	—	—	—	—	—	—	xx00
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
3010	USB IENCSR0(4)	31:16	AUTOSET	ISO(1)	MODE	DMA REQEN	FRC DATTG	DMA REQMD	—(1)	—(1)	INCOMP TX(1)	CLRDT	SENT STALL(1)	SEND STALL(1)	FLUSH	UNDER RUN(1)	FIFONE	TXPKT RDY	0000
				—					DTWREN(2)	DATA TGGL(2)	NAK TMOUT(2)		RXSTALL(2)	SETUPPKT(2)		ERROR(2)			0000
		15:0	MULT<4:0>					TXMAXP<10:0>											0000
3014	USB IENCSR1(4)	31:16	AUTOCLR	ISO(1)	DMA REQEN	DISNYET(1)	DMA REQMD	—(1)	—(1)	INCOM PRX	CLRDT	SENTSTALL(1)	SENDSTALL(1)	FLUSH	DATAERR(1)	OVERRUN(1)	FIFOFULL	RXPKT RDY	0000
				AUTORQ(2)		PIDERR(2)		DATA TWEN(2)	DATA TGGL(2)			RXSTALL(2)	REQPKT(2)		DERR-NAKT(1)	ERROR(2)			0000
		15:0	MULT<4:0>					RXMAXP<10:0>											0000
3018	USB IENCSR2(4)	31:16	TXINTERV<7:0>(2)								SPEED<1:0>(2)		PROTOCOL<1:0>		TEP<3:0>				0000
		15:0	—	—	RXCNT<13:0>														0000
301C	USB IENCSR3(1,3)	31:16	RXFIFOSZ<3:0>				TXFIFOSZ<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	RXINTERV<7:0>								SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>				0000
3020	USB FIFO0	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3024	USB FIFO1	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

REGISTER 12-3: CNCONx: CHANGE NOTICE CONTROL FOR PORTx REGISTER (x = A – K)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	ON	—	—	—	EDGEDETECT	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notice (CN) Control ON bit
1 = CN is enabled
0 = CN is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **EDGEDETECT:** Change Notification Style bit
1 = Edge Style. Detect edge transitions (CNFx used for CN Event).
0 = Mismatch Style. Detect change from last PORTx read (CNSTATx used for CN Event).

bit 10-0 **Unimplemented:** Read as '0'

TABLE 14-1: TIMER2 THROUGH TIMER9 REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0C10	TMR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR7<15:0>																0000
0C20	PR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR7<15:0>																FFFF
0E00	T8CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0E10	TMR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR8<15:0>																0000
0E20	PR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR8<15:0>																FFFF
1000	T9CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
1010	TMR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR9<15:0>																0000
1020	PR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR9<15:0>																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

The timer source for each Input Capture module depends on the setting of the ICACLK bit in the CFGCON register. The available configurations are shown in Table 17-1.

TABLE 17-1: TIMER SOURCE CONFIGURATIONS

Input Capture Module	Timerx	Timery
ICACLK (CFGCON<17>) = 0		
IC1 • • • IC9	Timer2 • • • Timer2	Timer3 • • • Timer3
ICACLK (CFGCON<17>) = 1		
IC1	Timer4	Timer5
IC2	Timer4	Timer5
IC3	Timer4	Timer5
IC4	Timer2	Timer3
IC5	Timer2	Timer3
IC6	Timer2	Timer3
IC7	Timer6	Timer7
IC8	Timer6	Timer7
IC9	Timer6	Timer7

23.1 PMP Control Registers

TABLE 23-1: PARALLEL MASTER PORT REGISTER MAP

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
E000	PMCON	31:16	—	—	—	—	—	—	—	—	RDSTART	—	—	—	—	—	DUALBUF	—	0000
		15:0	ON	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN	CSF<1:0>		ALP	CS2P	CS1P	—	WRSP	RDSP	0000
E010	PMMODE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>		WAITB<1:0>		WAITM<3:0>				WAITE<1:0>		0000
E020	PMADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CS2	CS1	ADDR<13:0>														0000
			ADDR15	ADDR14															0000
E030	PMDOUT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DATAOUT<15:0>																0000
E040	PMDIN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DATAIN<15:0>																0000
E050	PMAEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PTEN<15:0>																0000
E060	PMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F
E070	PMWADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WCS2	WCS1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
			WADDR15	WADDR14	WADDR<13:0>														0000
E080	PMRADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RCS2	RCS1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
			RADDR15	RADDR14	RADDR<13:0>														0000
E090	PMRDIN	31:16	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	15:0	RDATAIN<15:0>															0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

26.2 Crypto Engine Buffer Descriptors

Host software creates a linked list of buffer descriptors and the hardware updates them. Table 26-3 provides a list of the Crypto Engine buffer descriptors, followed by format descriptions of each buffer descriptor (see Figure 26-2 through Figure 26-9).

TABLE 26-3: CRYPTO ENGINE BUFFER DESCRIPTORS

Name (see Note 1)		Bit 31/2315/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
BD_CTRL	31:24	DESC_EN	—	CRY_MODE<2:0>			—	—	—
	23:16	—	SA_FETCH_EN	—	—	LAST_BD	LIFM	PKT_INT_EN	CBD_INT_EN
	15:8	BD_BUFLEN<15:8>							
	7:0	BD_BUFLEN<7:0>							
BD_SA_ADDR	31:24	BD_SAADDR<31:24>							
	23:16	BD_SAADDR<23:16>							
	15:8	BD_SAADDR<15:8>							
	7:0	BD_SAADR<7:0>							
BD_SCRADDR	31:24	BD_SRCADDR<31:24>							
	23:16	BD_SRCADDR<23:16>							
	15:8	BD_SRCADDR<15:8>							
	7:0	BD_SRCADDR<7:0>							
BD_DSTADDR	31:24	BD_DSTADDR<31:24>							
	23:16	BD_DSTADDR<23:16>							
	15:8	BD_DSTADDR<15:8>							
	7:0	BD_DSTADDR<7:0>							
BD_NXTPTR	31:24	BD_NXTADDR<31:24>							
	23:16	BD_NXTADDR<23:16>							
	15:8	BD_NXTADDR<15:8>							
	7:0	BD_NXTADDR<7:0>							
BD_UPDPTR	31:24	BD_UPDADDR<31:24>							
	23:16	BD_UPDADDR<23:16>							
	15:8	BD_UPDADDR<15:8>							
	7:0	BD_UPDADDR<7:0>							
BD_MSG_LEN	31:24	MSG_LENGTH<31:24>							
	23:16	MSG_LENGTH<23:16>							
	15:8	MSG_LENGTH<15:8>							
	7:0	MSG_LENGTH<7:0>							
BD_ENC_OFF	31:24	ENCR_OFFSET<31:24>							
	23:16	ENCR_OFFSET<23:16>							
	15:8	ENCR_OFFSET<15:8>							
	7:0	ENCR_OFFSET<7:0>							

Note 1: The buffer descriptor must be allocated in memory on a 64-bit boundary.

REGISTER 34-7: CFGCON: CONFIGURATION CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DMAPRI(1)	CPUPRI(1)
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	ICACLK(1)	OCACLK(1)
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	IOLOCK(1)	PMDLOCK(1)	PGLOCK(1)	—	—	USBSSEN(1)
7:0	R/W-0	U-0	R/W-1	R/W-1	R/W-1	R/W-0	U-0	R/W-1
	IOANCPEN	—	ECCCON<1:0>		JTAGEN	TROEN	—	TDOEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **DMAPRI:** DMA Read and DMA Write Arbitration Priority to SRAM bit(1)
- 1 = DMA gets High Priority access to SRAM
- 0 = DMA uses Least Recently Serviced Arbitration (same as other initiators)

bit 24 **CPUPRI:** CPU Arbitration Priority to SRAM When Servicing an Interrupt bit(1)
- 1 = CPU gets High Priority access to SRAM
- 0 = CPU uses Least Recently Serviced Arbitration (same as other initiators)

bit 23-18 **Unimplemented:** Read as '0'

bit 17 **ICACLK:** Input Capture Alternate Clock Selection bit(1)
- 1 = Input Capture modules use an alternative Timer pair as their timebase clock
- 0 = All Input Capture modules use Timer2/3 as their timebase clock

bit 16 **OCACLK:** Output Compare Alternate Clock Selection bit(1)
- 1 = Output Compare modules use an alternative Timer pair as their timebase clock
- 0 = All Output Compare modules use Timer2/3 as their timebase clock

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **IOLOCK:** Peripheral Pin Select Lock bit(1)
- 1 = Peripheral Pin Select is locked. Writes to PPS registers are not allowed
- 0 = Peripheral Pin Select is not locked. Writes to PPS registers are allowed

bit 12 **PMDLOCK:** Peripheral Module Disable bit(1)
- 1 = Peripheral module is locked. Writes to PMD registers are not allowed
- 0 = Peripheral module is not locked. Writes to PMD registers are allowed

bit 11 **PGLOCK:** Permission Group Lock bit(1)
- 1 = Permission Group registers are locked. Writes to PG registers are not allowed
- 0 = Permission Group registers are not locked. Writes to PG registers are allowed

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **USBSSEN:** USB Suspend Sleep Enable bit(1)

Enables features for USB PHY clock shutdown in Sleep mode.
- 1 = USB PHY clock is shut down when Sleep mode is active
- 0 = USB PHY clock continues to run when Sleep is active

Note 1: To change this bit, the unlock sequence must be performed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

36.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

36.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

37.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MZ EF electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MZ EF devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Specifications for Extended Temperature devices (-40ºC to +125ºC) that are different from the specifications in this section are provided in **38.0 "Extended Temperature Electrical Characteristics"**.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias ..... -40°C to +85°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to V_{SS} **(Note 3)** ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 2.1V$ **(Note 3)** ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} < 2.1V$ **(Note 3)** ..... -0.3V to +3.6V
Voltage on D+ or D- pin with respect to V_{USB3V3} ..... -0.3V to (V_{USB3V3} + 0.3V)
Voltage on V_{BUS} with respect to V_{SS} ..... -0.3V to +5.5V
Maximum current out of V_{SS} pin(s) ..... 200 mA
Maximum current into V_{DD} pin(s) **(Note 2)** ..... 200 mA
Maximum current sunk/sourced by any 4x I/O pin **(Note 4)** ..... 15 mA
Maximum current sunk/sourced by any 8x I/O pin **(Note 4)** ..... 25 mA
Maximum current sunk/sourced by any 12x I/O pin **(Note 4)** ..... 33 mA
Maximum current sunk by all ports ..... 150 mA
Maximum current sourced by all ports **(Note 2)** ..... 150 mA

Note 1: Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 37-2).

3: See the pin name tables (Table 2 through Table 4) for the 5V tolerant pins.

4: Characterized, but not tested. Refer to parameters DO10, DO20, and DO20a for the 4x, 8x, and 12x I/O pin lists.

38.0 EXTENDED TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MZ EF electrical characteristics for devices running up to 125ºC. Additional information will be provided in future revisions of this document as it becomes available.

The specifications for Extended Temperature are identical to those shown in **37.0 "Electrical Characteristics"**, with the exception of the parameters listed in this chapter.

Parameters in this chapter begin with the letter "E", which denotes Extended Temperature operation. For example, parameter DC28 in **37.0 "Electrical Characteristics"**, is the Extended Temperature operation equivalent for EDC28.

Absolute maximum ratings for the PIC32MZ EF devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

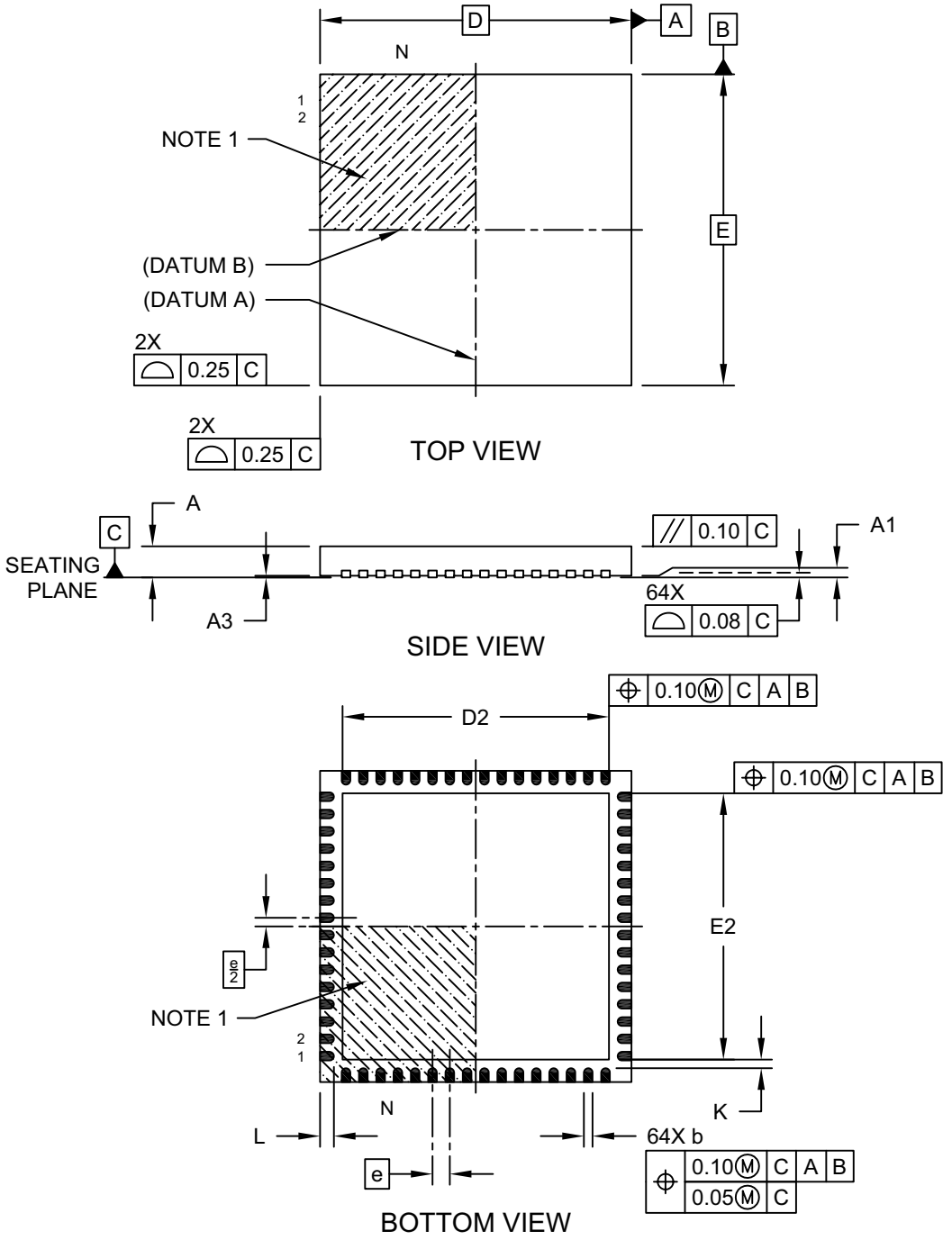
(See Note 1)

Ambient temperature under bias.....-40°C to +125°C

Note	**1:**	Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 7.70 x 7.70 Exposed Pad [QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-213B Sheet 1 of 2

APPENDIX A: MIGRATING FROM PIC32MX5XX/6XX/7XX TO PIC32MZ EF

This appendix provides an overview of considerations for migrating from PIC32MX5XX/6XX/7XX devices to the PIC32MZ EF family of devices. The code developed for PIC32MX5XX/6XX/7XX devices can be ported to PIC32MZ EF devices after making the appropriate changes outlined in the following sections.

The PIC32MZ EF devices are based on a new architecture, and feature many improvements and new capabilities over PIC32MX5XX/6XX/7XX devices.

A.1 Oscillator and PLL Configuration

Because the maximum speed of the PIC32MZ EF family is greater, the configuration of the oscillator is different from prior PIC32MX5XX/6XX/7XX devices.

Table A-1 summarizes the differences (indicated by **Bold** type) between the family devices for the oscillator.

TABLE A-1: OSCILLATOR CONFIGURATION DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Primary Oscillator Configuration	
On PIC32MX devices, XT mode had to be selected if the input frequency was in the 3 MHz to 10 MHz range (4-10 for PLL), and HS mode had to be selected if the input frequency was in the 10 MHz to 20 MHz range.	On PIC32MZ EF devices, HS mode has a wider input frequency range (4 MHz to 12 MHz). The bit setting of '01' is Reserved.
POSCMOD<1:0> (DEVCFG1<9:8>) 11 = Primary Oscillator disabled 10 = HS Oscillator mode selected **01 = XT Oscillator mode selected** 00 = External Clock mode selected	POSCMOD<1:0> (DEVCFG1<9:8>) 11 = Primary Oscillator disabled 10 = HS Oscillator mode selected **01 = Reserved** 00 = External Clock mode selected
On PIC32MX devices, crystal mode could be selected with the HS or XT POSC setting, but an external oscillator could be fed into the OSC1/CLKI pin and the part would operate normally.	On PIC32MZ devices, this option is not available. External oscillator signals should only be fed into the OSC1/CLKI pin with the POSC set to EC mode.
Oscillator Selection	
On PIC32MX devices, clock selection choices are as follows:	On PIC32MZ EF devices, clock selection choices are as follows:
FNOSC<2:0> (DEVCFG1<2:0>) NOSC<2:0> (OSCCON<10:8>) 111 = FRCDIV **110 = FRCDIV16** 101 = LPRC 100 = SOSC **011 = POSC with PLL module** 010 = POSC (XT, HS, EC) **001 = FRCDIV+PLL** **000 = FRC**	FNOSC<2:0> (DEVCFG1<2:0>) NOSC<2:0> (OSCCON<10:8>) 111 = FRCDIV **110 = Reserved** 101 = LPRC 100 = SOSC **011 = Reserved** 010 = POSC (HS or EC) **001 = System PLL (SPLL)** **000 = FRCDIV**
COSC<2:0> (OSCCON<14:12>) 111 = FRC divided by FRCDIV **110 = FRC divided by 16** 101 = LPRC 100 = SOSC **011 = POSC + PLL module** 010 = POSC **001 = FRCPLL** **000 = FRC**	COSC<2:0> (OSCCON<14:12>) 111 = FRC divided by FRCDIV **110 = BFRC** 101 = LPRC 100 = SOSC **011 = Reserved** 010 = POSC **001 = System PLL** **000 = FRC divided by FRCDIV**

A.8 Flash Programming

The PIC32MZ EF family of devices incorporates a new Flash memory technology. Applications ported from PIC32MX5XX/6XX/7XX devices that take advantage of Run-time Self Programming will need to adjust the Flash programming steps to incorporate these changes.

Table A-9 lists the differences (indicated by **Bold** type) that will affect software migration.

TABLE A-9: FLASH PROGRAMMING DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Program Flash Write Protection	
On PIC32MX devices, the Program Flash write-protect bits are part of the Flash Configuration words (DEVCFG0). PWP<**7**:0> (**DEVCFG0<19:12>**) 11111111 = Disabled 11111110 = 0xBD000FFF 11111101 = 0xBD001FFF 11111100 = 0xBD002FFF 11111011 = 0xBD003FFF 11111010 = 0xBD004FFF 11111001 = 0xBD005FFF 11111000 = 0xBD006FFF 11110111 = 0xBD007FFF 11110110 = 0xBD008FFF 11110101 = 0xBD009FFF 11110100 = 0xBD00AFFF 11110011 = 0xBD00BFFF 11110010 = 0xBD00CFFF 11110001 = 0xBD00DFFF 11110000 = 0xBD00EFFF 11101111 = 0xBD00FFFF • • • 01111111 = 0xBD07FFFF	On PIC32MZ EF devices, the write-protect register is contained separately as the NVMPWP register. It has been expanded to 24 bits, and now represents the address below, which all Flash memory is protected. Note that the lower 14 bits are forced to zero, so that all memory locations in the page are protected. PWP<**23**:0> (**NVMPWP<23:0>**) Physical memory below address 0x1Dxxxxxx is write protected, where 'xxxxxx' is specified by PWP<23:0>. When PWP<23:0> has a value of '0', write protection is disabled for the entire program Flash. If the specified address falls within the page, the entire page and all pages below the current page will be protected.
Code Protection	
On PIC32MX devices, code protection is enabled by the CP (**DEVCFG**<28>) bit.	On PIC32MZ EF devices, code protection is enabled by the CP (**DEVCP0**<28>) bit.
Boot Flash Write Protection	
On PIC32MX devices, Boot Flash write protection is enable by the **BWP (DEVCFG<24>)** bit and protects the entire Boot Flash memory.	On PIC32MZ EF devices, Boot Flash write protection is divided into pages and is enable by the **LBWPx** and **UBWPx** bits in the **NVMBWP** register.
Low-Voltage Detect Status	
LVDSTAT (NVMCON<11>) 1 = Low-voltage event is active 0 = Low-voltage event is not active	The LVDSTAT bit is not available in PIC32MZ EF devices.