Microchip Technology - PIC32MZ0512EFK144T-I/PL Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz0512efk144t-i-pl

TABLE 5: PIN NAMES FOR 144-PIN DEVICES

144-PIN LQFP AND TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)144
PIC32MZ1024EF(G/H/M)144
PIC32MZ1024EF(E/F/K)144
PIC32MZ2048EF(G/H/M)144

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Pin Number	Full Pin Name	Pin Number	Full Pin Name
1	AN23/RG15	37	PGEC2/AN46/RPB6/RB6
2	EBIA5/AN34/PMA5/RA5	38	PGED2/AN47/RPB7/RB7
3	EBID5/AN17/RPE5/PMD5/RE5	39	VREF-/CVREF-/AN27/RA9
4	EBID6/AN16/PMD6/RE6	40	VREF+/CVREF+/AN28/RA10
5	EBID7/AN15/PMD7/RE7	41	AVDD
6	EBIA6/AN22/RPC1/PMA6/RC1	42	AVSS
7	AN35/ETXD0/RJ8	43	AN38/ETXD2/RH0
8	AN36/ETXD1/RJ9	44	AN39/ETXD3/RH1
9	EBIBS0/RJ12	45	EBIRP/RH2
10	EBIBS1/RJ10	46	RH3
11	EBIA12/AN21/RPC2/PMA12/RC2	47	EBIA10/AN48/RPB8/PMA10/RB8
12	EBIWE/AN20/RPC3/PMWR/RC3	48	EBIA7/AN49/RPB9/PMA7/RB9
13	EBIOE/AN19/RPC4/PMRD/RC4	49	CVREFOUT/AN5/RPB10/RB10
14	AN14/C1IND/RPG6/SCK2/RG6	50	AN6/RB11
15	AN13/C1INC/RPG7/SDA4/RG7	51	EBIA1/PMA1/RK1
16	AN12/C2IND/RPG8/SCL4/RG8	52	EBIA3/PMA3/RK2
17	VSS	53	EBIA17/RK3
18	VDD	54	VSS
19	EBIA16/RK0	55	VDD
20	MCLR	56	TCK/AN29/RA1
21	EBIA2/AN11/C2INC/RPG9/PMA2/RG9	57	TDI/AN30/RPF13/SCK5/RF13
22	TMS/AN24/RA0	58	TDO/AN31/RPF12/RF12
23	AN25/RPE8/RE8	59	AN7/RB12
24	AN26/RPE9/RE9	60	AN8/RB13
25	AN45/C1INA/RPB5/RB5	61	AN9/RPB14/SCK3/RB14
26	AN4/C1INB/RB4	62	AN10/RPB15/OCFB/RB15
27	AN37/ERXCLK/EREFCLK/RJ11	63	VSS
28	EBIA13/PMA13/RJ13	64	VDD
29	EBIA11/PMA11/RJ14	65	AN40/ERXERR/RH4
30	EBIA0/PMA0/RJ15	66	AN41/ERXD1/RH5
31	AN3/C2INA/RPB3/RB3	67	AN42/ERXD2/RH6
32	VSS	68	EBIA4/PMA4/RH7
33	VDD	69	AN32/RPD14/RD14
34	AN2/C2INB/RPB2/RB2	70	AN33/RPD15/SCK6/RD15
35	PGEC1/AN1/RPB1/RB1	71	OSC1/CLKI/RC12
36	PGED1/AN0/RPB0/RB0	72	OSC2/CLKO/RC15

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

TABLE 5: PIN NAMES FOR 144-PIN DEVICES (CONTINUED)

144-PIN LQFP AND TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)144
PIC32MZ1024EF(G/H/M)144
PIC32MZ1024EF(E/F/K)144
PIC32MZ2048EF(G/H/M)144

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Pin Number	Full Pin Name	Pin Number	Full Pin Name
73	VBUS	109	RPD1/SCK1/RD1
74	VUSB3V3	110	EBID14/RPD2/PMD14/RD2
75	VSS	111	EBID15/RPD3/PMD15/RD3
76	D-	112	EBID12/RPD12/PMD12/RD12
77	D+	113	EBID13/PMD13/RD13
78	RPF3/USBID/RF3	114	ETXERR/RJ0
79	SDA3/RPF2/RF2	115	EMDIO/RJ1
80	SCL3/RPF8/RF8	116	EBIRDY3/RJ2
81	ERXD0/RH8	117	EBIA22/RJ3
82	ERXD3/RH9	118	$\overline{\text{SQICS0}}$/RPD4/RD4
83	ECOL/RH10	119	$\overline{\text{SQICS1}}$/RPD5/RD5
84	EBIRDY2/RH11	120	ETXEN/RPD6/RD6
85	SCL2/RA2	121	ETXCLK/RPD7/RD7
86	EBIRDY1/SDA2/RA3	122	VDD
87	EBIA14/PMCS1/PMA14/RA4	123	VSS
88	VDD	124	EBID11/RPF0/PMD11/RF0
89	VSS	125	EBID10/RPF1/PMD10/RF1
90	EBIA9/RPF4/SDA5/PMA9/RF4	126	EBIA21/RK7
91	EBIA8/RPF5/SCL5/PMA8/RF5	127	EBID9/RPG1/PMD9/RG1
92	EBIA18/RK4	128	EBID8/RPG0/PMD8/RG0
93	EBIA19/RK5	129	TRCLK/SQICLK/RA6
94	EBIA20/RK6	130	TRD3/SQID3/RA7
95	RPA14/SCL1/RA14	131	$\overline{\text{EBICS0}}$/RJ4
96	RPA15/SDA1/RA15	132	$\overline{\text{EBICS1}}$/RJ5
97	EBIA15/RPD9/PMCS2/PMA15/RD9	133	$\overline{\text{EBICS2}}$/RJ6
98	RPD10/SCK4/RD10	134	$\overline{\text{EBICS3}}$/RJ7
99	EMDC/RPD11/RD11	135	EBID0/PMD0/RE0
100	ECRS/RH12	136	VSS
101	ERXDV/ECRSDV/RH13	137	VDD
102	RH14	138	EBID1/PMD1/RE1
103	EBIA23/RH15	139	TRD2/SQID2/RG14
104	RPD0/RTCC/INT0/RD0	140	TRD1/SQID1/RG12
105	SOSCI/RPC13/RC13	141	TRD0/SQID0/RG13
106	SOSCO/RPC14/T1CK/RC14	142	EBID2/PMD2/RE2
107	VDD	143	EBID3/RPE3/PMD3/RE3
108	VSS	144	EBID4/AN18/PMD4/RE4

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

NOTES:

REGISTER 3-10: FCSR: FLOATING POINT CONTROL AND STATUS REGISTER; CP1 REGISTER 31

bit 16	**V:** Invalid Operation bit
bit 15	**Z:** Divide-by-Zero bit
bit 14	**O:** Overflow bit
bit 13	**U:** Underflow bit
bit 12	**I:** Inexact bit
bit 11-7	**ENABLES<4:0>:** FPU Exception Enable bits These bits control whether or not a trap is taken when an IEEE exception condition occurs for any of the five conditions. The trap occurs when both an enable bit and its corresponding cause bit are set either during an FPU arithmetic operation or by moving a value to the FCSR or one of its alternative representations.
bit 11	**V:** Invalid Operation bit
bit 10	**Z:** Divide-by-Zero bit
bit 9	**O:** Overflow bit
bit 8	**U:** Underflow bit
bit 7	**I:** Inexact bit
bit 6-2	**FLAGS<4:0>:** FPU Flags bits These bits show any exception conditions that have occurred for completed instructions since the flag was last reset by software.
bit 6	**V:** Invalid Operation bit
bit 5	**Z:** Divide-by-Zero bit
bit 4	**O:** Overflow bit
bit 3	**U:** Underflow bit
bit 2	**I:** Inexact bit
bit 1-0	**RM<1:0>:** Rounding Mode control bits 11 = Round towards Minus Infinity (− ∞) 10 = Round towards Plus Infinity (+ ∞) 01 = Round toward Zero (0) 00 = Round to Nearest

5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MZ EF devices contain an internal Flash program memory for executing user code, which includes the following features:

- Two Flash banks for live update support
- Dual boot support
- Write protection for program and boot Flash
- ECC support

There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193) in the *"PIC32 Family Reference Manual".*

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the *"PIC32 Flash Programming Specification"* (DS60001145), which is available for download from the Microchip web site (www.microchip.com).

Note: In PIC32MZ EF devices, the Flash page size is 16 KB (4K IW) and the row size is 2 KB (512 IW).

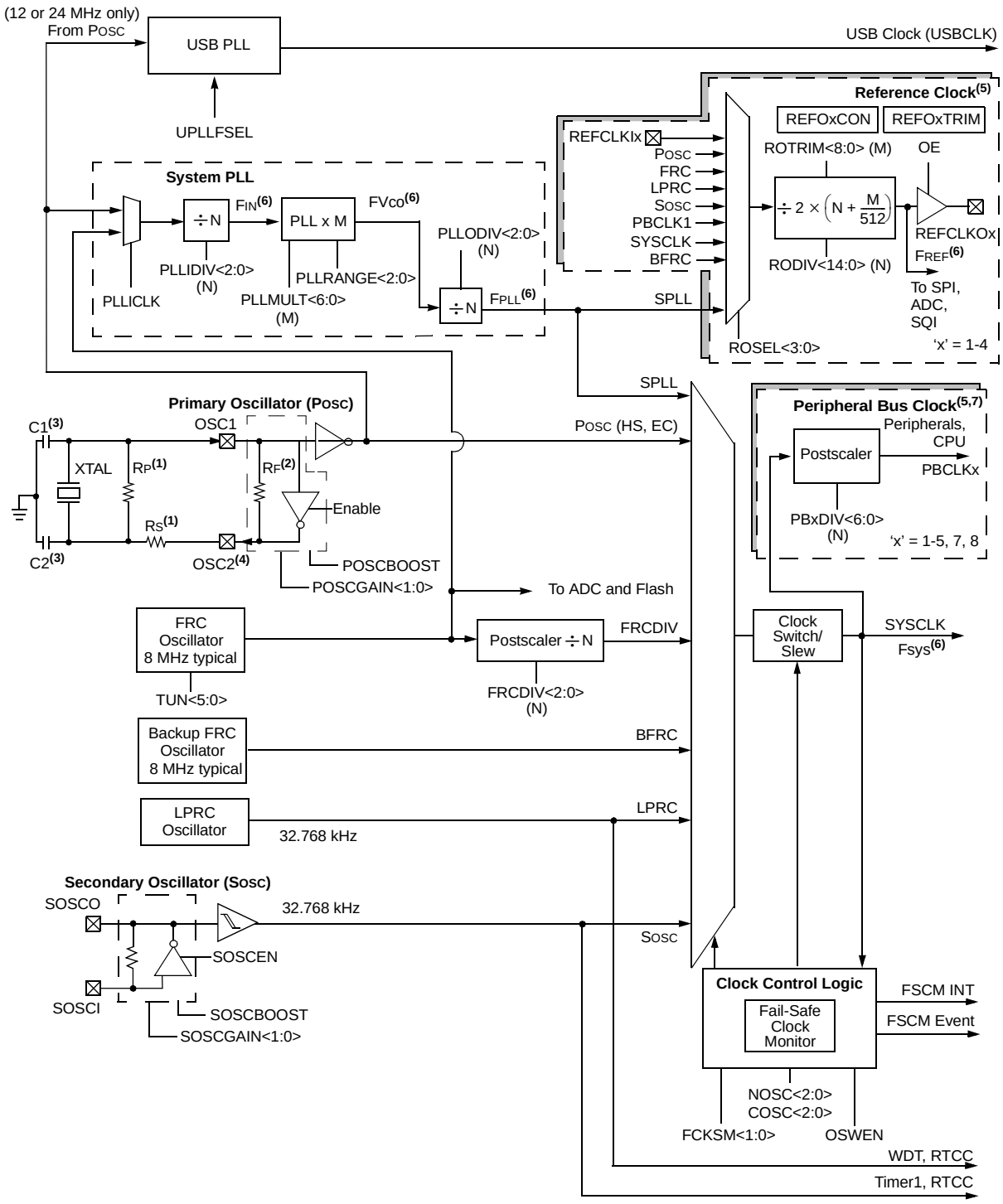
TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0768	OFF138	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
076C	OFF139	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0770	OFF140	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0774	OFF141	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0778	OFF142	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
077C	OFF143	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0780	OFF144	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0784	OFF145	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0788	OFF146	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
078C	OFF147	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0790	OFF148(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0794	OFF149(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0798	OFF150(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
079C	OFF151(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07A0	OFF152(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

FIGURE 8-1: PIC32MZ EF FAMILY OSCILLATOR DIAGRAM



Notes:
1. A series resistor, RS, may be required for AT strip cut crystals, or to eliminate clipping. Alternately, to increase oscillator circuit gain, add a parallel resistor, RP.
2. The internal feedback resistor, RF, is typically in the range of 2 to 10 MΩ.
3. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the "*PIC32 Family Reference Manual*" for help in determining the best oscillator components.
4. PBCLK1 divided by 2 is available on the OSC2 pin in certain clock modes.
5. Shaded regions indicate multiple instantiations of a peripheral or feature.
6. Refer to Table 37-19 in **Section 37.0 "Electrical Characteristics"** for frequency limitations.
7. If the DEVCFG registers are configured for a SYSCLK speed greater than 200 MHz, these PBCLKs will be running faster than the maximum rating when the device comes out of Reset. To ensure proper operation, firmware must start the device at a speed less than or equal to 200 MHz, adjust the speed of the PBCLKs, and then raise the SYSCLK speed to the desired speed.

REGISTER 9-1: PRECON: PREFETCH MODULE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
	—	—	—	—	—	PFMSECEN	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
	—	—	PREFEN<1:0>		—	PFMWS<2:0>(1)		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **PFMSECEN:** Flash SEC Interrupt Enable bit
1 = Generate an interrupt when the PFMSEC bit (PRESTAT<26>) is set
0 = Do not generate an interrupt when the PFMSEC bit is set

bit 25-6 **Unimplemented:** Read as '0'

bit 5-4 **PREFEN<1:0>:** Predictive Prefetch Enable bits
11 = Enable predictive prefetch for any address
10 = Enable predictive prefetch for CPU instructions and CPU data
01 = Enable predictive prefetch for CPU instructions only
00 = Disable predictive prefetch

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **PFMWS<2:0>:** PFM Access Time Defined in Terms of SYSCLK Wait States bits(1)
111 = Seven Wait states
•
•
•
010 = Two Wait states
001 = One Wait state
000 = Zero Wait states

Note 1: For the Wait states to SYSCLK relationship, refer to Table 37-13 in **Section37.0 "Electrical Characteristics"**.

TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3248	USB DMA5A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
324C	USB DMA5N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3254	USB DMA6C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000
3258	USB DMA6A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
325C	USB DMA6N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3264	USB DMA7C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000
3268	USB DMA7A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
326C	USB DMA7N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3274	USB DMA8C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000
3278	USB DMA8A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
327C	USB DMA8N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3304	USB E1RPC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RQPKTCNT<15:0>																0000
3308	USB E2RPC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RQPKTCNT<15:0>																0000
330C	USB E3RPC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RQPKTCNT<15:0>																0000
3310	USB E4RPC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RQPKTCNT<15:0>																0000
3314	USB E5RPC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RQPKTCNT<15:0>																0000
3318	USB E6RPC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RQPKTCNT<15:0>																0000
331C	USB E7RPC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RQPKTCNT<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

REGISTER 11-28: USBLPMR1: USB LINK POWER MANAGEMENT CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	LPMERRIE	LPMRESIE	LPMACKIE	LPMNYIE	LPMSTIE	LPMTOIE
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC
	—	—	—	LPMNAK	LPMEN<1:0>		LPMRES	LPMXMT
15:8	R-0	R-0	R-0	R-0	U-0	U-0	U-0	R-0
	ENDPOINT<3:0>				—	—	—	RMTWAK
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	HIRD<3:0>				LNKSTATE<3:0>			

Legend:	HC = Hardware Cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29 **LPMERRIE:** LPM Error Interrupt Enable bit
1 = LPMERR interrupt is enabled
0 = LPMERR interrupt is disabled

bit 28 **LPMRESIE:** LPM Resume Interrupt Enable bit
1 = LPMRES interrupt is enabled
0 = LPMRES interrupt is disabled

bit 27 **LPMACKIE:** LPM Acknowledge Interrupt Enable bit
1 = Enable the LPMACK Interrupt
0 = Disable the LPMACK Interrupt

bit 26 **LPMNYIE:** LPM NYET Interrupt Enable bit
1 = Enable the LPMNYET Interrupt
0 = Disable the LPMNYET Interrupt

bit 25 **LPMSTIE:** LPM STALL Interrupt Enable bit
1 = Enable the LPMST Interrupt
0 = Disable the LPMST Interrupt

bit 24 **LPMTOIE:** LPM Time-out Interrupt Enable bit
1 = Enable the LPMTO Interrupt
0 = Disable the LPMTO Interrupt

bit 23-21 **Unimplemented:** Read as '0'

bit 20 **LPMNAK:** LPM-only Transaction Setting bit
1 = All endpoints will respond to all transactions other than a LPM transaction with a NAK
0 = Normal transaction operation
Setting this bit to '1' will only take effect after the USB module as been LPM suspended.

bit 19-18 **LPMEN<1:0>:** LPM Enable bits (*Device mode*)
11 = LPM Extended transactions are supported
10 = LPM and Extended transactions are not supported
01 = LPM mode is not supported but Extended transactions are supported
00 = LPM Extended transactions are supported

bit 17 **LPMRES:** LPM Resume bit
1 = Initiate resume (remote wake-up). Resume signaling is asserted for 50 µs.
0 = No resume operation
This bit is self-clearing.

TABLE 12-7: PORTC REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	—	—	—	—	—	F000
0220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUC15	CNPUC14	CNPUC13	CNPUC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
0260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDC15	CNPDC14	CNPDC13	CNPDC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
0270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0280	CNENC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNENC15	CNENC14	CNENC13	CNENC12													0000
0290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATC15	CNSTATC14	CNSTATC13	CNSTATC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
02A0	CNNEC	31:16	—	—		—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEC15	CNNEC14	CNNEC13	CNNEC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
02B0	CNFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFC15	CNFC14	CNFC13	CNFC12	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

15.1 Deadman Timer Control Registers

TABLE 15-1: DEADMAN TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0A00	DMTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	x000
0A10	DMTPRECLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STEP1<7:0>								—	—	—	—	—	—	—	—	0000
0A20	DMTCLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STEP2<7:0>								0000
0A30	DMTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN	0000
0A40	DMTCNT	31:16	COUNTER<31:0>																0000
		15:0																	0000
0A60	DMTPSCNT	31:16	PSCNT<31:0>																0000
		15:0																	00xx
0A70	DMTPSINTV	31:16	PSINTV<31:0>																0000
		15:0																	000x

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

23.0 PARALLEL MASTER PORT (PMP)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. "Parallel Master Port (PMP)"** (DS60001128) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

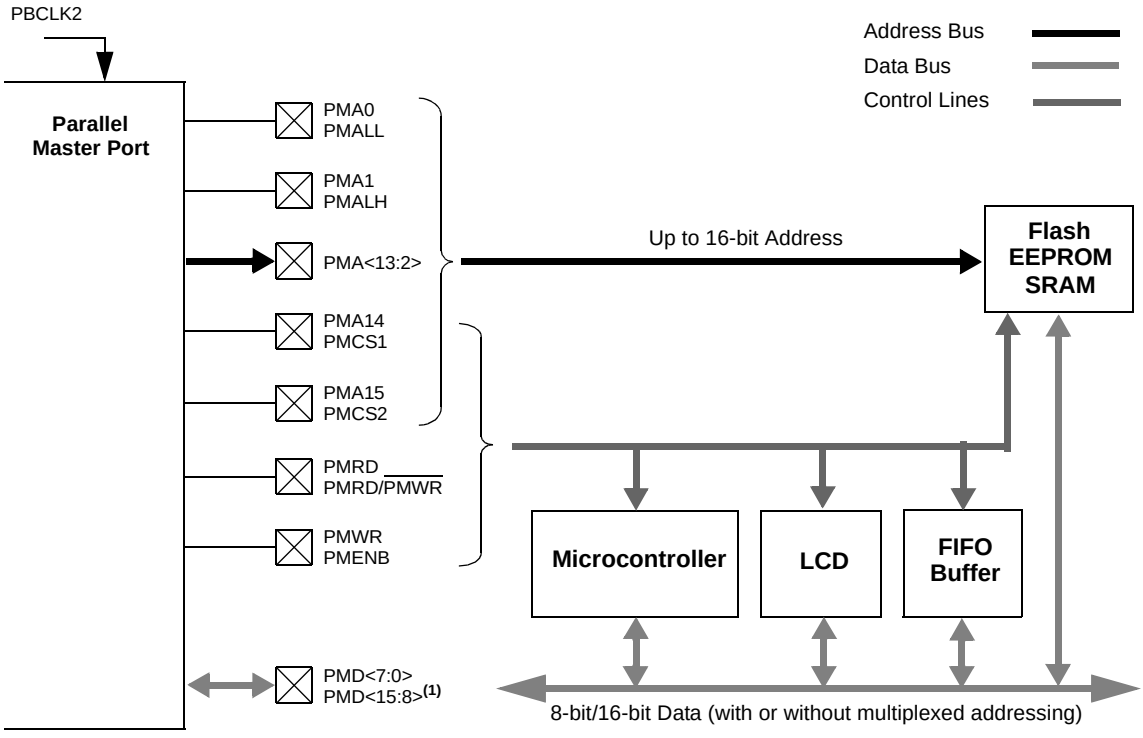
The PMP is a parallel 8-bit/16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

The following are key features of the PMP module:

- 8-bit,16-bit interface
- Up to 16 programmable address lines
- Up to two Chip Select lines
- Programmable strobe options:
  - Individual read and write strobes, or
  - Read/$\overline{\text{write}}$ strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Parallel Slave Port support:
  - Legacy addressable
  - Address support
  - 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Operate during Sleep and Idle modes
- Separate configurable read/write registers or dual buffers for Master mode
- Fast bit manipulation using CLR, SET, and INV registers

Note: On 64-pin devices, data pins PMD<15:8> are not available in 16-bit Master modes.

FIGURE 23-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



Note: On 64-pin devices, data pins PMD<15:8> are not available in 16-bit Master modes.

REGISTER 29-17: CiFLTCON7: CAN FILTER CONTROL REGISTER 7 (CONTINUED)

bit 15 **FLTEN29:** Filter 29 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL29<1:0>:** Filter 29 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL29<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN28:** Filter 28 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL28<1:0>:** Filter 28 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL28<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-23: EMAC1CFG1: ETHERNET CONTROLLER MAC CONFIGURATION 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-1	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	SOFT RESET	SIM RESET	—	—	RESET RMCS	RESET RFUN	RESET TMCS	RESET TFUN
7:0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1
	—	—	—	LOOPBACK	TX PAUSE	RX PAUSE	PASSALL	RX ENABLE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SOFTRESET:** Soft Reset bit
Setting this bit will put the MACMII in reset. Its default value is '1'.

bit 14 **SIMRESET:** Simulation Reset bit
Setting this bit will cause a reset to the random number generator within the Transmit Function.

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **RESETRMCS:** Reset MCS/RX bit
Setting this bit will put the MAC Control Sub-layer/Receive domain logic in reset.

bit 10 **RESETRFUN:** Reset RX Function bit
Setting this bit will put the MAC Receive function logic in reset.

bit 9 **RESETTMCS:** Reset MCS/TX bit
Setting this bit will put the MAC Control Sub-layer/TX domain logic in reset.

bit 8 **RESETTFUN:** Reset TX Function bit
Setting this bit will put the MAC Transmit function logic in reset.

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **LOOPBACK:** MAC Loopback mode bit
1 = MAC Transmit interface is loop backed to the MAC Receive interface
0 = MAC normal operation

bit 3 **TXPAUSE:** MAC TX Flow Control bit
1 = PAUSE Flow Control frames are allowed to be transmitted
0 = PAUSE Flow Control frames are blocked

bit 2 **RXPAUSE:** MAC RX Flow Control bit
1 = The MAC acts upon received PAUSE Flow Control frames
0 = Received PAUSE Flow Control frames are ignored

bit 1 **PASSALL:** MAC Pass all Receive Frames bit
1 = The MAC will accept all frames regardless of type (Normal vs. Control)
0 = The received Control frames are ignored

bit 0 **RXENABLE:** MAC Receive Enable bit
1 = Enable the MAC receiving of frames
0 = Disable the MAC receiving of frames

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

32.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 20. "Comparator Voltage Reference (CVREF)"** (DS60001109) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

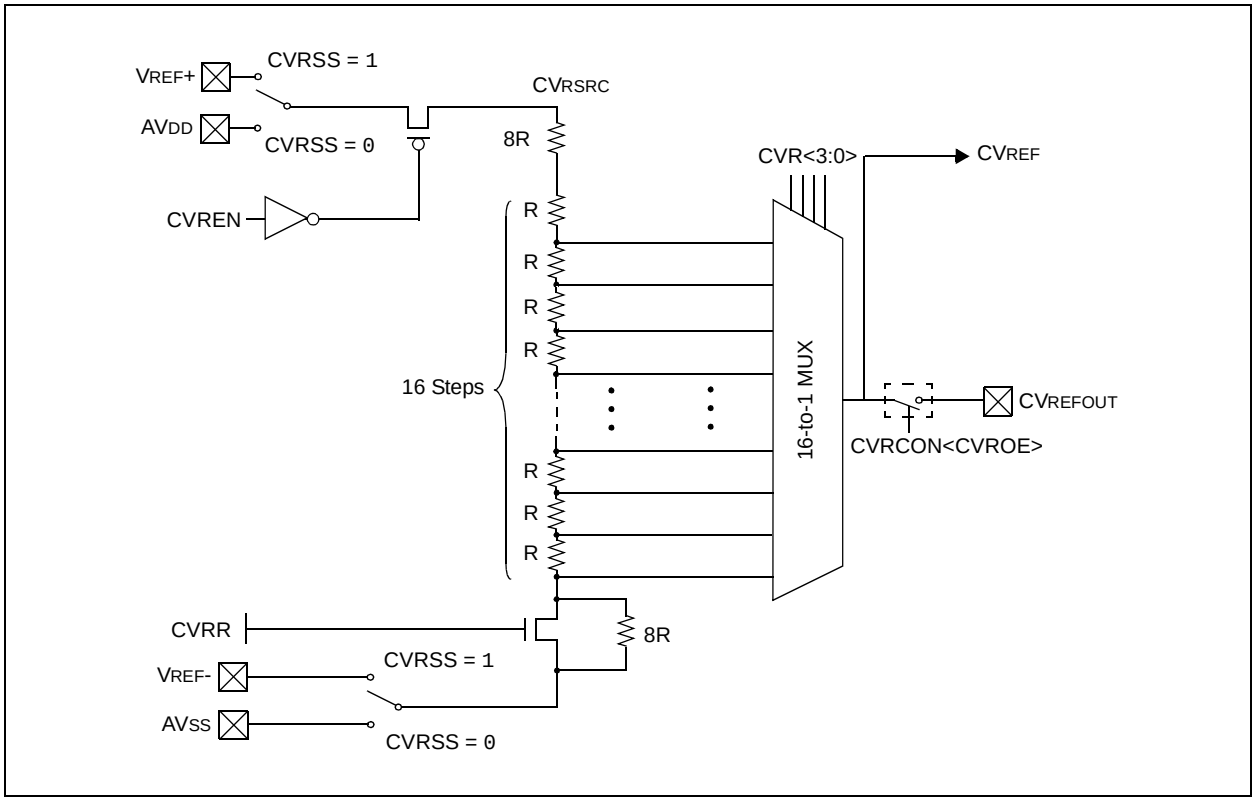
The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The comparator voltage reference has the following features:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

A block diagram of the CVREF module is illustrated in Figure 32-1.

FIGURE 32-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



A.6 DMA

The DMA controller in PIC32MZ EF devices is similar to the DMA controller in PIC32MX5XX/6XX/7XX devices. New features include the extension of pattern matching to two by bytes and the addition of the optional Pattern Ignore mode. Table A-7 lists differences (indicated by **Bold** type) that will affect software migration.

TABLE A-7: DMA DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Read/Write Status on Error	
	The RDWR bit has moved from DMASTAT<3> in PIC32MX5XX/6XX/7XX devices to DMASTAT<31> in PIC32MZ EF devices.
RDWR (DMASTAT<**3**>) 1 = Last DMA bus access when an error was detected was a read 0 = Last DMA bus access when an error was detected was a write	RDWR (DMASTAT<**31**>) 1 = Last DMA bus access when an error was detected was a read 0 = Last DMA bus access when an error was detected was a write
Source-to-Destination Transfer	
On PIC32MX devices, a DMA channel performs a read of the source data and completes the transfer of this data into the destination address before it is ready to read the next data from the source.	On PIC32MZ EF devices, the DMA implements a 4-deep queue for data transfers. A DMA channel reads the source data and places it into the queue, regardless of whether previous data in the queue has been delivered to the destination address.

TABLE C-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
37.0 "Electrical Characteristics"	The DC Characteristics: Operating Current (I_{DD}) and Note 6 were updated (see Table 37-6). The DC Characteristics: Idle Current (I_{IDLE}) and Note 4 were updated (see Table 37-7). Parameter DC40m and Note 5 in the DC Characteristics: Power-down Current (I_{PD}) were updated (see Table 37-8). Parameter DO50 (Cosco) was removed from the Capacitive Loading Requirements on Output Pins (see Table 37-16). The Internal FRC Accuracy and Internal LPRC conditions were updated for 125ºC (see Table 37-20 and Table 37-21). Parameter SP15 and Note 5 of the SPIx Module Master Mode Timing Requirements were updated (see Table 37-30 and Table 37-31). The Temperature Sensor Specifications were updated (see Table 37-41).
38.0 "Extended Temperature Electrical Characteristics"	New chapter for Extended Temperature devices was added.
39.0 "AC and DC Characteristics Graphs"	The Typical Temperature Sensor Voltage graph was updated (see Figure 39-7).
40.0 "Packaging Information"	The package drawings and land pattern for the 64-Lead Plastic Quad Flat, No Lead Package (MR) were updated.
Appendix A: "Migrating from PIC32MX5XX/6XX/7XX to PIC32MZ EF"	The Primary Oscillator Configuration section in the Oscillator Configuration Differences was updated (see Table A-1).
Appendix B: "Migrating from PIC32MZ EC to PIC32MZ EF"	Boot Flashing aliasing was updated for PIC32MZ EF devices (see Table B-4).

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