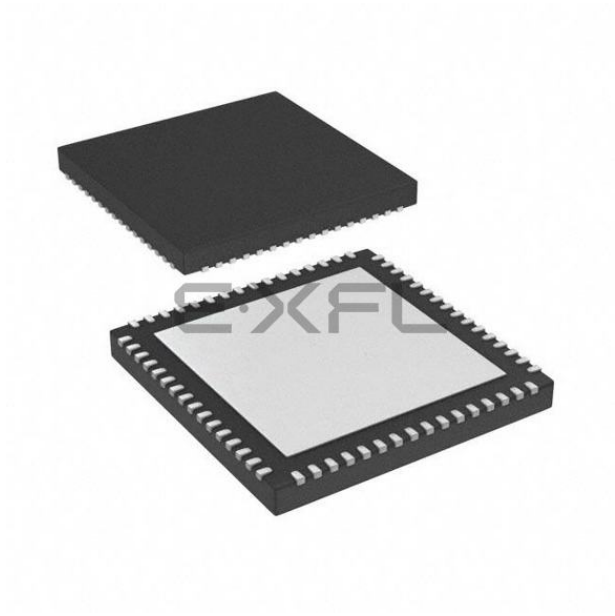

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	46
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efe064-e-mr

REGISTER 3-9: FENR: FLOATING POINT EXCEPTIONS AND MODES ENABLE REGISTER; CP1 REGISTER 28

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	ENABLES<4:1>			
					V	Z	O	U
7:0	R/W-x	U-0	U-0	U-0	U-0	R-x	R/W-x	R/W-x
	ENABLES<0>	—	—	—	—	FS	RM<1:0>	
	I							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11-7 **ENABLES<4:0>:** FPU Exception Enable bits

These bits control whether or not a trap is taken when an IEEE exception condition occurs for any of the five conditions. The trap occurs when both an enable bit and its corresponding cause bit are set either during an FPU arithmetic operation or by moving a value to the FCSR or one of its alternative representations.

bit 11 **V:** Invalid Operation bit

bit 10 **Z:** Divide-by-Zero bit

bit 9 **O:** Overflow bit

bit 8 **U:** Underflow bit

bit 7 **I:** Inexact bit

bit 6-3 **Unimplemented:** Read as '0'

bit 2 **FS:** Flush to Zero control bit

1 = Denormal input operands are flushed to zero. Tiny results are flushed to either zero or the applied format's smallest normalized number (MinNorm) depending on the rounding mode settings.

0 = Denormal input operands result in an Unimplemented Operation exception.

bit 1-0 **RM<1:0>:** Rounding Mode control bits

11 = Round towards Minus Infinity ($-\infty$)
10 = Round towards Plus Infinity ($+\infty$)
01 = Round toward Zero (0)
00 = Round to Nearest

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
05C0	OFF032	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05C4	OFF033	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05C8	OFF034	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05CC	OFF035	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05D0	OFF036	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05D4	OFF037	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05D8	OFF038	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05DC	OFF039	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E0	OFF040	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E4	OFF041	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E8	OFF042	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05EC	OFF043	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F0	OFF044	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F4	OFF045	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F8	OFF046	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

REGISTER 7-8: OFFx: INTERRUPT VECTOR ADDRESS OFFSET REGISTER (x = 0-190)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	VOFF<17:16>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VOFF<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	VOFF<7:1>							—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 17-1 **VOFF<17:1>:** Interrupt Vector 'x' Address Offset bits

bit 0 **Unimplemented:** Read as '0'

TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3028	USB FIFO2	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
302C	USB FIFO3	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3030	USB FIFO4	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3034	USB FIFO5	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3038	USB FIFO6	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
303C	USB FIFO7	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3060	USBOTG	31:16	—	—	—	RXDPB	RXFIFOSZ<3:0>				—	—	—	TXDPB	TXFIFOSZ<3:0>				0000
		15:0	—	—	—	—	—	—	TXEDMA	RXEDMA	BDEV	FSDEV	LSDEV	VBUS<1:0>		HOSTMODE	HOSTREQ	SESSION	0080
3064	USB FIFOA	31:16	—	—	—	RXFIFOAD<12:0>													0000
		15:0	—	—	—	TXFIFOAD<12:0>													0000
306C	USB HWVER	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC	VERMAJOR<4:0>					VERMINOR<9:0>										0800
3078	USB INFO	31:16	VPLEN<7:0>								WTCON<3:0>				WTID<3:0>				3C5C
		15:0	DMACHANS<3:0>				RAMBITS<3:0>				RXENDPTS<3:0>				TXENDPTS<3:0>				8C77
307C	USB EOFRST	31:16	—	—	—	—	—	—	NRSTX	NRST	LSEOF<7:0>								0072
		15:0	FSEOF<7:0>								HSEOF<7:0>								7780
3080	USB E0TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
3084	USB E0RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
3088	USB E1TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
308C	USB E1RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
3090	USB E2TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
3094	USB E2RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
3098	USB E3TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

REGISTER 11-8: USBIENCSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 1-7) (CONTINUED)

bit 15-11 **MULT<4:0>:** Multiplier Control bits

For Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints, multiplies TXMAXP by MULT+1 for the payload size.

For Bulk endpoints, MULT can be up to 32 and defines the number of “USB” packets of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. The data packet is required to be an exact multiple of the payload specified by TXMAXP.

For Isochronous/Interrupts endpoints operating in Hi-Speed mode, MULT may be either 2 or 3 and specifies the maximum number of such transactions that can take place in a single microframe.

bit 10-0 **TXMAXP<10:0>:** Maximum TX Payload per transaction Control bits

This field sets the maximum payload (in bytes) transmitted in a single transaction. The value is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-Speed and Hi-Speed operations.

TXMAXP must be set to an even number of bytes for proper interrupt generation in DMA Mode 1.

TABLE 12-16: PORTG REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	ANSELG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSG9	ANSG8	ANSG7	ANSG6	—	—	—	—	—	—	03C0
0610	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	—	—	03C0
0620	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RG9	RG8	RG7	RG6	—	—	—	—	—	—	xxxx
0630	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	—	—	xxxx
0640	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	—	—	0000
0650	CNPUG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	—	—	0000
0660	CNPDG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	—	—	0000
0670	CNCONG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0680	CNENG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNENG9	CNENG8	CNENG7	CNENG6	—	—	—	—	—	—	0000
0690	CNSTATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CN STATG9	CN STATG8	CN STATG7	CN STATG6	—	—	—	—	—	—	0000
06A0	CNNEG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNNEG9	CNNEG8	CNNEG7	CNNEG6	—	—	—	—	—	—	0000
06B0	CNFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNFG9	CNFG8	CNFG7	CNFG6	—	—	—	—	—	—	0000
06C0	SRCON0G	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	SR0G9	—	—	SR0G6	—	—	—	—	—	—	0000
06D0	SRCON1G	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	SR1G9	—	—	SR1G6	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 20-18: SQI1BDPOLLCON: SQI BUFFER DESCRIPTOR POLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLLCON<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLLCON<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **POLLCON<15:0>:** Buffer Descriptor Processor Poll Status bits
These bits indicate the number of cycles the BDP would wait before refetching the descriptor control word if the previous descriptor fetched was disabled.

REGISTER 20-19: SQI1BDTXDSTAT: SQI BUFFER DESCRIPTOR DMA TRANSMIT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-x	R-x	R-x	R-x	U-0
	—	—	—	TXSTATE<3:0>				—
23:16	U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
	—	—	—	TXBUFCNT<4:0>				
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	TXCURBUFLEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-25 **TXSTATE<3:0>:** Current DMA Transmit State Status bits
These bits provide information on the current DMA receive states.

bit 24-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFCNT<4:0>:** DMA Buffer Byte Count Status bits
These bits provide information on the internal FIFO space.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **TXCURBUFLEN<7:0>:** Current DMA Transmit Buffer Length Status bits
These bits provide the length of the current DMA transmit buffer.

REGISTER 22-1: UxMODE: UARTx MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>(1)	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** UARTx Enable bit
- 1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by UEN<1:0> and UTXEN control bits
- 0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation in Idle mode

bit 12 **IREN:** IrDA Encoder and Decoder Enable bit
- 1 = IrDA is enabled
- 0 = IrDA is disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits(1)
- 11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit
- 1 = Wake-up is enabled
- 0 = Wake-up is disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Loopback mode is enabled
- 0 = Loopback mode is disabled

Note 1: These bits are present for legacy compatibility, and are superseded by PPS functionality on these devices. For additional information, see **Section 12.4 "Peripheral Pin Select (PPS)"**.

23.0 PARALLEL MASTER PORT (PMP)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. "Parallel Master Port (PMP)"** (DS60001128) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

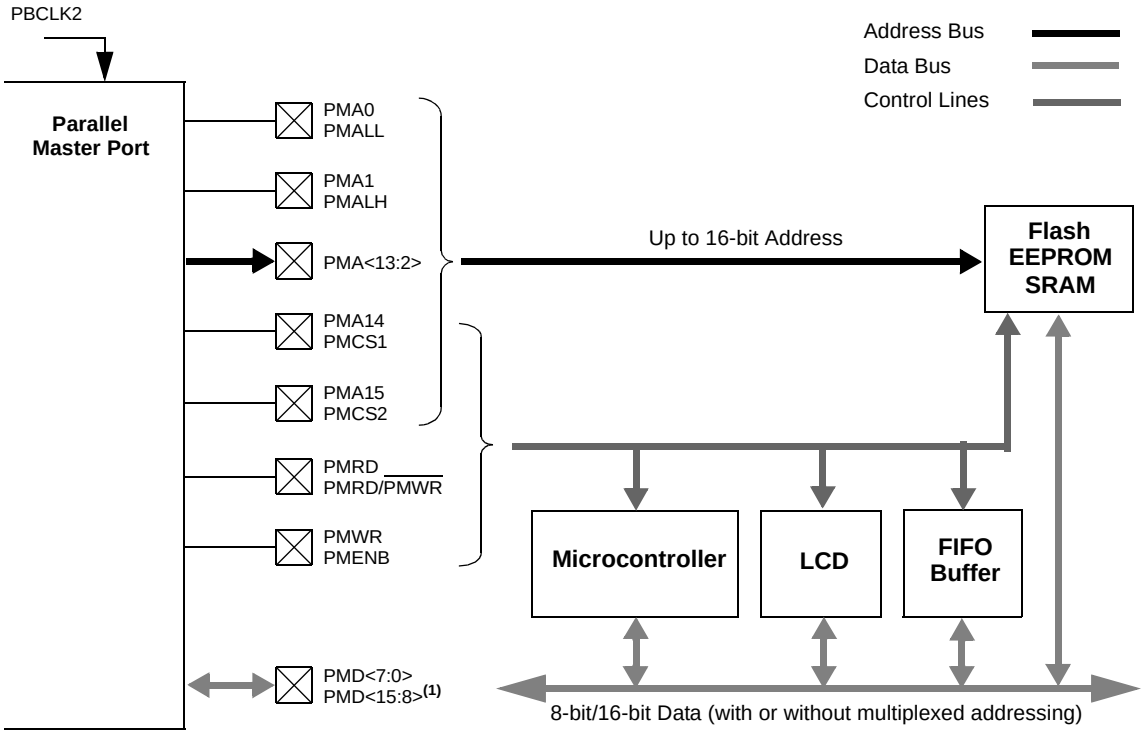
The PMP is a parallel 8-bit/16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

The following are key features of the PMP module:

- 8-bit,16-bit interface
- Up to 16 programmable address lines
- Up to two Chip Select lines
- Programmable strobe options:
  - Individual read and write strobes, or
  - Read/$\overline{\text{write}}$ strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Parallel Slave Port support:
  - Legacy addressable
  - Address support
  - 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Operate during Sleep and Idle modes
- Separate configurable read/write registers or dual buffers for Master mode
- Fast bit manipulation using CLR, SET, and INV registers

Note: On 64-pin devices, data pins PMD<15:8> are not available in 16-bit Master modes.

FIGURE 23-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



Note: On 64-pin devices, data pins PMD<15:8> are not available in 16-bit Master modes.

REGISTER 23-4: PMDOUT: PARALLEL PORT OUTPUT DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAOUT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAOUT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **DATAOUT<15:0>:** Port Data Output bits

This register is used for Read operations in the Enhanced Parallel Slave mode and Write operations for Dual Buffer Master mode.

In Dual Buffer Master mode, the DUALBUF bit (PMPCON<17>) = 1, a write to the MSB triggers the transaction on the PMP port. When MODE16 = 1, MSB = DATAOUT<15:8>. When MODE16 = 0, MSB = DATAOUT<7:0>.

Note: In Master mode, a read will return the last value written to the register. In Slave mode, a read will return indeterminate results.

REGISTER 23-5: PMDIN: PARALLEL PORT INPUT DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAIN<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAIN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **DATAIN<15:0>:** Port Data Input bits

This register is used for both Parallel Master Port mode and Enhanced Parallel Slave mode.

In Parallel Master mode, a write to the MSB triggers the write transaction on the PMP port. Similarly, a read to the MSB triggers the read transaction on the PMP port.

When MODE16 = 1, MSB = DATAIN<15:8>. When MODE16 = 0, MSB = DATAIN<7:0>.

Note: This register is not used in Dual Buffer Master mode (i.e., DUALBUF bit (PMPCON<17>) = 1).

REGISTER 23-7: PMSTAT: PARALLEL PORT STATUS REGISTER (SLAVE MODES ONLY)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0, HS, SC	U-0	U-0	R-0	R-0	R-0	R-0
	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7:0	R-1	R/W-0, HS, SC	U-0	U-0	R-1	R-1	R-1	R-1
	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E

Legend:	HS = Hardware Set	SC = Software Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **IBF:** Input Buffer Full Status bit
- 1 = All writable input buffer registers are full
- 0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
- 1 = A write attempt to a full input byte buffer is occurred (must be cleared in software)
- 0 = No overflow is occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer x Status Full bits
- 1 = Input Buffer contains data that has not been read (reading buffer will clear this bit)
- 0 = Input Buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
- 1 = All readable output buffer registers are empty
- 0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
- 1 = A read occurred from an empty output byte buffer (must be cleared in software)
- 0 = No underflow is occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer x Status Empty bits
- 1 = Output buffer is empty (writing data to the buffer will clear this bit)
- 0 = Output buffer contains data that has not been transmitted

NOTES:

25.1 RTCC Control Registers

TABLE 25-1: RTCC REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0C00	RTCCON	31:16	—	—	—	—	—	—	CAL<9:0>										0000
		15:0	ON	—	SIDL	—	—	RTCCLKSEL<1:0>		RTCOUTSEL<1:0>		RTCCLKON	—	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	0000
0C10	RTCALRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALRMEN	CHIME	PIV	ALRMSYNC	AMASK<3:0>				ARPT<7:0>								0000
0C20	RTCTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0C30	RTCDATE	31:16	YEAR10<3:0>				YEAR01<3:0>				MONTH10<3:0>				MONTH01<3:0>				xxxx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx00
0C40	ALRMTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0C50	ALRMDATE	31:16	—	—	—	—	—	—	—	—	MONTH10<3:0>				MONTH01<3:0>				00xx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx0x

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 28-4: ADCTRGMODE: ADC TRIGGERING MODE FOR DEDICATED ADC REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	SH4ALT<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SH3ALT<1:0>		SH2ALT<1:0>		SH1ALT<1:0>		SH0ALT<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	STRGEN4	STRGEN3	STRGEN2	STRGEN1	STRGEN0
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	SSAMPEN4	SSAMPEN3	SSAMPEN2	SSAMPEN1	SSAMPEN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25-24 **SH4ALT<1:0>:** ADC4 Analog Input Select bit
- 11 = Reserved
- 10 = Reserved
- 01 = AN49
- 00 = AN4

bit 23-22 **SH3ALT<1:0>:** ADC3 Analog Input Select bit
- 11 = Reserved
- 10 = Reserved
- 01 = AN48
- 00 = AN3

bit 21-20 **SH2ALT<1:0>:** ADC2 Analog Input Select bit
- 11 = Reserved
- 10 = Reserved
- 01 = AN47
- 00 = AN2

bit 19-18 **SH1ALT<1:0>:** ADC1 Analog Input Select bit
- 11 = Reserved
- 10 = Reserved
- 01 = AN46
- 00 = AN1

bit 17-16 **SH0ALT<1:0>:** ADC0 Analog Input Select bit
- 11 = Reserved
- 10 = Reserved
- 01 = AN45
- 00 = AN0

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **STRGEN4:** ADC4 Presynchronized Triggers bit
- 1 = ADC4 uses presynchronized triggers
- 0 = ADC4 does not use presynchronized triggers

bit 11 **STRGEN3:** ADC3 Presynchronized Triggers bit
- 1 = ADC3 uses presynchronized triggers
- 0 = ADC3 does not use presynchronized triggers

bit 10 **STRGEN2:** ADC2 Presynchronized Triggers bit
- 1 = ADC2 uses presynchronized triggers
- 0 = ADC2 does not use presynchronized triggers

REGISTER 28-26: ADCTRGSNS: ADC TRIGGER LEVEL/EDGE SENSITIVITY REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	LVL11	LVL10	LVL9	LVL8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LVL7	LVL6	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11 **LVL11:LVL0:** Trigger Level and Edge Sensitivity bits

1 = Analog input is sensitive to the high level of its trigger (level sensitivity implies retriggering as long as the trigger signal remains high)

0 = Analog input is sensitive to the positive edge of its trigger (this is the value after a reset)

Note 1: This register specifies the trigger level for analog inputs 0 to 31.

2: The higher analog input ID belongs to Class 3, and therefore, is only scan triggered. All Class 3 analog inputs use the Scan Trigger, for which the level/edge is defined by the STRGLVL bit (ADCCON1<3>).

REGISTER 29-16: CiFLTCON6: CAN FILTER CONTROL REGISTER 6 (CONTINUED)

bit 15 **FLTEN25:** Filter 25 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL25<1:0>:** Filter 25 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL25<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN24:** Filter 24 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL24<1:0>:** Filter 24 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL24<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note:	The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 34-3: DEVCFG0/ADEVCFG0: DEVICE CONFIGURATION WORD 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-x	R/P	r-1	r-1	r-1	r-1	r-1	r-1
	—	EJTAGBEN	—	—	—	—	—	—
23:16	r-1	r-1	R/P	R/P	R/P	R/P	R/P	R/P
	—	—	POSCBOOST	POSCGAIN<1:0>		SOSCBOOST	SOSCGAIN<1:0>	
15:8	R/P	R/P	R/P	R/P	r-y	R/P	R/P	R/P
	SMCLR	DBGPER<2:0>			—	FSLEEP	FECCCON<1:0>	
7:0	r-1	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN(1)	DEBUG<1:0>	

Legend:	r = Reserved bit	y = Value set from Configuration bits on POR	
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** The reset value of this bit is the same as DEVSIGN0<31>.

bit 30 **EJTAGBEN:** EJTAG Boot Enable bit
- 1 = Normal EJTAG functionality
- 0 = Reduced EJTAG functionality

bit 29-22 **Reserved:** Write as '1'

bit 21 **POSCBOOST:** Primary Oscillator Boost Kick Start Enable bit
- 1 = Boost the kick start of the oscillator
- 0 = Normal start of the oscillator

bit 20-19 **POSCGAIN<1:0>:** Primary Oscillator Gain Control bits
- 11 = Gain Level 3 (highest)
- 10 = Gain Level 2
- 01 = Gain Level 1
- 00 = Gain Level 0 (lowest)

bit 18 **SOSCBOOST:** Secondary Oscillator Boost Kick Start Enable bit
- 1 = Boost the kick start of the oscillator
- 0 = Normal start of the oscillator

bit 17-16 **SOSCGAIN<1:0>:** Secondary Oscillator Gain Control bits
- 11 = Gain Level 3 (highest)
- 10 = Gain Level 2
- 01 = Gain Level 1
- 00 = Gain Level 0 (lowest)

bit 15 **SMCLR:** Soft Master Clear Enable bit
- 1 = $\overline{\text{MCLR}}$ pin generates a normal system Reset
- 0 = $\overline{\text{MCLR}}$ pin generates a POR Reset

bit 14-12 **DBGPER<2:0>:** Debug Mode CPU Access Permission bits
- 1xx = Allow CPU access to Permission Group 2 permission regions
- x1x = Allow CPU access to Permission Group 1 permission regions
- xx1 = Allow CPU access to Permission Group 0 permission regions
- 0xx = Deny CPU access to Permission Group 2 permission regions
- x0x = Deny CPU access to Permission Group 1 permission regions
- xx0 = Deny CPU access to Permission Group 0 permission regions

When the CPU is in Debug mode and the CPU1PG<1:0> bits (CFGPG<1:0>) are set to a denied permission group as defined by DBGPER<2:0>, the transaction request is assigned Group 3 permissions.

bit 11 **Reserved:** This bit is controlled by debugger/emulator development tools and should not be modified by the user.

Note 1: This bit sets the value of the JTAGEN bit in the CFGCON register.

36.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

36.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

36.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

36.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

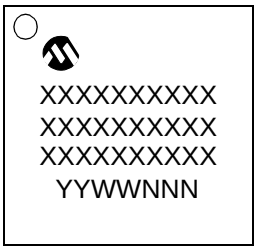
36.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

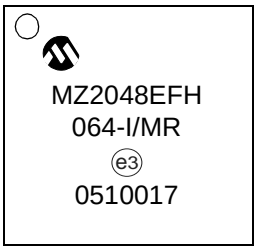
41.0 PACKAGING INFORMATION

41.1 Package Marking Information

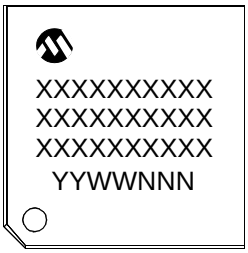
64-Lead QFN (9x9x0.9 mm)



Example

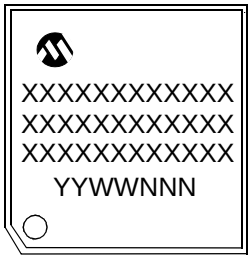


64-Lead TQFP (10x10x1 mm)

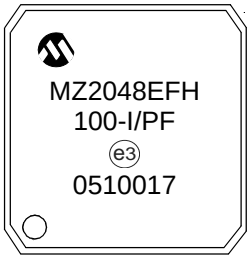


Example

100-Lead TQFP (14x14x1 mm)



Example

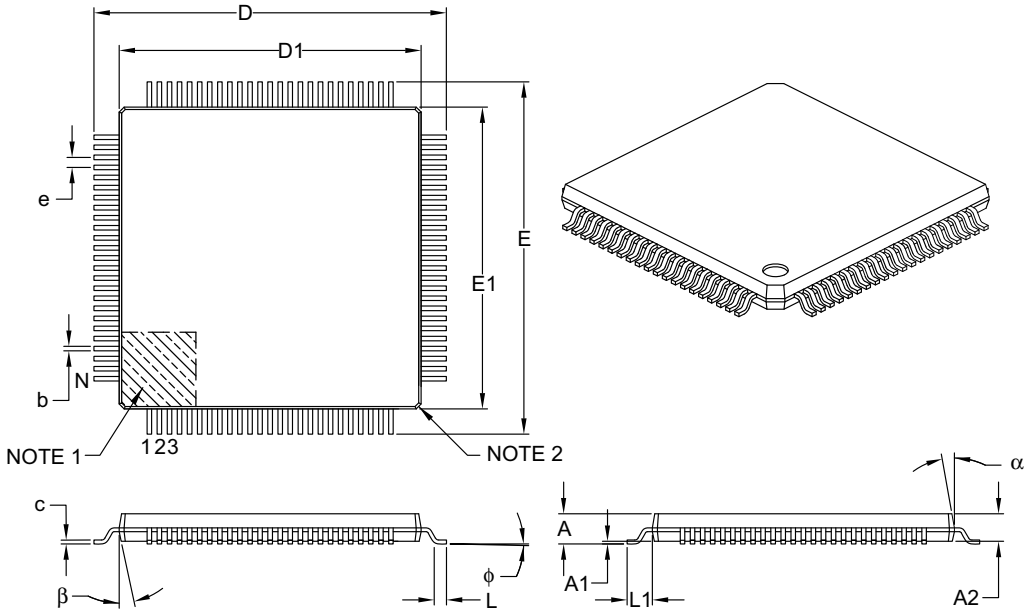


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.40 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.13	0.18	0.23
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B