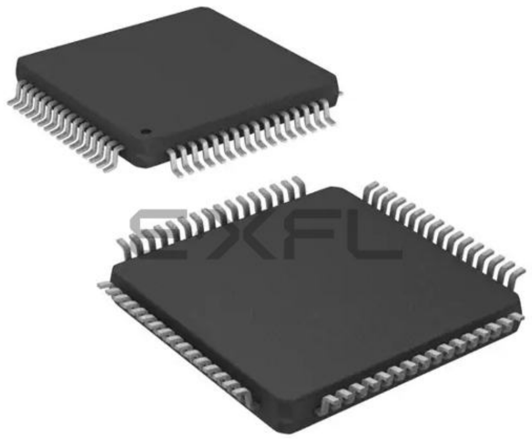

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	46
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efe064-e-pt

TABLE 1-9: SPI1 THROUGH SPI 6 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Serial Peripheral Interface 1							
SCK1	49	76	A52	109	I/O	ST	SPI1 Synchronous Serial Clock Input/Output
SDI1	PPS	PPS	PPS	PPS	I	ST	SPI1 Data In
SDO1	PPS	PPS	PPS	PPS	O	—	SPI1 Data Out
$\overline{\text{SS1}}$	PPS	PPS	PPS	PPS	I/O	ST	SPI1 Slave Synchronization Or Frame Pulse I/O
Serial Peripheral Interface 2							
SCK2	4	10	B6	14	I/O	ST	SPI2 Synchronous Serial Clock Input/output
SDI2	PPS	PPS	PPS	PPS	I	ST	SPI2 Data In
SDO2	PPS	PPS	PPS	PPS	O	—	SPI2 Data Out
$\overline{\text{SS2}}$	PPS	PPS	PPS	PPS	I/O	ST	SPI2 Slave Synchronization Or Frame Pulse I/O
Serial Peripheral Interface 3							
SCK3	29	43	A28	61	I/O	ST	SPI3 Synchronous Serial Clock Input/Output
SDI3	PPS	PPS	PPS	PPS	I	ST	SPI3 Data In
SDO3	PPS	PPS	PPS	PPS	O	—	SPI3 Data Out
$\overline{\text{SS3}}$	PPS	PPS	PPS	PPS	I/O	ST	SPI3 Slave Synchronization Or Frame Pulse I/O
Serial Peripheral Interface 4							
SCK4	44	69	A46	98	I/O	ST	SPI4 Synchronous Serial Clock Input/Output
SDI4	PPS	PPS	PPS	PPS	I	ST	SPI4 Data In
SDO4	PPS	PPS	PPS	PPS	O	—	SPI4 Data Out
$\overline{\text{SS4}}$	PPS	PPS	PPS	PPS	I/O	ST	SPI4 Slave Synchronization Or Frame Pulse I/O
Serial Peripheral Interface 5							
SCK5	—	39	A26	57	I/O	ST	SPI5 Synchronous Serial Clock Input/Output
SDI5	—	PPS	PPS	PPS	I	ST	SPI5 Data In
SDO5	—	PPS	PPS	PPS	O	—	SPI5 Data Out
$\overline{\text{SS5}}$	—	PPS	PPS	PPS	I/O	ST	SPI5 Slave Synchronization Or Frame Pulse I/O
Serial Peripheral Interface 6							
SCK6	—	48	A32	70	I/O	ST	SPI6 Synchronous Serial Clock Input/Output
SDI6	—	PPS	PPS	PPS	I	ST	SPI6 Data In
SDO6	—	PPS	PPS	PPS	O	—	SPI6 Data Out
$\overline{\text{SS6}}$	—	PPS	PPS	PPS	I/O	ST	SPI6 Slave Synchronization Or Frame Pulse I/O

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-13: EBI PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
$\overline{\text{EBIOE}}$	—	9	A7	13	O	—	External Bus Interface Output Enable
EBIRDY1	—	60	B34	86	I	ST	External Bus Interface Ready Input
EBIRDY2	—	58	A39	84	I	ST	
EBIRDY3	—	57	B45	116	I	ST	
$\overline{\text{EBIRP}}$	—	—	—	45	O	—	External Bus Interface Flash Reset Pin
$\overline{\text{EBIWE}}$	—	8	B5	12	O	—	External Bus Interface Write Enable

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

2.4 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For more information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available from the Microchip web site.

- *"Using MPLAB® ICD 3"* (poster) (DS50001765)
- *"MPLAB® ICD 3 Design Advisory"* (DS50001764)
- *"MPLAB® REAL ICE™ In-Circuit Debugger User's Guide" (*DS50001616)
- *"Using MPLAB® REAL ICE™ Emulator"* (poster) (DS50001749)

2.5 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input voltage low (V_{IL}) requirements.

2.6 Trace

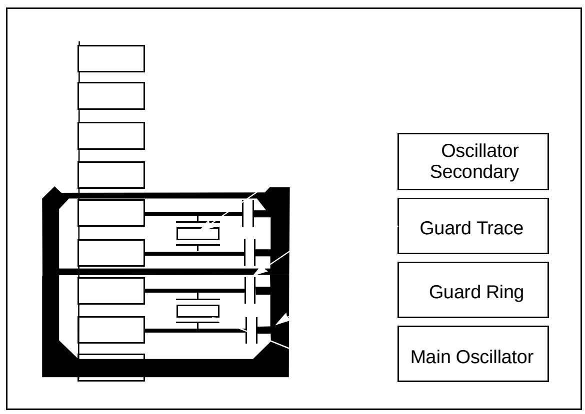
The trace pins can be connected to a hardware trace-enabled programmer to provide a compressed real-time instruction trace. When used for trace, the TRD3, TRD2, TRD1, TRD0 and TRCLK pins should be dedicated for this use. The trace hardware requires a 22 Ohm series resistor between the trace pins and the trace connector.

2.7 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT



2.8 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

Alternatively, inputs can be reserved by connecting the pin to V_{SS} through a 1k to 10k resistor and configuring the pin as an input.

TABLE 4-15: SYSTEM BUS TARGET 7 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
9C20	SBT7ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
9C24	SBT7ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
9C28	SBT7ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9C30	SBT7ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9C38	SBT7ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9C40	SBT7REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9C50	SBT7RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9C58	SBT7WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9C60	SBT7REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9C70	SBT7RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9C78	SBT7WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name[1]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
01F0	IPC11	31:16	—	—	—	ADCDC2IP<2:0>			ADCDC2IS<1:0>		—	—	—	ADCDC1IP<2:0>			ADCDC1IS<1:0>		0000
		15:0	—	—	—	ADCFIFOIP<2:0>			ADCFIFOIS<1:0>		—	—	—	ADCIP<2:0>			ADCIS<1:0>		0000
0200	IPC12	31:16	—	—	—	ADCDC6IP<2:0>			ADCDC6IS<1:0>		—	—	—	ADCDC5IP<2:0>			ADCDC5IS<1:0>		0000
		15:0	—	—	—	ADCDC4IP<2:0>			ADCDC4IS<1:0>		—	—	—	ADCDC3IP<2:0>			ADCDC3IS<1:0>		0000
0210	IPC13	31:16	—	—	—	ADCDF4IP<2:0>			ADCDF4IS<1:0>		—	—	—	ADCDF3IP<2:0>			ADCDF3IS<1:0>		0000
		15:0	—	—	—	ADCDF2IP<2:0>			ADCDF2IS<1:0>		—	—	—	ADCDF1IP<2:0>			ADCDF1IS<1:0>		0000
0220	IPC14	31:16	—	—	—	ADCD0IP<2:0>			ADCD0IS<1:0>		—	—	—	ADCDFLTIP<2:0>			ADCDFLTIS<1:0>		0000
		15:0	—	—	—	ADCDF6IP<2:0>			ADCDF6IS<1:0>		—	—	—	ADCDF5IP<2:0>			ADCDF5IS<1:0>		0000
0230	IPC15	31:16	—	—	—	ADCD4IP<2:0>			ADCD4IS<1:0>		—	—	—	ADCD3IP<2:0>			ADCD3IS<1:0>		0000
		15:0	—	—	—	ADCD2IP<2:0>			ADCD2IS<1:0>		—	—	—	ADCD1IP<2:0>			ADCD1IS<1:0>		0000
0240	IPC16	31:16	—	—	—	ADCD8IP<2:0>			ADCD8IS<1:0>		—	—	—	ADCD7IP<2:0>			ADCD7IS<1:0>		0000
		15:0	—	—	—	ADCD6IP<2:0>			ADCD6IS<1:0>		—	—	—	ADCD5IP<2:0>			ADCD5IS<1:0>		0000
0250	IPC17	31:16	—	—	—	ADCD12IP<2:0>			ADCD12IS<1:0>		—	—	—	ADCD11IP<2:0>			ADCD11IS<1:0>		0000
		15:0	—	—	—	ADCD10IP<2:0>			ADCD10IS<1:0>		—	—	—	ADCD9IP<2:0>			ADCD9IS<1:0>		0000
0260	IPC18	31:16	—	—	—	ADCD16IP<2:0>			ADCD16IS<1:0>		—	—	—	ADCD15IP<2:0>			ADCD15IS<1:0>		0000
		15:0	—	—	—	ADCD14IP<2:0>			ADCD14IS<1:0>		—	—	—	ADCD13IP<2:0>			ADCD13IS<1:0>		0000
0270	IPC19	31:16	—	—	—	ADCD20IP<2:0>[2]			ADCD20IS<1:0>[2]		—	—	—	ADCD19IP<2:0>[2]			ADCD19IS<1:0>[2]		0000
		15:0	—	—	—	ADCD18IP<2:0>			ADCD18IS<1:0>		—	—	—	ADCD17IP<2:0>			ADCD17IS<1:0>		0000
0280	IPC20	31:16	—	—	—	ADCD24IP<2:0>[2]			ADCD24IS<1:0>[2]		—	—	—	ADCD23IP<2:0>[2]			ADCD23IS<1:0>[2]		0000
		15:0	—	—	—	ADCD22IP<2:0>[2]			ADCD22IS<1:0>[2]		—	—	—	ADCD21IP<2:0>[2]			ADCD21IS<1:0>[2]		0000
0290	IPC21	31:16	—	—	—	ADCD28IP<2:0>[2]			ADCD28IS<1:0>[2]		—	—	—	ADCD27IP<2:0>[2]			ADCD27IS<1:0>[2]		0000
		15:0	—	—	—	ADCD26IP<2:0>[2]			ADCD26IS<1:0>[2]		—	—	—	ADCD25IP<2:0>[2]			ADCD25IS<1:0>[2]		0000
02A0	IPC22	31:16	—	—	—	ADCD32IP<2:0>[2]			ADCD32IS<1:0>[2]		—	—	—	ADCD31IP<2:0>[2]			ADCD31IS<1:0>[2]		0000
		15:0	—	—	—	ADCD30IP<2:0>[2]			ADCD30IS<1:0>[2]		—	—	—	ADCD29IP<2:0>[2]			ADCD29IS<1:0>[2]		0000
02B0	IPC23	31:16	—	—	—	ADCD36IP<2:0>[2,4]			ADCD36IS<1:0>[2,4]		—	—	—	ADCD35IP<2:0>[2,4]			ADCD35IS<1:0>[2,4]		0000
		15:0	—	—	—	ADCD34IP<2:0>[2]			ADCD34IS<1:0>[2]		—	—	—	ADCD33IP<2:0>[2]			ADCD33IS<1:0>[2]		0000
02C0	IPC24	31:16	—	—	—	ADCD40IP<2:0>[2,4]			ADCD40IS<1:0>[2,4]		—	—	—	ADCD39IP<2:0>[2,4]			ADCD39IS<1:0>[2,4]		0000
		15:0	—	—	—	ADCD38IP<2:0>[2,4]			ADCD38IS<1:0>[2,4]		—	—	—	ADCD37IP<2:0>[2,4]			ADCD37IS<1:0>[2,4]		0000
02D0	IPC25	31:16	—	—	—	ADCD44IP<2:0>			ADCD44IS<1:0>		—	—	—	ADCD43IP<2:0>			ADCD43IS<1:0>		0000
		15:0	—	—	—	ADCD42IP<2:0>[2,4]			ADCD42IS<1:0>[2,4]		—	—	—	ADCD41IP<2:0>[2,4]			ADCD41IS<1:0>[2,4]		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

2: This bit or register is not available on 64-pin devices.

3: This bit or register is not available on devices without a CAN module.

4: This bit or register is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.

7: This bit or register is not available on devices without a Crypto module.

8: This bit or register is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
07A4	OFF153	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07A8	OFF154	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07AC	OFF155	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B0	OFF156	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B4	OFF157	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B8	OFF158	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07BC	OFF159	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C0	OFF160	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C4	OFF161	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C8	OFF162	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07CC	OFF163	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07D0	OFF164	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07D4	OFF165	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07D8	OFF166	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07DC	OFF167	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

2: This bit or register is not available on 64-pin devices.

3: This bit or register is not available on devices without a CAN module.

4: This bit or register is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.

7: This bit or register is not available on devices without a Crypto module.

8: This bit or register is not available on 124-pin devices.

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI7SS<3:0>(1)				PRI6SS<3:0>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI5SS<3:0>(1)				PRI4SS<3:0>(1)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI3SS<3:0>				PRI2SS<3:0>(1)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	PRI1SS<3:0>(1)				—	—	—	SS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **PRI7SS<3:0>:** Interrupt with Priority Level 7 Shadow Set bits(1)

`1xxx` = Reserved (by default, an interrupt with a priority level of 7 uses Shadow Set 0)
`0111` = Interrupt with a priority level of 7 uses Shadow Set 7
`0110` = Interrupt with a priority level of 7 uses Shadow Set 6
•
•
•
`0001` = Interrupt with a priority level of 7 uses Shadow Set 1
`0000` = Interrupt with a priority level of 7 uses Shadow Set 0

bit 27-24 **PRI6SS<3:0>:** Interrupt with Priority Level 6 Shadow Set bits(1)

`1xxx` = Reserved (by default, an interrupt with a priority level of 6 uses Shadow Set 0)
`0111` = Interrupt with a priority level of 6 uses Shadow Set 7
`0110` = Interrupt with a priority level of 6 uses Shadow Set 6
•
•
•
`0001` = Interrupt with a priority level of 6 uses Shadow Set 1
`0000` = Interrupt with a priority level of 6 uses Shadow Set 0

bit 23-20 **PRI5SS<3:0>:** Interrupt with Priority Level 5 Shadow Set bits(1)

`1xxx` = Reserved (by default, an interrupt with a priority level of 5 uses Shadow Set 0)
`0111` = Interrupt with a priority level of 5 uses Shadow Set 7
`0110` = Interrupt with a priority level of 5 uses Shadow Set 6
•
•
•
`0001` = Interrupt with a priority level of 5 uses Shadow Set 1
`0000` = Interrupt with a priority level of 5 uses Shadow Set 0

bit 19-16 **PRI4SS<3:0>:** Interrupt with Priority Level 4 Shadow Set bits(1)

`1xxx` = Reserved (by default, an interrupt with a priority level of 4 uses Shadow Set 0)
`0111` = Interrupt with a priority level of 4 uses Shadow Set 7
`0110` = Interrupt with a priority level of 4 uses Shadow Set 6
•
•
•
`0001` = Interrupt with a priority level of 4 uses Shadow Set 1
`0000` = Interrupt with a priority level of 4 uses Shadow Set 0

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = `0`.

REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28-26 **IP3<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as ‘0’

bit 20-18 **IP2<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as ‘0’

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-2 for the exact bit definitions.

REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RXDPB	RXFIFOSZ<3:0>			
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TXDPB	TXFIFOSZ<3:0>			
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	TXEDMA	RXEDMA
7:0	R-1	R-0	R-0	R-0	R-0	R-0	R/W-0, HC	R/W-0
	BDEV	FSDEV	LSDEV	VBUS<1:0>		HOSTMODE	HOSTREQ	SESSION

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28 **RXDPB:** RX Endpoint Double-packet Buffering Control bit
1 = Double-packet buffer is supported. This doubles the size set in RXFIFOSZ.
0 = Double-packet buffer is not supported

bit 27-24 **RXFIFOSZ<3:0>:** RX Endpoint FIFO Packet Size bits

The maximum packet size to allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)

1111 = Reserved
•
•
•
1010 = Reserved
1001 = 4096 bytes
1000 = 2048 bytes
0111 = 1024 bytes
0110 = 512 bytes
0101 = 256 bytes
0100 = 128 bytes
0011 = 64 bytes
0010 = 32 bytes
0001 = 16 bytes
0000 = 8 bytes

bit 23-21 **Unimplemented:** Read as ‘0’

bit 20 **TXDPB:** TX Endpoint Double-packet Buffering Control bit
1 = Double-packet buffer is supported. This doubles the size set in TXFIFOSZ.
0 = Double-packet buffer is not supported

TABLE 12-6: PORTC REGISTER MAP FOR 100-PIN, 124-PIN, AND 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name[(1)]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	ANSELC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	ANSC4	ANSC3	ANSC2	ANSC1	—	001E
0210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	TRISC4	TRISC3	TRISC2	TRISC1	—	F01E
0220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	RC4	RC3	RC2	RC1	—	xxxx
0230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	LATC4	LATC3	LATC2	LATC1	—	xxxx
0240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	ODCC4	ODCC3	ODCC2	ODCC1	—	0000
0250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUC15	CNPUC14	CNPUC13	CNPUC12	—	—	—	—	—	—	—	CNPUC4	CNPUC3	CNPUC2	CNPUC1	—	0000
0260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDC15	CNPDC14	CNPDC13	CNPDC12	—	—	—	—	—	—	—	CNPDC4	CNPDC3	CNPDC2	CNPDC1	—	0000
0270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0280	CNENC	31:16	—	—		—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNENC15	CNENC14	CNENC13	CNENC12								CNENC4	CNENC3	CNENC2	CNENC1	—	0000
0290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATC15	CNSTATC14	CNSTATC13	CNSTATC12	—	—	—	—	—	—	—	CNSTATC4	CNSTATC3	CNSTATC2	CNSTATC1	—	0000
02A0	CNNEC	31:16	—	—		—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEC15	CNNEC14	CNNEC13	CNNEC12	—	—	—	—	—	—	—	CNNEC4	CNNEC3	CNNEC2	CNNEC1	—	0000
02B0	CNFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFC15	CNFC14	CNFC13	CNFC12	—	—	—	—	—	—	—	CNFC4	CNFC3	CNFC2	CNFC1	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

bit 2 **TSYNC:** Timer External Clock Input Synchronization Selection bit

When TCS = 1:
1 = External clock input is synchronized
0 = External clock input is not synchronized

When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer Clock Source Select bit

1 = External clock from T1CKI pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

REGISTER 23-3: PMADDR: PARALLEL PORT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CS2(1)	CS1(3)	ADDR<13:8>					
	ADDR15(2)	ADDR14(4)						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **CS2:** Chip Select 2 bit(1)
- 1 = Chip Select 2 is active
- 0 = Chip Select 2 is inactive

bit 15 **ADDR<15>:** Target Address bit 15(2)

bit 14 **CS1:** Chip Select 1 bit(3)
- 1 = Chip Select 1 is active
- 0 = Chip Select 1 is inactive

bit 14 **ADDR<14>:** Target Address bit 14(4)

bit 13-0 **ADDR<13:0>:** Address bits

Note 1: When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.
2: When the CSF<1:0> bits (PMCON<7:6>) = 00.
3: When the CSF<1:0> bits (PMCON<7:6>) = 10.
4: When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

Note: If the DUALBUF bit (PMCON<17>) = 0, the bits in this register control both read and write target addressing. If the DUALBUF bit = 1, the bits in this register are not used. In this instance, use the PMRADDR register for Read operations and the PMWADDR register for Write operations.

REGISTER 26-7: CEINTEN: CRYPTO ENGINE INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	AREIE	PKTIE	BDPIE	PENDIE(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as ‘0’

bit 3 **AREIE:** Access Response Error Interrupt Enable bit
1 = Access response error interrupts are enabled
0 = Access response error interrupts are not enabled

bit 2 **PKTIE:** DMA Packet Completion Interrupt Enable bit
1 = DMA packet completion interrupts are enabled
0 = DMA packet completion interrupts are not enabled

bit 1 **BDPIE:** DMA Buffer Descriptor Processor Interrupt Enable bit
1 = BDP interrupts are enabled
0 = BDP interrupts are not enabled

bit 0 **PENDIE:** Master Interrupt Enable bit(1)
1 = Crypto Engine interrupts are enabled
0 = Crypto Engine interrupts are not enabled

Note 1: The PENDIE bit is a global enable bit and must be enabled together with the other interrupts desired.

REGISTER 28-7: ADCIMCON3: ADC INPUT MODE CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DIFF44	SIGN44
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF43	SIGN43	DIFF42(2)	SIGN42(2)	DIFF41(2)	SIGN41(2)	DIFF40(2)	SIGN40(2)
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF39(2)	SIGN39(2)	DIFF38(2)	SIGN38(2)	DIFF37(2)	SIGN37(2)	DIFF36(2)	SIGN36(2)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF35(2)	SIGN35(2)	DIFF34(1)	SIGN34(1)	DIFF33(1)	SIGN33(1)	DIFF32(1)	SIGN32(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as ‘0’

bit 25 **DIFF44:** AN44 Mode bit
1 = AN44 is using Differential mode
0 = AN44 is using Single-ended mode

bit 24 **SIGN44:** AN44 Signed Data Mode bit
1 = AN44 is using Signed Data mode
0 = AN44 is using Unsigned Data mode

bit 23 **DIFF43:** AN43 Mode bit
1 = AN43 is using Differential mode
0 = AN43 is using Single-ended mode

bit 22 **SIGN43:** AN43 Signed Data Mode bit
1 = AN43 is using Signed Data mode
0 = AN43 is using Unsigned Data mode

bit 21 **DIFF42:** AN42 Mode bit(2)
1 = AN42 is using Differential mode
0 = AN42 is using Single-ended mode

bit 20 **SIGN42:** AN42 Signed Data Mode bit(2)
1 = AN42 is using Signed Data mode
0 = AN42 is using Unsigned Data mode

bit 19 **DIFF41:** AN41 Mode bit(2)
1 = AN41 is using Differential mode
0 = AN41 is using Single-ended mode

bit 18 **SIGN41:** AN41 Signed Data Mode bit(2)
1 = AN41 is using Signed Data mode
0 = AN41 is using Unsigned Data mode

bit 17 **DIFF40:** AN40 Mode bit(2)
1 = AN40 is using Differential mode
0 = AN40 is using Single-ended mode

Note 1: This bit is not available on 64-pin devices.
2: This bit is not available on 64-pin and 100-pin devices.

REGISTER 28-17: ADCTRG1: ADC TRIGGER SOURCE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC3<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC2<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC1<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC0<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28-24 **TRGSRC3<4:0>:** Trigger Source for Conversion of Analog Input AN3 Select bits
11111 = Reserved
•
•
•
01101 = Reserved
01100 = Comparator 2 (COUT)
01011 = Comparator 1 (COUT)
01010 = OCMP5
01001 = OCMP3
01000 = OCMP1
00111 = TMR5 match
00110 = TMR3 match
00101 = TMR1 match
00100 = INT0 External interrupt
00011 = STRIG
00010 = Global level software trigger (GLSWTRG)
00001 = Global software edge Trigger (GSWTRG)
00000 = No Trigger

For STRIG, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSS*x* registers.

bit 23-21 **Unimplemented:** Read as ‘0’

bit 20-16 **TRGSRC2<4:0>:** Trigger Source for Conversion of Analog Input AN2 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **TRGSRC1<4:0>:** Trigger Source for Conversion of Analog Input AN1 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **TRGSRC0<4:0>:** Trigger Source for Conversion of Analog Input AN0 Select bits
See bits 28-24 for bit value definitions.

REGISTER 30-24: EMAC1CFG2: ETHERNET CONTROLLER MAC CONFIGURATION 2 REGISTER

bit 6 **VLANPAD:** VLAN Pad Enable bit[1,2]

1 = The MAC will pad all short frames to 64 bytes and append a valid CRC
0 = The MAC does not perform padding of short frames

bit 5 **PADENABLE:** Pad/CRC Enable bit[1,3]

1 = The MAC will pad all short frames
0 = The frames presented to the MAC have a valid length

bit 4 **CRCENABLE:** CRC Enable1 bit

1 = The MAC will append a CRC to every frame whether padding was required or not. Must be set if the PADENABLE bit is set.
0 = The frames presented to the MAC have a valid CRC

bit 3 **DELAYCRC:** Delayed CRC bit

This bit determines the number of bytes, if any, of proprietary header information that exist on the front of the IEEE 802.3 frames.

1 = Four bytes of header (ignored by the CRC function)
0 = No proprietary header

bit 2 **HUGEFRM:** Huge Frame enable bit

1 = Frames of any length are transmitted and received
0 = Huge frames are not allowed for receive or transmit

bit 1 **LENGTHCK:** Frame Length checking bit

1 = Both transmit and receive frame lengths are compared to the Length/Type field. If the Length/Type field represents a length then the check is performed. Mismatches are reported on the transmit/receive statistics vector.
0 = Length/Type field check is not performed

bit 0 **FULLDPLX:** Full-Duplex Operation bit

1 = The MAC operates in Full-Duplex mode
0 = The MAC operates in Half-Duplex mode

Note 1: Table 30-6 provides a description of the pad function based on the configuration of this register.
2: This bit is ignored if the PADENABLE bit is cleared.
3: This bit is used in conjunction with the AUTOPAD and VLANPAD bits.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware

TABLE 30-6: PAD OPERATION

Type	AUTOPAD	VLANPAD	PADENABLE	Action
Any	x	x	0	No pad, check CRC
Any	0	0	1	Pad to 60 Bytes, append CRC
Any	x	1	1	Pad to 64 Bytes, append CRC
Any	1	0	1	If untagged: Pad to 60 Bytes, append CRC If VLAN tagged: Pad to 64 Bytes, append CRC

TABLE 37-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	**Supply Voltage (Note 1)**	2.1	—	3.6	V	—
DC12	VDR	**RAM Data Retention Voltage (Note 2)**	2.0	—	—	V	—
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal **(Note 3)**	1.75	—	—	V	—
DC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	0.000011	—	1.1	V/μs	300 ms to 3 μs @ 3.3V

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is guaranteed, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 37-5 for BOR values.

2: This is the limit to which VDD can be lowered without losing RAM data.

3: This is the limit to which VDD must be lowered to ensure Power-on Reset.

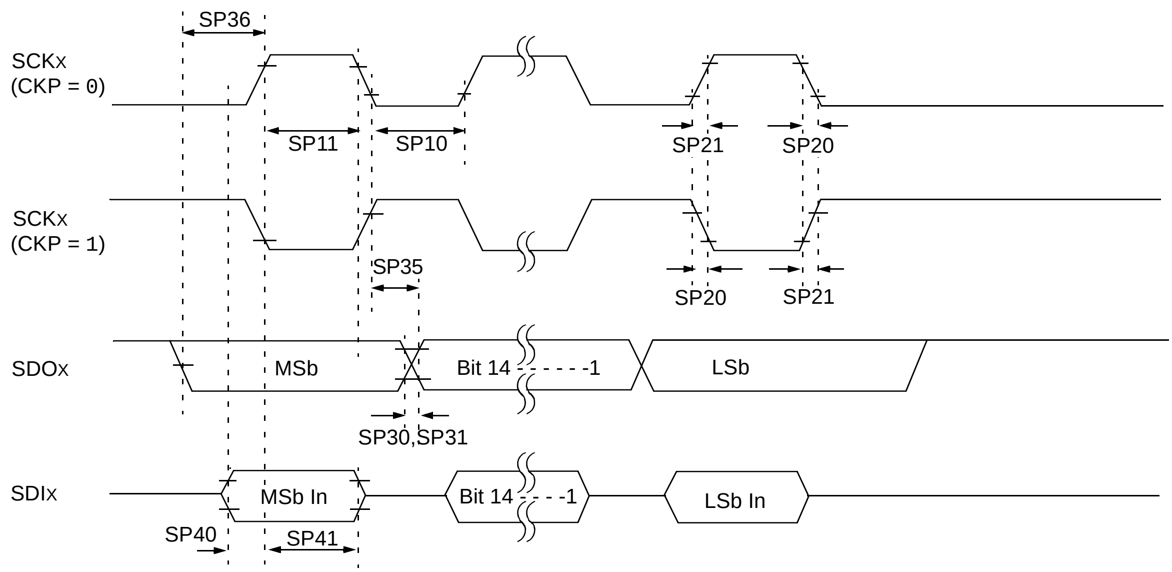
TABLE 37-5: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.(1)**	**Typical**	**Max.**	**Units**	**Conditions**
BO10	VBOR	BOR Event on VDD transition high-to-low **(Note 2)**	1.88	—	2.02	V	—

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN.

FIGURE 37-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 37-1 for load conditions.

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