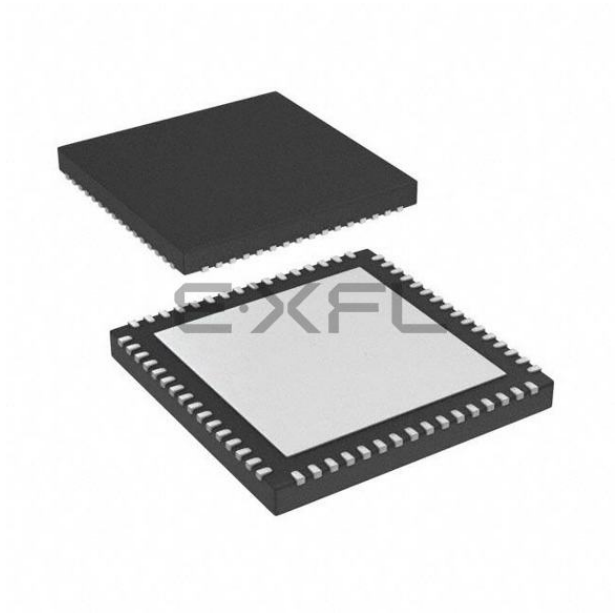
# Microchip Technology - PIC32MZ1024EFE064-I/MR Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M-Class |
| Core Size | 32-Bit Single-Core |
| Speed | 200MHz |
| Connectivity | Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 46 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.1V ~ 3.6V |
| Data Converters | A/D 24x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-QFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efe064-i-mr |

**TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | 124-pin VTLA | 144-pin TQFP/ LQFP | | | |
| **PORTA** | | | | | | | |
| RA0 | — | 17 | A11 | 22 | I/O | ST | PORTA is a bidirectional I/O port |
| RA1 | — | 38 | B21 | 56 | I/O | ST | |
| RA2 | — | 59 | A41 | 85 | I/O | ST | |
| RA3 | — | 60 | B34 | 86 | I/O | ST | |
| RA4 | — | 61 | A42 | 87 | I/O | ST | |
| RA5 | — | 2 | B1 | 2 | I/O | ST | |
| RA6 | — | 89 | A61 | 129 | I/O | ST | |
| RA7 | — | 90 | B51 | 130 | I/O | ST | |
| RA9 | — | 28 | B15 | 39 | I/O | ST | |
| RA10 | — | 29 | A20 | 40 | I/O | ST | |
| RA14 | — | 66 | B37 | 95 | I/O | ST | |
| RA15 | — | 67 | A45 | 96 | I/O | ST | |
| **PORTB** | | | | | | | |
| RB0 | 16 | 25 | A18 | 36 | I/O | ST | PORTB is a bidirectional I/O port |
| RB1 | 15 | 24 | A17 | 35 | I/O | ST | |
| RB2 | 14 | 23 | A16 | 34 | I/O | ST | |
| RB3 | 13 | 22 | A14 | 31 | I/O | ST | |
| RB4 | 12 | 21 | A13 | 26 | I/O | ST | |
| RB5 | 11 | 20 | B11 | 25 | I/O | ST | |
| RB6 | 17 | 26 | B14 | 37 | I/O | ST | |
| RB7 | 18 | 27 | A19 | 38 | I/O | ST | |
| RB8 | 21 | 32 | B18 | 47 | I/O | ST | |
| RB9 | 22 | 33 | A23 | 48 | I/O | ST | |
| RB10 | 23 | 34 | B19 | 49 | I/O | ST | |
| RB11 | 24 | 35 | A24 | 50 | I/O | ST | |
| RB12 | 27 | 41 | A27 | 59 | I/O | ST | |
| RB13 | 28 | 42 | B23 | 60 | I/O | ST | |
| RB14 | 29 | 43 | A28 | 61 | I/O | ST | |
| RB15 | 30 | 44 | B24 | 62 | I/O | ST | |
| **PORTC** | | | | | | | |
| RC1 | — | 6 | B3 | 6 | I/O | ST | PORTC is a bidirectional I/O port |
| RC2 | — | 7 | A6 | 11 | I/O | ST | |
| RC3 | — | 8 | B5 | 12 | I/O | ST | |
| RC4 | — | 9 | A7 | 13 | I/O | ST | |
| RC12 | 31 | 49 | B28 | 71 | I/O | ST | |
| RC13 | 47 | 72 | B41 | 105 | I/O | ST | |
| RC14 | 48 | 73 | A49 | 106 | I/O | ST | |
| RC15 | 32 | 50 | A33 | 72 | I/O | ST | |

**Legend:** CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

**REGISTER 3-8: FEXR: FLOATING POINT EXCEPTIONS STATUS REGISTER; CP1 REGISTER 26**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-x | R/W-x |
| | — | — | — | — | — | — | CAUSE<5:4> | |
| | | | | | | | E | V |
| 15:8 | R/W-x | R/W-x | R/W-x | U-0 | U-0 | U-0 | U-0 | U-0 |
| | CAUSE<3:0> | | | | — | — | — | — |
| | Z | O | U | I | | | | |
| 7:0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | U-0 | U-0 |
| | — | FLAGS<4:0> | | | | | — | — |
| | | V | Z | O | U | I | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-18 **Unimplemented:** Read as '0'

bit 17-12 **CAUSE<5:0>:** FPU Exception Cause bits
These bits indicated the exception conditions that arise during execution of an FPU arithmetic instruction.

bit 17 **E:** Unimplemented Operation bit

bit 16 **V:** Invalid Operation bit

bit 15 **Z:** Divide-by-Zero bit

bit 14 **O:** Overflow bit

bit 13 **U:** Underflow bit

bit 12 **I:** Inexact bit

bit 11-7 **Unimplemented:** Read as '0'

bit 6-2 **FLAGS<4:0>:** FPU Flags bits
These bits show any exception conditions that have occurred for completed instructions since the flag was last reset by software.

bit 6 **V:** Invalid Operation bit

bit 4 **Z:** Divide-by-Zero bit

bit 4 **O:** Overflow bit

bit 3 **U:** Underflow bit

bit 2 **I:** Inexact bit

bit 1-0 **Unimplemented:** Read as '0'

**TABLE 4-6: SYSTEM BUS TARGETS AND ASSOCIATED PROTECTION REGISTERS**

| Target Number | Target Description[5] | SBTxREGy Register | | | | | | | SBTxRDy Register | | SBTxWRy Register | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Name | Region Base (BASE<21:0>) (see Note 2) | Physical Start Address | Region Size (SIZE<4:0>) (see Note 3) | Region Size | Priority (PRI) | Priority Level | Name | Read Permission (GROUP3, GROUP2, GROUP1, GROUP0) | Name | Write Permission (GROUP3, GROUP2, GROUP1, GROUP0) |
| 0 | System Bus | SBT0REG0 | R | 0x1F8F0000 | R | 64 KB | — | 0 | SBT0RD0 | R/W[1] | SBT0WR0 | R/W[1] |
| | | SBT0REG1 | R | 0x1F8F8000 | R | 32 KB | — | 3 | SBT0RD1 | R/W[1] | SBT0WR1 | R/W[1] |
| 1 | **Flash Memory[6]:**<br>Program Flash<br>Boot Flash<br>Prefetch Module | SBT1REG0 | R | 0x1D000000 | R[4] | R[4] | — | 0 | SBT1RD0 | R/W[1] | SBT1WR0 | 0, 0, 0, 0 |
| | | SBT1REG2 | R | 0x1F8E0000 | R | 4 KB | 1 | 2 | SBT1RD2 | R/W[1] | SBT1WR2 | R/W[1] |
| | | SBT1REG3 | R/W | R/W | R/W | R/W | 1 | 2 | SBT1RD3 | R/W[1] | SBT1WR3 | 0, 0, 0, 0 |
| | | SBT1REG4 | R/W | R/W | R/W | R/W | 1 | 2 | SBT1RD4 | R/W[1] | SBT1WR4 | 0, 0, 0, 0 |
| | | SBT1REG5 | R/W | R/W | R/W | R/W | 1 | 2 | SBT1RD5 | R/W[1] | SBT1WR5 | 0, 0, 0, 0 |
| | | SBT1REG6 | R/W | R/W | R/W | R/W | 1 | 2 | SBT1RD6 | R/W[1] | SBT1WR6 | 0, 0, 0, 0 |
| | | SBT1REG7 | R/W | R/W | R/W | R/W | 0 | 1 | SBT1RD7 | R/W[1] | SBT1WR7 | 0, 0, 0, 0 |
| | | SBT1REG8 | R/W | R/W | R/W | R/W | 0 | 1 | SBT1RD8 | R/W[1] | SBT1WR8 | 0, 0, 0, 0 |
| 2 | RAM Bank 1 Memory | SBT2REG0 | R | 0x00000000 | R[4] | R[4] | — | 0 | SBT2RD0 | R/W[1] | SBT2WR0 | R/W[1] |
| | | SBT2REG1 | R/W | R/W | R/W | R/W | — | 3 | SBT2RD1 | R/W[1] | SBT2WR1 | R/W[1] |
| | | SBT2REG2 | R/W | R/W | R/W | R/W | 0 | 1 | SBT2RD2 | R/W[1] | SBT2WR2 | R/W[1] |
| 3 | RAM Bank 2 Memory | SBT3REG0 | R[4] | R[4] | R[4] | R[4] | — | 0 | SBT3RD0 | R/W[1] | SBT3WR0 | R/W[1] |
| | | SBT3REG1 | R/W | R/W | R/W | R/W | — | 3 | SBT3RD1 | R/W[1] | SBT3WR1 | R/W[1] |
| | | SBT3REG2 | R/W | R/W | R/W | R/W | 0 | 1 | SBT3RD2 | R/W[1] | SBT3WR2 | R/W[1] |
| 4 | External Memory via EBI and EBI Module[6] | SBT4REG0 | R | 0x20000000 | R | 64 MB | — | 0 | SBT4RD0 | R/W[1] | SBT4WR0 | R/W[1] |
| | | SBT4REG2 | R | 0x1F8E1000 | R | 4 KB | 0 | 1 | SBT4RD2 | R/W[1] | SBT4WR2 | R/W[1] |
| 5 | **Peripheral Set 1:**<br>System Control<br>Flash Control<br>DMT/WDT<br>RTCC<br>CVR<br>PPS Input<br>PPS Output<br>Interrupts<br>DMA | SBT5REG0 | R | 0x1F800000 | R | 128 KB | — | 0 | SBT5RD0 | R/W[1] | SBT5WR0 | R/W[1] |
| | | SBT5REG1 | R/W | R/W | R/W | R/W | — | 3 | SBT5RD1 | R/W[1] | SBT5WR1 | R/W[1] |
| | | SBT5REG2 | R/W | R/W | R/W | R/W | 0 | 1 | SBT5RD2 | R/W[1] | SBT5WR2 | R/W[1] |

**Legend:** R = Read; R/W = Read/Write; 'x' in a register name = 0-13; 'y' in a register name = 0-8.

**Note 1:** Reset values for these bits are '0', '1', '1', '1', respectively.

**2:** The BASE<21:0> bits must be set to the corresponding Physical Address and right shifted by 10 bits. For Read-only bits, this value is set by hardware on Reset.

**3:** The SIZE<4:0> bits must be set to the corresponding Region Size, based on the following formula: Region Size = $2^{(SIZE-1)}$ x 1024 bytes. For read-only bits, this value is set by hardware on Reset.

**4:** Refer to the Device Memory Maps (Figure 4-1 through Figure 4-4) for specific device memory sizes and start addresses.

**5:** See Table 4-1for information on specific target memory size and start addresses.

**6:** The SBTxREG1 SFRs are reserved, and therefore, are not listed in this table for this target.

**TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION (CONTINUED)**

| Interrupt Source(1) | XC32 Vector Name | IRQ # | Vector # | Interrupt Bit Location | | | | Persistent Interrupt |
|---|---|---|---|---|---|---|---|---|
| | | | | Flag | Enable | Priority | Sub-priority | |
| Output Compare 4 | _OUTPUT_COMPARE_4_VECTOR | 22 | OFF022<17:1> | IFS0<22> | IEC0<22> | IPC5<20:18> | IPC5<17:16> | No |
| External Interrupt 4 | _EXTERNAL_4_VECTOR | 23 | OFF023<17:1> | IFS0<23> | IEC0<23> | IPC5<28:26> | IPC5<25:24> | No |
| Timer5 | _TIMER_5_VECTOR | 24 | OFF024<17:1> | IFS0<24> | IEC0<24> | IPC6<4:2> | IPC6<1:0> | No |
| Input Capture 5 Error | _INPUT_CAPTURE_5_ERROR_VECTOR | 25 | OFF025<17:1> | IFS0<25> | IEC0<25> | IPC6<12:10> | IPC6<9:8> | Yes |
| Input Capture 5 | _INPUT_CAPTURE_5_VECTOR | 26 | OFF026<17:1> | IFS0<26> | IEC0<26> | IPC6<20:18> | IPC6<17:16> | Yes |
| Output Compare 5 | _OUTPUT_COMPARE_5_VECTOR | 27 | OFF027<17:1> | IFS0<27> | IEC0<27> | IPC6<28:26> | IPC6<25:24> | No |
| Timer6 | _TIMER_6_VECTOR | 28 | OFF028<17:1> | IFS0<28> | IEC0<28> | IPC7<4:2> | IPC7<1:0> | No |
| Input Capture 6 Error | _INPUT_CAPTURE_6_ERROR_VECTOR | 29 | OFF029<17:1> | IFS0<29> | IEC0<29> | IPC7<12:10> | IPC7<9:8> | Yes |
| Input Capture 6 | _INPUT_CAPTURE_6_VECTOR | 30 | OFF030<17:1> | IFS0<30> | IEC0<30> | IPC7<20:18> | IPC7<17:16> | Yes |
| Output Compare 6 | _OUTPUT_COMPARE_6_VECTOR | 31 | OFF031<17:1> | IFS0<31> | IEC0<31> | IPC7<28:26> | IPC7<25:24> | No |
| Timer7 | _TIMER_7_VECTOR | 32 | OFF032<17:1> | IFS1<0> | IEC1<0> | IPC8<4:2> | IPC8<1:0> | No |
| Input Capture 7 Error | _INPUT_CAPTURE_7_ERROR_VECTOR | 33 | OFF033<17:1> | IFS1<1> | IEC1<1> | IPC8<12:10> | IPC8<9:8> | Yes |
| Input Capture 7 | _INPUT_CAPTURE_7_VECTOR | 34 | OFF034<17:1> | IFS1<2> | IEC1<2> | IPC8<20:18> | IPC8<17:16> | Yes |
| Output Compare 7 | _OUTPUT_COMPARE_7_VECTOR | 35 | OFF035<17:1> | IFS1<3> | IEC1<3> | IPC8<28:26> | IPC8<25:24> | No |
| Timer8 | _TIMER_8_VECTOR | 36 | OFF036<17:1> | IFS1<4> | IEC1<4> | IPC9<4:2> | IPC9<1:0> | No |
| Input Capture 8 Error | _INPUT_CAPTURE_8_ERROR_VECTOR | 37 | OFF037<17:1> | IFS1<5> | IEC1<5> | IPC9<12:10> | IPC9<9:8> | Yes |
| Input Capture 8 | _INPUT_CAPTURE_8_VECTOR | 38 | OFF038<17:1> | IFS1<6> | IEC1<6> | IPC9<20:18> | IPC9<17:16> | Yes |
| Output Compare 8 | _OUTPUT_COMPARE_8_VECTOR | 39 | OFF039<17:1> | IFS1<7> | IEC1<7> | IPC9<28:26> | IPC9<25:24> | No |
| Timer9 | _TIMER_9_VECTOR | 40 | OFF040<17:1> | IFS1<8> | IEC1<8> | IPC10<4:2> | IPC10<1:0> | No |
| Input Capture 9 Error | _INPUT_CAPTURE_9_ERROR_VECTOR | 41 | OFF041<17:1> | IFS1<9> | IEC1<9> | IPC10<12:10> | IPC10<9:8> | Yes |
| Input Capture 9 | _INPUT_CAPTURE_9_VECTOR | 42 | OFF042<17:1> | IFS1<10> | IEC1<10> | IPC10<20:18> | IPC10<17:16> | Yes |
| Output Compare 9 | _OUTPUT_COMPARE_9_VECTOR | 43 | OFF043<17:1> | IFS1<11> | IEC1<11> | IPC10<28:26> | IPC10<25:24> | No |
| ADC Global Interrupt | _ADC_VECTOR | 44 | OFF044<17:1> | IFS1<12> | IEC1<12> | IPC11<4:2> | IPC11<1:0> | Yes |
| ADC FIFO Data Ready Interrupt | _ADC_FIFO_VECTOR | 45 | OFF045<17:1> | IFS1<13> | IEC1<13> | IPC11<12:10> | IPC11<9:8> | Yes |
| ADC Digital Comparator 1 | _ADC_DC1_VECTOR | 46 | OFF046<17:1> | IFS1<14> | IEC1<14> | IPC11<20:18> | IPC11<17:16> | Yes |
| ADC Digital Comparator 2 | _ADC_DC2_VECTOR | 47 | OFF047<17:1> | IFS1<15> | IEC1<15> | IPC11<28:26> | IPC11<25:24> | Yes |
| ADC Digital Comparator 3 | _ADC_DC3_VECTOR | 48 | OFF048<17:1> | IFS1<16> | IEC1<16> | IPC12<4:2> | IPC12<1:0> | Yes |
| ADC Digital Comparator 4 | _ADC_DC4_VECTOR | 49 | OFF049<17:1> | IFS1<17> | IEC1<17> | IPC12<12:10> | IPC12<9:8> | Yes |

**Note 1:** Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MZ EF Family Features"** for the list of available peripherals.

**2:** This interrupt source is not available on 64-pin devices.

**3:** This interrupt source is not available on 100-pin devices.

**4:** This interrupt source is not available on 124-pin devices.

**TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)**

| Virtual Address (BF81_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 06B0 | OFF092(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06B4 | OFF093(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06B8 | OFF094(2,4) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06BC | OFF095(2,4) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06C0 | OFF096(2,4) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06C4 | OFF097(2,4) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06C8 | OFF098(2,4) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06CC | OFF099(2,4) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06D0 | OFF100(2,4) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06D4 | OFF101(2,4) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06D8 | OFF102 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06DC | OFF103 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06E0 | OFF104 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06E4 | OFF105 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 06E8 | OFF106 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
**2:** This bit or register is not available on 64-pin devices.
**3:** This bit or register is not available on devices without a CAN module.
**4:** This bit or register is not available on 100-pin devices.
**5:** Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
**6:** Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
**7:** This bit or register is not available on devices without a Crypto module.
**8:** This bit or register is not available on 124-pin devices.

**TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)**

| Virtual Address (BF81_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 081C | OFF183 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0820 | OFF184 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0824 | OFF185(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0828 | OFF186(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 082C | OFF187(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0830 | OFF188 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0834 | OFF189 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0838 | OFF190 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0840 | OFF192 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0844 | OFF193 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0848 | OFF194 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0850 | OFF196 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0858 | OFF198 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 085C | OFF199 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0860 | OFF200 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
**2:** This bit or register is not available on 64-pin devices.
**3:** This bit or register is not available on devices without a CAN module.
**4:** This bit or register is not available on 100-pin devices.
**5:** Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
**6:** Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
**7:** This bit or register is not available on devices without a Crypto module.
**8:** This bit or register is not available on 124-pin devices.

**REGISTER 10-5: DCRCDATA: DMA CRC DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **DCRCDATA<31:0>:** CRC Data Register bits

Writing to this register will seed the CRC generator. Reading from this register will return the current value of the CRC. Bits greater than PLEN will return '0' on any read.

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
Only the lower 16 bits contain IP header checksum information. The upper 16 bits are always '0'. Data written to this register is converted and read back in 1's complement form (i.e., current IP header checksum value).

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
Bits greater than PLEN will return '0' on any read.

**REGISTER 10-6: DCRCXOR: DMA CRCXOR ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **DCRCXOR<31:0>:** CRC XOR Register bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
This register is unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
1 = Enable the XOR input to the Shift register
0 = Disable the XOR input to the Shift register; data is shifted in directly from the previous stage in the register

**REGISTER 10-7: DCHxCON: DMA CHANNEL x CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHPIGN<7:0> | | | | | | | |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 |
| | CHBUSY | — | CHIPGNEN | — | CHPATLEN | — | — | CHCHNS(1) |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R-0 | R/W-0 | R/W-0 |
| | CHEN(2) | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **CHPIGN<7:0>:** Channel Register Data bits
Pattern Terminate mode:
Any byte matching these bits during a pattern match may be ignored during the pattern match determination when the CHPIGNEN bit is set. If a byte is read that is identical to this data byte, the pattern match logic will treat it as a "don't care" when the pattern matching logic is enabled and the CHPIGEN bit is set.

bit 23-16 **Unimplemented:** Read as '0'

bit 15 **CHBUSY:** Channel Busy bit
1 = Channel is active or has been enabled
0 = Channel is inactive or has been disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CHPIGNEN:** Enable Pattern Ignore Byte bit
1 = Treat any byte that matches the CHPIGN<7:0> bits as a "don't care" when pattern matching is enabled
0 = Disable this feature

bit 12 **Unimplemented:** Read as '0'

bit 11 **CHPATLEN:** Pattern Length bit
1 = 2 byte length
0 = 1 byte length

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **CHCHNS:** Chain Channel Selection bit(1)
1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 **CHEN:** Channel Enable bit(2)
1 = Channel is enabled
0 = Channel is disabled

bit 6 **CHAED:** Channel Allow Events If Disabled bit
1 = Channel start/abort events will be registered, even if the channel is disabled
0 = Channel start/abort events will be ignored if the channel is disabled

bit 5 **CHCHN:** Channel Chain Enable bit
1 = Allow channel to be chained
0 = Do not allow channel to be chained

**Note 1:** The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).

**2:** When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

## 12.5 I/O Ports Control Registers

**TABLE 12-4: PORTA REGISTER MAP FOR 100-PIN, 124-PIN, AND 144-PIN DEVICES ONLY**

| Virtual Address (BF86_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0000 | ANSELA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | ANSA10 | ANSA9 | — | — | — | ANSA5 | — | — | — | ANSA1 | ANSA0 | 0623 |
| 0010 | TRISA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISA15 | TRISA14 | — | — | — | TRISA10 | TRISA9 | — | TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | C6FF |
| 0020 | PORTA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RA15 | RA14 | — | — | — | RA10 | RA9 | — | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | xxxx |
| 0030 | LATA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATA15 | LATA14 | — | — | — | LATA10 | LATA9 | — | LATA7 | LATA6 | LATA5 | LATA4 | LATA3 | LATA2 | LATA1 | LATA0 | xxxx |
| 0040 | ODCA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCA15 | ODCA14 | — | — | — | ODCA10 | ODCA9 | — | ODCA7 | ODCA6 | ODCA5 | ODCA4 | ODCA3 | ODCA2 | ODCA1 | ODCA0 | 0000 |
| 0050 | CNPUA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPUA15 | CNPUA14 | — | — | — | CNPUA10 | CNPUA9 | — | CNPUA7 | CNPUA6 | CNPUA5 | CNPUA4 | CNPUA3 | CNPUA2 | CNPUA1 | CNPUA0 | 0000 |
| 0060 | CNPDA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPDA15 | CNPDA14 | — | — | — | CNPDA10 | CNPDA9 | — | CNPDA7 | CNPDA6 | CNPDA5 | CNPDA4 | CNPDA3 | CNPDA2 | CNPDA1 | CNPDA0 | 0000 |
| 0070 | CNCONA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | — | EDGEDETECT | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 0080 | CNENA | 31:16 | — | — | | | | — | — | | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNENA15 | CNENA14 | — | — | — | CNENA10 | CNENA9 | | CNENA7 | CNENA6 | CNENA5 | CNENA4 | CNENA3 | CNENA2 | CNENA1 | CNENA0 | 0000 |
| 0090 | CNSTATA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CN STATA15 | CN STATA14 | — | — | — | CN STATA10 | CN STATA9 | — | CN STATA7 | CN STATA6 | CN STATA5 | CN STATA4 | CN STATA3 | CN STATA2 | CN STATA1 | CN STATA0 | 0000 |
| 00A0 | CNNEA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNNEA15 | CNNEA14 | — | — | — | CNNEA10 | CNNEA9 | — | CNNEA7 | CNNEA6 | CNNEA5 | CNNEA4 | CNNEA3 | CNNEA2 | CNNEA1 | CNNEA0 | 0000 |
| 00B0 | CNFA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNFA15 | CNFA14 | — | — | — | CNFA10 | CNFA9 | — | CNFA7 | CNFA76 | CNFA5 | CNFA4 | CNFA3 | CNFA2 | CNFA71 | CNFA0 | 0000 |
| 00C0 | SRCON0A | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | SR0A7 | SR0A6 | — | — | — | — | — | — | 0000 |
| 00D0 | SRCON1A | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | SR1A7 | SR0A6 | — | — | — | — | — | — | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

## 16.1 Watchdog Timer Control Registers

**TABLE 16-1: WATCHDOG TIMER REGISTER MAP**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0800 | WDTCON(1) | 31:16 | WDTCLRKEY<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | ON | — | — | RUNDIV<4:0> | | | | | — | — | — | — | — | — | — | WDTWINEN | xx00 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **12.0 "I/O Ports"** for more information.

**REGISTER 19-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)**

bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (Framed SPI mode only)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock

bit 16 **ENHBUF:** Enhanced Buffer Enable bit(1)
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

bit 15 **ON:** SPI/$I^2S$ Module On bit
1 = SPI/$I^2S$ module is enabled
0 = SPI/$I^2S$ module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation when CPU enters in Idle mode
0 = Continue operation in Idle mode

bit 12 **DISSDO:** Disable SDOx pin bit(4)
1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register
0 = SDOx pin is controlled by the module

bit 11-10 **MODE<32,16>:** 32/16-Bit Communication Select bits

When AUDEN = 1:

| MODE32 | MODE16 | Communication |
|---|---|---|
| 1 | 1 | 24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame |
| 1 | 0 | 32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame |
| 0 | 1 | 16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame |
| 0 | 0 | 16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame |

When AUDEN = 0:

| MODE32 | MODE16 | Communication |
|---|---|---|
| 1 | x | 32-bit |
| 0 | 1 | 16-bit |
| 0 | 0 | 8-bit |

bit 9 **SMP:** SPI Data Input Sample Phase bit
Master mode (MSTEN = 1):
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
Slave mode (MSTEN = 0):
SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.

bit 8 **CKE:** SPI Clock Edge Select bit(2)
1 = Serial output data changes on transition from active clock state to Idle clock state (see CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see CKP bit)

bit 7 **SSEN:** Slave Select Enable (Slave mode) bit
1 = $\overline{SSx}$ pin is used for Slave mode
0 = SSx pin is not used for Slave mode, pin is controlled by the port function.

bit 6 **CKP:** Clock Polarity Select bit(3)
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

**Note 1:** This bit can only be written when the ON bit = 0. Refer to **Section 37.0 "Electrical Characteristics"** for maximum clock frequency requirements.

**2:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

**3:** When AUDEN = 1, the SPI/$I^2S$ module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

**4:** This bit present for legacy compatibility and is superseded by PPS functionality on these devices (see **Section 12.4 "Peripheral Pin Select (PPS)"** for more information).

**REGISTER 28-3: ADCCON3: ADC CONTROL REGISTER 3 (CONTINUED)**

bit 18 **DIGEN2:** ADC2 Digital Enable bit
1 = ADC2 is digital enabled
0 = ADC2 is digital disabled

bit 17 **DIGEN1:** ADC1 Digital Enable bit
1 = ADC1 is digital enabled
0 = ADC1 is digital disabled

bit 16 **DIGEN0:** ADC0 Digital Enable bit
1 = ADC0 is digital enabled
0 = ADC0 is digital disabled

bit 15-13 **VREFSEL<2:0>:** Voltage Reference (VREF) Input Selection bits

| VREFSEL<2:0> | ADREF+ | ADREF- |
|---|---|---|
| 1xx | Reserved; do not use | |
| 011 | External VREFH | External VREFL |
| 010 | AVDD | External VREFL |
| 001 | External VREFH | AVss |
| 000 | AVDD | AVss |

bit 12 **TRGSUSP:** Trigger Suspend bit
1 = Triggers are blocked from starting a new analog-to-digital conversion, but the ADC module is not disabled
0 = Triggers are not blocked

bit 11 **UPDIEN:** Update Ready Interrupt Enable bit
1 = Interrupt will be generated when the UPDRDY bit is set by hardware
0 = No interrupt is generated

bit 10 **UPDRDY:** ADC Update Ready Status bit
1 = ADC SFRs can be updated
0 = ADC SFRs cannot be updated

**Note:** This bit is only active while the TRGSUSP bit is set and there are no more running conversions of any ADC modules.

bit 9 **SAMP:** Class 2 and Class 3 Analog Input Sampling Enable bit**(1,2,3,4)**
1 = The ADC S&H amplifier is sampling
0 = The ADC S&H amplifier is holding

bit 8 **RQCNVRT:** Individual ADC Input Conversion Request bit
This bit and its associated ADINSEL<5:0> bits enable the user to individually request an analog-to-digital conversion of an analog input through software.
1 = Trigger the conversion of the selected ADC input as specified by the ADINSEL<5:0> bits
0 = Do not trigger the conversion

**Note:** This bit is automatically cleared in the next ADC clock cycle.

bit 7 **GLSWTRG:** Global Level Software Trigger bit
1 = Trigger conversion for ADC inputs that have selected the GLSWTRG bit as the trigger signal, either through the associated TRGSRC<4:0> bits in the ADCTRGx registers or through the STRGSRC<4:0> bits in the ADCCON1 register
0 = Do not trigger an analog-to-digital conversion

**Note 1:** The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit will cause settings of SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

**2:** The SAMP bit only connects Class 2 and Class 3 analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

**3:** The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion.

**4:** Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx<4:0> bits and STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

## 29.1 CAN Control Registers

**Note:** The 'i' shown in register names denotes CAN1 or CAN2.

**TABLE 29-1: CAN1 REGISTER SUMMARY FOR PIC32MZXXXXECF AND PIC32MZXXXXECH DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0000 | C1CON | 31:16 | — | — | — | — | ABAT | REQOP<2:0> | | | OPMOD<2:0> | | | CANCAP | — | — | — | — | 0480 |
| | | 15:0 | ON | — | SIDLE | — | CANBUSY | — | — | — | — | — | — | DNCNT<4:0> | | | | | 0000 |
| 0010 | C1CFG | 31:16 | — | — | — | — | — | — | — | — | — | WAKFIL | — | — | — | SEG2PH<2:0> | | | 0000 |
| | | 15:0 | SEG2PHTS | SAM | SEG1PH<2:0> | | | PRSEG<2:0> | | | SJW<1:0> | | BRP<5:0> | | | | | | 0000 |
| 0020 | C1INT | 31:16 | IVRIE | WAKIE | CERRIE | SERRIE | RBOVIE | — | — | — | — | — | — | — | MODIE | CTMRIE | RBIE | TBIE | 0000 |
| | | 15:0 | IVRIF | WAKIF | CERRIF | SERRIF | RBOVIF | — | — | — | — | — | — | — | MODIF | CTMRIF | RBIF | TBIF | 0000 |
| 0030 | C1VEC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | FILHIT<4:0> | | | | | — | ICODE<6:0> | | | | | | | 0040 |
| 0040 | C1TREC | 31:16 | — | — | — | — | — | — | — | — | — | — | TXBO | TXBP | RXBP | TXWARN | RXWARN | EWARN | 0000 |
| | | 15:0 | TERRCNT<7:0> | | | | | | | | RERRCNT<7:0> | | | | | | | | 0000 |
| 0050 | C1FSTAT | 31:16 | FIFOIP31 | FIFOIP30 | FIFOIP29 | FIFOIP28 | FIFOIP27 | FIFOIP26 | FIFOIP25 | FIFOIP24 | FIFOIP23 | FIFOIP22 | FIFOIP21 | FIFOIP20 | FIFOIP19 | FIFOIP18 | FIFOIP17 | FIFOIP16 | 0000 |
| | | 15:0 | FIFOIP15 | FIFOIP14 | FIFOIP13 | FIFOIP12 | FIFOIP11 | FIFOIP10 | FIFOIP9 | FIFOIP8 | FIFOIP7 | FIFOIP6 | FIFOIP5 | FIFOIP4 | FIFOIP3 | FIFOIP2 | FIFOIP1 | FIFOIP0 | 0000 |
| 0060 | C1RXOVF | 31:16 | RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 | RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 | 0000 |
| | | 15:0 | RXOVF15 | RXOVF14 | RXOVF13 | RXOVF12 | RXOVF11 | RXOVF10 | RXOVF9 | RXOVF8 | RXOVF7 | RXOVF6 | RXOVF5 | RXOVF4 | RXOVF3 | RXOVF2 | RXOVF1 | RXOVF0 | 0000 |
| 0070 | C1TMR | 31:16 | CANTS<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | CANTSPRE<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0080 | C1RXM0 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| 0090 | C1RXM1 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| 00A0 | C1RXM2 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| 00B0 | C1RXM3 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| 00C0 | C1FLTCON0 | 31:16 | FLTEN3 | MSEL3<1:0> | | FSEL3<4:0> | | | | | FLTEN2 | MSEL2<1:0> | | FSEL2<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN1 | MSEL1<1:0> | | FSEL1<4:0> | | | | | FLTEN0 | MSEL0<1:0> | | FSEL0<4:0> | | | | | 0000 |
| 00D0 | C1FLTCON1 | 31:16 | FLTEN7 | MSEL7<1:0> | | FSEL7<4:0> | | | | | FLTEN6 | MSEL6<1:0> | | FSEL6<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN5 | MSEL5<1:0> | | FSEL5<4:0> | | | | | FLTEN4 | MSEL4<1:0> | | FSEL4<4:0> | | | | | 0000 |
| 00E0 | C1FLTCON2 | 31:16 | FLTEN11 | MSEL11<1:0> | | FSEL11<4:0> | | | | | FLTEN10 | MSEL10<1:0> | | FSEL10<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN9 | MSEL9<1:0> | | FSEL9<4:0> | | | | | FLTEN8 | MSEL8<1:0> | | FSEL8<4:0> | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

**REGISTER 30-3: ETHTXST: ETHERNET CONTROLLER TX PACKET DESCRIPTOR START ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TXSTADDR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TXSTADDR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TXSTADDR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| | TXSTADDR<7:2> | | | | | | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-2 **TXSTADDR<31:2>:** Starting Address of First Transmit Descriptor bits
This register should not be written while any transmit, receive or DMA operations are in progress.
This address must be 4-byte aligned (bits 1-0 must be '00').

bit 1-0 **Unimplemented:** Read as '0'

**Note 1:** This register is only used for TX operations.
**2:** This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

**REGISTER 30-4: ETHRXST: ETHERNET CONTROLLER RX PACKET DESCRIPTOR START ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXSTADDR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXSTADDR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXSTADDR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| | RXSTADDR<7:2> | | | | | | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-2 **RXSTADDR<31:2>:** Starting Address of First Receive Descriptor bits
This register should not be written while any transmit, receive or DMA operations are in progress.
This address must be 4-byte aligned (bits 1-0 must be '00').

bit 1-0 **Unimplemented:** Read as '0'

**Note 1:** This register is only used for RX operations.
**2:** This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

**REGISTER 30-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | HTEN | MPEN | — | NOTPM | PMMODE<3:0> | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CRCERREN | CRCOKEN | RUNTERREN | RUNTEN | UCEN | NOTMEEN | MCEN | BCEN |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **HTEN:** Enable Hash Table Filtering bit
1 = Enable Hash Table Filtering
0 = Disable Hash Table Filtering

bit 14 **MPEN:** Magic Packet™ Enable bit
1 = Enable Magic Packet Filtering
0 = Disable Magic Packet Filtering

bit 13 **Unimplemented:** Read as '0'

bit 12 **NOTPM:** Pattern Match Inversion bit
1 = The Pattern Match Checksum must not match for a successful Pattern Match to occur
0 = The Pattern Match Checksum must match for a successful Pattern Match to occur
This bit determines whether Pattern Match Checksum must match in order for a successful Pattern Match to occur.

bit 11-8 **PMMODE<3:0>:** Pattern Match Mode bits
1001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Packet = Magic Packet)**(1,3)**
1000 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Hash Table Filter match)**(1,1)**
0111 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)**(1)**
0110 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)**(1)**
0101 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)**(1)**
0100 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)**(1)**
0011 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)**(1)**
0010 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)**(1)**
0001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches)**(1)**
0000 = Pattern Match is disabled; pattern match is always unsuccessful

**Note 1:** XOR = True when either one or the other conditions are true, but not both.
**2:** This Hash Table Filter match is active regardless of the value of the HTEN bit.
**3:** This Magic Packet Filter match is active regardless of the value of the MPEN bit.

**Note 1:** This register is only used for RX operations.
**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

**REGISTER 30-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER (CONTINUED)**

bit 6 **TXBUSY:** Transmit Busy bit(2,6)

1 = TX logic is receiving data
0 = TX logic is idle

This bit indicates that a packet is currently being transmitted. A change in this status bit is not necessarily reflected by the TXDONE interrupt, as TX packets may be aborted or rejected by the MAC.

bit 5 **RXBUSY:** Receive Busy bit(3,6)

1 = RX logic is receiving data
0 = RX logic is idle

This bit indicates that a packet is currently being received. A change in this status bit is not necessarily reflected by the RXDONE interrupt, as RX packets may be aborted or rejected by the RX filter.

bit 4-0 **Unimplemented:** Read as '0'

**Note 1:** This bit is only used for RX operations.
**2:** This bit is only affected by TX operations.
**3:** This bit is only affected by RX operations.
**4:** This bit is affected by TX and RX operations.
**5:** This bit will be *set* when the ON bit (ETHCON1<15>) = 1.
**6:** This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

**REGISTER 30-37: EMAC1SA0: ETHERNET CONTROLLER MAC STATION ADDRESS 0 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P |
| | STNADDR6<7:0> | | | | | | | |
| 7:0 | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P |
| | STNADDR5<7:0> | | | | | | | |

| **Legend:** | | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STNADDR6<7:0>:** Station Address Octet 6 bits
These bits hold the sixth transmitted octet of the station address.

bit 7-0 **STNADDR5<7:0>:** Station Address Octet 5 bits
These bits hold the fifth transmitted octet of the station address.

**Note 1:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**2:** This register is loaded at reset from the factory preprogrammed station address.

**TABLE 37-10: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| DI60a | IICL | **Input Low Injection Current** | 0 | — | -5(2,5) | mA | This parameter applies to all pins, with the exception of RB10. Maximum IICH current for this exception is 0 mA. |
| DI60b | IICH | **Input High Injection Current** | 0 | — | +5(3,4,5) | mA | This parameter applies to all pins, with the exception of all 5V tolerant pins, OSCI, OSCO, SOSCI, SOSCO, D+, D- and RB10. Maximum IICH current for these exceptions is 0 mA. |
| DI60c | ∑IICT | **Total Input Injection Current (sum of all I/O and control pins)** | -20(6) | — | +20(6) | mA | Absolute instantaneous sum of all ± input injection currents from all I/O pins ( \| IICL + \| IICH \| ) ≤ ∑IICT |

**Note 1:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** VIL source < (VSS - 0.3). Characterized but not tested.

**3:** VIH source > (VDD + 0.3) for non-5V tolerant pins only.

**4:** Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any “positive” input injection current.

**5:** Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

**6:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. If **Note 2**, IICL = (((Vss - 0.3) - VIL source) / Rs). If **Note 3**, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

## 40.0 AC AND DC CHARACTERISTICS GRAPHS

**Note:** The graphs provided are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

**FIGURE 40-1: VOH – 4x DRIVER PINS**

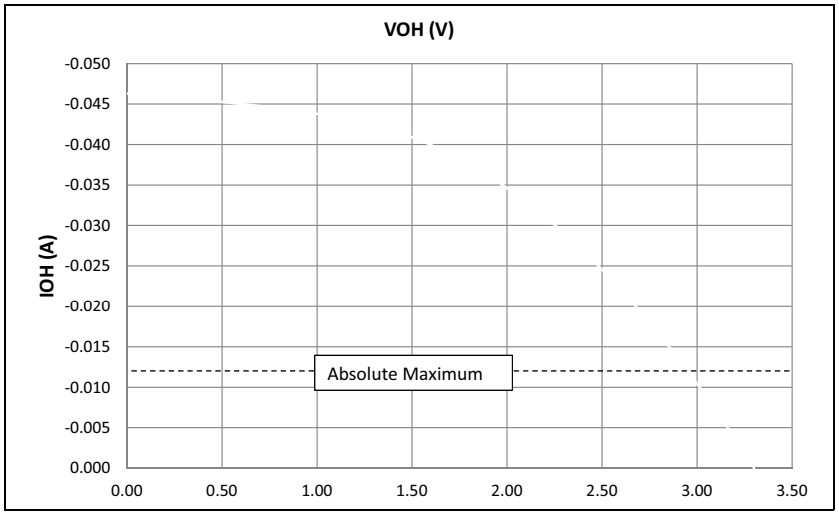



**FIGURE 40-2: VOL – 4x DRIVER PINS**

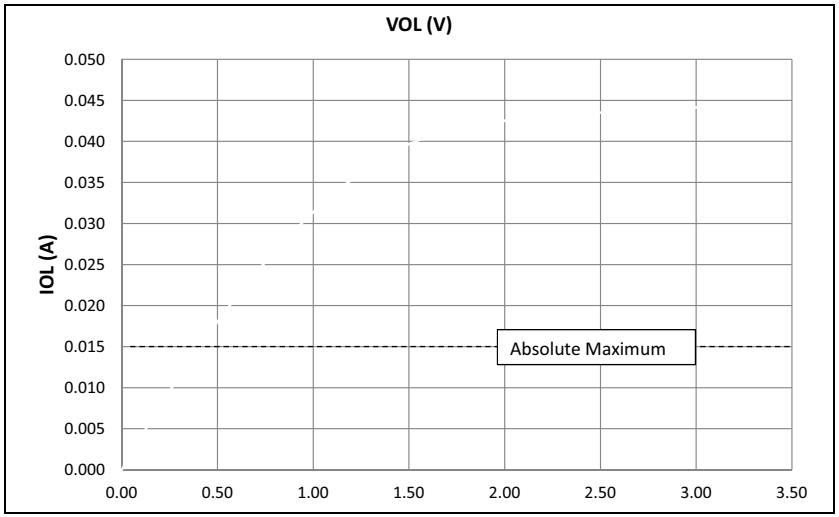



**FIGURE 40-3: VOH – 8x DRIVER PINS**

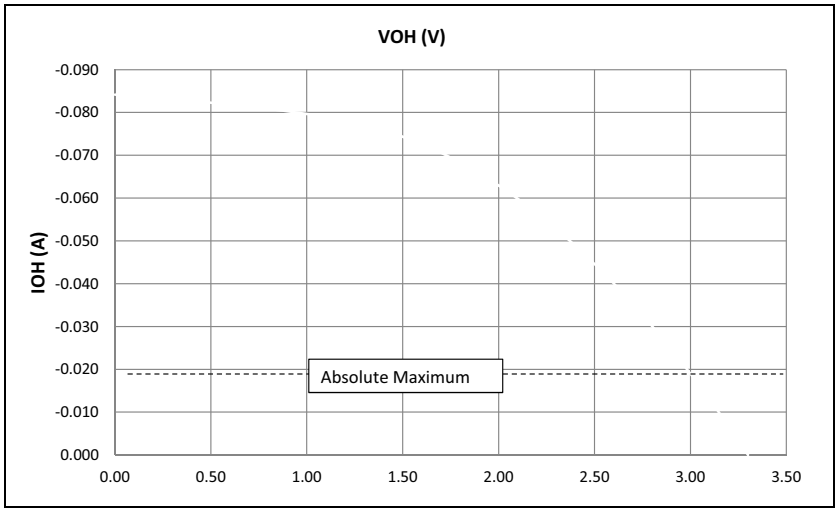
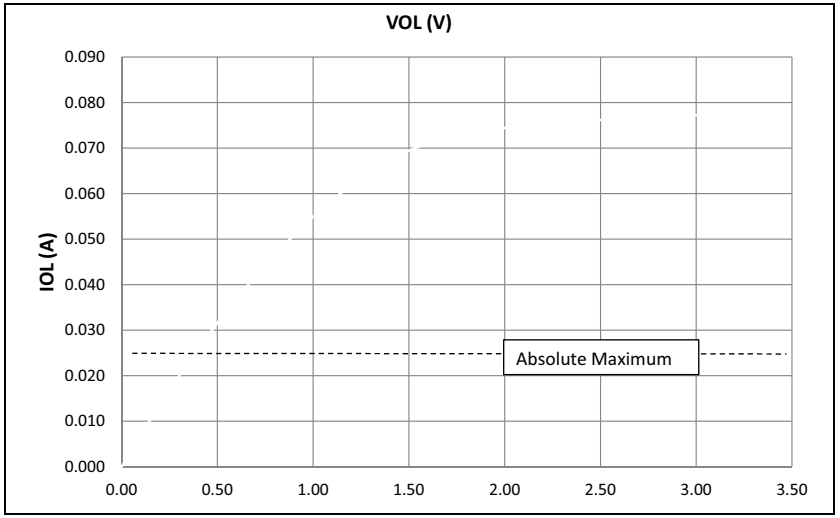
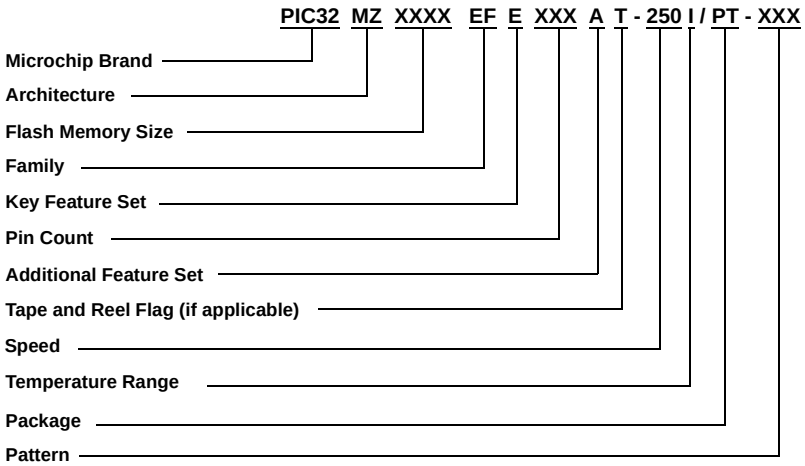



**FIGURE 40-4: VOL – 8x DRIVER PINS**



## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.




**Example:**

PIC32MZ2048EFH144-I/PT:
Embedded Connectivity PIC32,
MIPS32® M-Class MPU core,
2048 KB program memory,
144-pin, with Floating Point Unit,
Industrial temperature, TQFP package.

**Flash Memory Family**

| | | |
|---|---|---|
| Architecture | MZ | = MIPS32® M-Class MPU Core |
| Flash Memory Size | 0512 | = 512 KB |
| | 1024 | = 1024 KB |
| | 2048 | = 2048 KB |
| Family | EF | = Embedded Connectivity Microcontroller Family with Floating Point Unit |
| Key Feature | E | = PIC32 EF Family Features (no CAN, no Crypto) |
| | F | = PIC32 EF Family Features (CAN, no Crypto) |
| | G | = PIC32 EF Family Features (no CAN, no Crypto) |
| | H | = PIC32 EF Family Features (CAN, no Crypto) |
| | K | = PIC32 EF Family Features (Crypto and CAN) |
| | M | = PIC32 EF Family Features (Crypto and CAN) |
| Pin Count | 064 | = 64-pin |
| | 100 | = 100-pin |
| | 124 | = 124-pin |
| | 144 | = 144-pin |
| Speed | Blank | = Up to 200 MHz |
| | 250 | = Up to 252 MHz |
| Temperature Range | I | = -40°C to +85°C (Industrial) |
| | E | = -40°C to +125°C (Extended) |
| Package | MR | = 64-Lead (9x9x0.9 mm) QFN (Plastic Quad Flatpack) |
| | PT | = 64-Lead (10x10x1 mm) TQFP (Thin Quad Flatpack) |
| | PT | = 100-Lead (12x12x1 mm) TQFP (Thin Quad Flatpack) |
| | PF | = 100-Lead (14x14x1 mm) TQFP (Thin Quad Flatpack) |
| | TL | = 124-Lead (9x9x0.9 mm) VTLA (Very Thin Leadless Array) |
| | PH | = 144-Lead (16x16x1 mm) TQFP (Thin Quad Flatpack) |
| | PL | = 144-Lead (20x20x1.40 mm) LQFP (Low Profile Quad Flatpack) |
| Pattern | | Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) |
| | ES | = Engineering Sample |