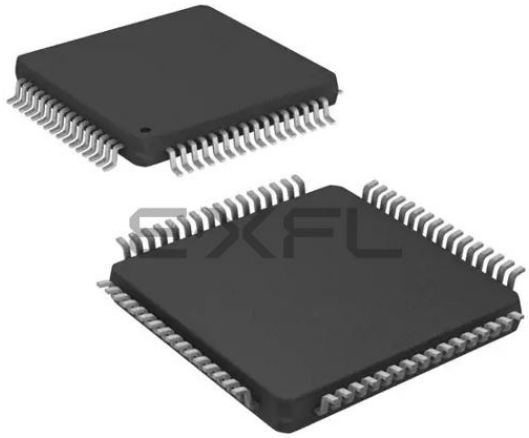
Microchip Technology - PIC32MZ1024EFE064-I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	46
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efe064-i-pt

A block diagram of the PIC32MZ EF family processor core is shown in Figure 3-1.

FIGURE 3-1: PIC32MZ EF FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM

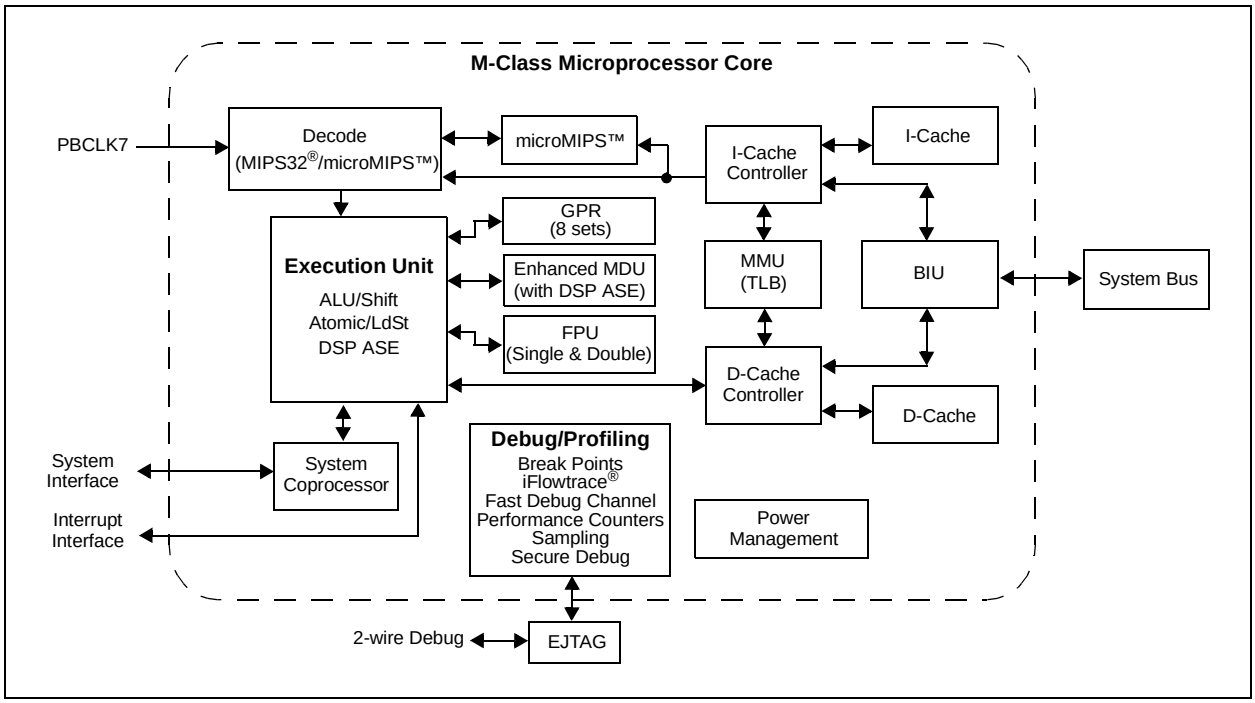


TABLE 4-11: SYSTEM BUS TARGET 3 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8C20	SBT3ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8C24	SBT3ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8C28	SBT3ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8C30	SBT3ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C38	SBT3ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C40	SBT3REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C50	SBT3RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C58	SBT3WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C60	SBT3REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C70	SBT3RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C78	SBT3WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C80	SBT3REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C90	SBT3RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C98	SBT3WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

7.3 Interrupt Control Registers

TABLE 7-3: INTERRUPT REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	INTCON	31:16	NMIKEY<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
0010	PRISS	31:16	PRI7SS<3:0>				PRI6SS<3:0>				PRI5SS<3:0>				PRI4SS<3:0>				0000
		15:0	PRI3SS<3:0>				PRI2SS<3:0>				PRI1SS<3:0>				—	—	—	SS0	0000
0020	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			SIRQ<7:0>								0000
0030	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
0040	IFS0	31:16	OC6IF	IC6IF	IC6EIF	T6IF	OC5IF	IC5IF	IC5EIF	T5IF	INT4IF	OC4IF	IC4IF	IC4EIF	T4IF	INT3IF	OC3IF	IC3IF	0000
		15:0	IC3EIF	T3IF	INT2IF	OC2IF	IC2IF	IC2EIF	T2IF	INT1IF	OC1IF	IC1IF	IC1EIF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
0050	IFS1	31:16	ADCD4IF	ADCD3IF	ADCD2IF	ADCD1IF	ADCD0IF	ADCFLTIF	ADCDF6IF	ADCDF5IF	ADCDF4IF	ADCDF3IF	ADCDF2IF	ADCDF1IF	ADCDC6IF	ADCDC5IF	ADCDC4IF	ADCDC3IF	0000
		15:0	ADCDC2IF	ADCDC1IF	ADCFIFOIF	ADCIF	OC9IF	IC9IF	IC9EIF	T9IF	OC8IF	IC8IF	IC8EIF	T8IF	OC7IF	IC7IF	IC7EIF	T7IF	0000
0060	IFS2(5)	31:16	ADCD36IF	ADCD35IF	ADCD34IF	ADCD33IF	ADCD32IF	ADCD31IF	ADCD30IF	ADCD29IF	ADCD28IF	ADCD27IF	ADCD26IF	ADCD25IF	ADCD24IF	ADCD23IF	ADCD22IF	ADCD21IF	0000
		15:0	ADCD20IF	ADCD19IF	ADCD18IF	ADCD17IF	ADCD16IF	ADCD15IF	ADCD14IF	ADCD13IF	ADCD12IF	ADCD11IF	ADCD10IF	ADCD9IF	ADCD8IF	ADCD7IF	ADCD6IF	ADCD5IF	0000
0070	IFS3(6)	31:16	CNKIF(8)	CNJIF	CNHIF	CNGIF	CNFIF	CNEIF	CNDIF	CNCIF	CNBIF	CNAIF	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	0000
		15:0	SPI1TXIF	SPI1RXIF	SPI1EIF	—	CRPTIF(7)	SBIF	CFDCIF	CPCIF	ADCD44IF	ADCD43IF	ADCD42IF	ADCD41IF	ADCD40IF	ADCD39IF	ADCD38IF	ADCD37IF	0000
0080	IFS4	31:16	U3TXIF	U3RXIF	U3EIF	SPI3TXIF	SPI3RXIF	SPI3EIF	ETHIF	CAN2IF(3)	CAN1IF(3)	I2C2MIF(2)	I2C2SIF(2)	I2C2BIF(2)	U2TXIF	U2RXIF	U2EIF	SPI2TXIF	0000
		15:0	SPI2RXIF	SPI2EIF	DMA7IF	DMA6IF	DMA5IF	DMA4IF	DMA3IF	DMA2IF	DMA1IF	DMA0IF	USBDMAIF	USBIF	CMP2IF	CMP1IF	PMPEIF	PMPIF	0000
0090	IFS5	31:16	—	U6TXIF	U6RXIF	U6EIF	SPI6TX(2)	SPI6RXIF(2)	SPI6IF(2)	I2C5MIF	I2C5SIF	I2C5BIF	U5TXIF	U5RXIF	U5EIF	SPI5TXIF(2)	SPI5RXIF(2)	SPI5EIF(2)	0000
		15:0	I2C4MIF	I2C4SIF	I2C4BIF	U4TXIF	U4RXIF	U4EIF	SQI1IF	PREIF	FCEIF	RTCCIF	SPI4TXIF	SPI4RXIF	SPI4EIF	I2C3MIF	I2C3SIF	I2C3BIF	0000
00A0	IFS6	31:16	—	—	—	—	—	—	—	—	—	—	ADC7WIF	—	—	ADC4WIF	ADC3WIF	ADC2WIF	0000
		15:0	ADC1WIF	ADC0WIF	ADC7EIF	—	—	ADC4EIF	ADC3EIF	ADC2EIF	ADC1EIF	ADC0EIF	—	ADCGRPIF	—	ADCURDYIF	ADCARDYIF	ADCEOSIF	0000
00C0	IEC0	31:16	OC6IE	IC6IE	IC6EIE	T6IE	OC5IE	IC5IE	IC5EIE	T5IE	INT4IE	OC4IE	IC4IE	IC4EIE	T4IE	INT3IE	OC3IE	IC3IE	0000
		15:0	IC3EIE	T3IE	INT2IE	OC2IE	IC2IE	IC2EIE	T2IE	INT1IE	OC1IE	IC1IE	IC1EIE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
00D0	IEC1	31:16	ADCD4IE	ADCD3IE	ADCD2IE	ADCD1IE	ADCD0IE	ADCFLTIE	ADCDF6IE	ADCDF5IE	ADCDF4IE	ADCDF3IE	ADCDF2IE	ADCDF1IE	ADCDC6IE	ADCDC5IE	ADCDC4IE	ADCDC3IE	0000
		15:0	ADCDC2IE	ADCDC1IE	ADCFIFOIE	ADCIE	OC9IE	IC9IE	IC9EIE	T9IE	OC8IE	IC8IE	IC8EIE	T8IE	OC7IE	IC7IE	IC7EIE	T7IE	0000
00E0	IEC2(5)	31:16	ADCD36IE	ADCD35IE	ADCD34IE	ADCD33IE	ADCD32IE	ADCD31IE	ADCD30IE	ADCD29IE	ADCD28IE	ADCD27IE	ADCD26IE	ADCD25IE	ADCD24IE	ADCD23IE	ADCD22IE	ADCD21IE	0000
		15:0	ADCD20IE	ADCD19IE	ADCD18IE	ADCD17IE	ADCD16IE	ADCD15IE	ADCD14IE	ADCD13IE	ADCD12IE	ADCD11IE	ADCD10IE	ADCD9IE	ADCD8IE	ADCD7IE	ADCD6IE	ADCD5IE	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

REGISTER 8-6: PBxDIV: PERIPHERAL BUS 'x' CLOCK DIVISOR CONTROL REGISTER ('x' = 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-1	U-0	U-0	U-0	R-1	U-0	U-0	U-0
	ON(1)	—	—	—	PBDIVRDY	—	—	—
7:0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	PBDIV<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Peripheral Bus 'x' Output Clock Enable bit(1)
- 1 = Output clock is enabled
- 0 = Output clock is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **PBDIVRDY:** Peripheral Bus 'x' Clock Divisor Ready bit
- 1 = Clock divisor logic is not switching divisors and the PBxDIV<6:0> bits may be written
- 0 = Clock divisor logic is currently switching values and the PBxDIV<6:0> bits cannot be written

bit 10-7 **Unimplemented:** Read as '0'

bit 6-0 **PBDIV<6:0>:** Peripheral Bus 'x' Clock Divisor Control bits
- 1111111 = PBCLKx is SYSCLK divided by 128
- 1111110 = PBCLKx is SYSCLK divided by 127
- •
- •
- •
- 0000011 = PBCLKx is SYSCLK divided by 4
- 0000010 = PBCLKx is SYSCLK divided by 3
- 0000001 = PBCLKx is SYSCLK divided by 2 (default value for x ≠ 7)
- 0000000 = PBCLKx is SYSCLK divided by 1 (default value for x = 7)

Note 1: The clock for peripheral bus 1 cannot be turned off. Therefore, the ON bit in the PB1DIV register cannot be written as a '0'.

Note: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 10-7: DCHxCON: DMA CHANNEL x CONTROL REGISTER (CONTINUED)

bit 4 **CHAEN:** Channel Automatic Enable bit
1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete
0 = Channel is disabled on block transfer complete

bit 3 **Unimplemented:** Read as '0'

bit 2 **CHEDET:** Channel Event Detected bit
1 = An event has been detected
0 = No events have been detected

bit 1-0 **CHPRI<1:0>:** Channel Priority bits
11 = Channel has priority 3 (highest)
10 = Channel has priority 2
01 = Channel has priority 1
00 = Channel has priority 0

Note 1: The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).

2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

REGISTER 10-16: DCHxCSIZ: DMA CHANNEL x CELL-SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCSIZ<15:0>:** Channel Cell-Size bits

1111111111111111 = 65,535 bytes transferred on an event
•
•
•
0000000000000010 = 2 bytes transferred on an event
0000000000000001= 1 byte transferred on an event
0000000000000000 = 65,536 bytes transferred on an event

REGISTER 10-17: DCHxCPTR: DMA CHANNEL x CELL POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCPTR<15:0>:** Channel Cell Progress Pointer bits

1111111111111111 = 65,535 bytes have been transferred since the last event
•
•
•
0000000000000001 = 1 byte has been transferred since the last event
0000000000000000 = 0 bytes have been transferred since the last event

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 11-28: USBLPMR1: USB LINK POWER MANAGEMENT CONTROL REGISTER 1 (CONTINUED)

bit 16 **LPMXMT:** LPM Transition to the L1 State bit

When in *Device mode*:

1 = USB module will transition to the L1 state upon the receipt of the next LPM transaction. LPMEN must be set to '0b11. Both LPMXMT and LPMEN must be set in the same cycle.

0 = Maintain current state

When LPMXMT and LPMEN are set, the USB module can respond in the following ways:

- If no data is pending (all TX FIFOs are empty), the USB module will respond with an ACK. The bit will self clear and a software interrupt will be generated.
- If data is pending (data resides in at least one TX FIFO), the USB module will respond with a NYET. In this case, the bit will not self clear however a software interrupt will be generated.

When in *Host mode*:

1 = USB module will transmit an LPM transaction. This bit is self clearing, and will be immediately cleared upon receipt of any Token or three time-outs have occurred.

0 = Maintain current state

bit 15-12 **ENDPOINT<3:0>:** LPM Token Packet Endpoint bits

This is the endpoint in the token packet of the LPM transaction.

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **RMTWAK:** Remote Wake-up Enable bit

This bit is applied on a temporary basis only and is only applied to the current suspend state.

1 = Remote wake-up is enabled

0 = Remote wake-up is disabled

bit 7-4 **HIRD<3:0>:** Host Initiated Resume Duration bits

The minimum time the host will drive resume on the bus. The value in this register corresponds to an actual resume time of:

Resume Time = 50 µs + HIRD * 75 µs. The resulting range is 50 µs to 1200 µs.

bit 3-0 **LNKSTATE<3:0>:** Link State bits

This value is provided by the host to the peripheral to indicate what state the peripheral must transition to after the receipt and acceptance of a LPM transaction. The only valid value for this register is '1' for Sleep State (L1). All other values are reserved.

TABLE 12-8: PORTD REGISTER MAP FOR 124-PIN AND 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0300	ANSELD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSD15	ANSD14	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C000
0310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	—	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FEFF
0320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	—	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
0330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	—	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
0340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	—	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
0350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUD15	CNPUD14	CNPUD13	CNPUD12	CNPUD11	CNPUD10	CNPUD9	—	CNPUD7	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
0360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDD15	CNPDD14	CNPDD13	CNPDD12	CNPDD11	CNPDD10	CNPDD9	—	CNPDD7	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
0370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNEND15	CNEND14	CNEND13	CNEND12	CNEND11	CNEND10	CNEND9	—	CNEND7	CNEND6	CNEND5	CNEND4	CNEND3	CNEND2	CNEND1	CNEND0	0000
0390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATD15	CN STATD14	CN STATD13	CN STATD12	CN STATD11	CN STATD10	CN STATD9	—	CN STATD7	CN STATD6	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	CN STATD0	0000
03A0	CNNED	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNED15	CNNED14	CNNED13	CNNED12	CNNED11	CNNED10	CNNED9	—	CNNED7	CNNED6	CNNED5	CNNED4	CNNED3	CNNED2	CNNED1	CNNED0	0000
03B0	CNFD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFD15	CNFD14	CNFD13	CNFD12	CNFD11	CNFD10	CNFD9	—	CNFD7	CNFD6	CNFD5	CNFD4	CNFD3	CNFD2	CNFD1	CNFD0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

TABLE 12-18: PORTH REGISTER MAP FOR 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0700	ANSELH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	ANSH6	ANSH5	ANSH4	—	—	ANSH1	ANSH0	0073
0710	TRISH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISH15	TRISH14	TRISH13	TRISH12	TRISH11	TRISH10	TRISH9	TRISH8	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	FFFF
0720	PORTH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RH15	RH14	RH13	RH12	RH11	RH10	RH9	RH8	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0	xxxx
0730	LATH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATH15	LATH14	LATH13	LATH12	LATH11	LATH10	LATH9	LATH8	LATH7	LATH6	LATH5	LATH4	LATH3	LATH2	LATH1	LATH0	xxxx
0740	ODCH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCH15	ODCH14	ODCH13	ODCH12	ODCH11	ODCH10	ODCH9	ODCH8	ODCH7	ODCH6	ODCH5	ODCH4	ODCH3	ODCH2	ODCH1	ODCH0	0000
0750	CNPUH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUH15	CNPUH14	CNPUH13	CNPUH12	CNPUH11	CNPUH10	CNPUH9	CNPUH8	CNPUH7	CNPUH6	CNPUH5	CNPUH4	CNPUH3	CNPUH2	CNPUH1	CNPUH0	0000
0760	CNPDH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDH15	CNPDH14	CNPDH13	CNPDH12	CNPDH11	CNPDH10	CNPDH9	CNPDH8	CNPDH7	CNPDH6	CNPDH5	CNPDH4	CNPDH3	CNPDH2	CNPDH1	CNPDH0	0000
0770	CNCONH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0780	CNENH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNENH15	CNENH14	CNENH13	CNENH12	CNENH11	CNENH10	CNENH9	CNENH8	CNENH7	CNENH6	CNENH5	CNENH4	CNENH3	CNENH2	CNENH1	CNENH0	0000
0790	CNSTATH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATH15	CN STATH14	CN STATH13	CN STATH12	CN STATH11	CN STATH10	CN STATH9	CN STATH8	CN STATH7	CN STATH6	CN STATH5	CN STATH4	CN STATH3	CN STATH2	CN STATH1	CN STATH0	0000
07A0	CNNEH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEH15	CNNEH14	CNNEH13	CNNEH12	CNNEH11	CNNEH10	CNNEH9	CNNEH8	CNNEH7	CNNEH6	CNNEH5	CNNEH4	CNNEH3	CNNEH2	CNNEH1	CNNEH0	0000
07B0	CNFH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFH15	CNFH14	CNFH13	CNFH12	CNFH11	CNFH10	CNFH9	CNFH8	CNFH7	CNFH6	CNFH5	CNFH4	CNFH3	CNFH2	CNFH1	CNFH0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

TABLE 12-23: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1620	RPE8R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE8R<3:0>				0000
1624	RPE9R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE9R<3:0>				0000
1640	RPF0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF0R<3:0>				0000
1644	RPF1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF1R<3:0>				0000
1648	RPF2R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF2R<3:0>				0000
164C	RPF3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF3R<3:0>				0000
1650	RPF4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF4R<3:0>				0000
1654	RPF5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF5R<3:0>				0000
1660	RPF8R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF8R<3:0>				0000
1670	RPF12R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG12R<3:0>				0000
1674	RPF13R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG0R<3:0>				0000
1680	RPG0R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG1R<3:0>				0000
1684	RPG1R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG1R<3:0>				0000
1698	RPG6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG6R<3:0>				0000
169C	RPG7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG7R<3:0>				0000
16A0	RPG8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG8R<3:0>				0000
16A4	RPG9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG9R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

2: This register is not available on 64-pin and 100-pin devices.

REGISTER 20-7: SQI1INTTHR: SQI INTERRUPT THRESHOLD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TXINTTHR<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RXINTTHR<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **TXINTTHR<4:0>:** Transmit Interrupt Threshold bits

A transmit interrupt is set when the transmit FIFO has more space than the set number of bytes. For 16-bit mode, the value should be a multiple of 2.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RXINTTHR<4:0>:** Receive Interrupt Threshold bits

A receive interrupt is set when the receive FIFO count is larger than or equal to the set number of bytes. For 16-bit mode, the value should be multiple of 2.

REGISTER 21-2: I2CxSTAT: I^2C STATUS REGISTER (CONTINUED)

bit 5 **D_A:** Data/Address bit (when operating as I^2C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was device address
Hardware clear at device address match. Hardware set by reception of slave byte.

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

bit 2 **R_W:** Read/Write Information bit (when operating as I^2C slave)
1 = Read – indicates data transfer is output from slave
0 = Write – indicates data transfer is input to slave
Hardware set or clear after reception of I^2C device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive complete, I2CxRCV is full
0 = Receive not complete, I2CxRCV is empty
Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit in progress, I2CxTRN is full
0 = Transmit complete, I2CxTRN is empty
Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

REGISTER 27-2: RNGCON: RANDOM NUMBER GENERATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	LOAD	TRNGMODE	CONT	PRNGEN	TRNGEN
7:0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
	PLEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12 **LOAD:** Device Select bit

This bit is self-clearing and is used to load the seed from the TRNG (i.e., the random value) as a seed to the PRNG.

bit 11 **TRNGMODE:** TRNG Mode Selection bit

1 = Use ring oscillators with bias corrector
0 = Use ring oscillators with XOR tree

Note: Enabling this bit will generate numbers with a more even distribution of randomness.

bit 10 **CONT:** PRNG Number Shift Enable bit

1 = The PRNG random number is shifted every cycle
0 = The PRNG random number is shifted when the previous value is removed

bit 9 **PRNGEN:** PRNG Operation Enable bit

1 = PRNG operation is enabled
0 = PRNG operation is not enabled

bit 8 **TRNGEN:** TRNG Operation Enable bit

1 = TRNG operation is enabled
0 = TRNG operation is not enabled

bit 7-0 **PLEN<7:0>:** PRNG Polynomial Length bits

These bits contain the length of the polynomial used for the PRNG.

REGISTER 28-32: ADCANCON: ADC ANALOG WARM-UP CONTROL REGISTER (CONTINUED)

bit 7 **ANEN7:** Shared ADC (ADC7) Analog and Bias Circuitry Enable bit

1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.

0 = Analog and bias circuitry disabled

bit 5-6 **Unimplemented:** Read as '0'

bit 4-0 **ANEN4:ANEN0:** ADC4-ADC0 Analog and Bias Circuitry Enable bits

1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.

0 = Analog and bias circuitry disabled

REGISTER 30-14: ETHIRQ: ETHERNET CONTROLLER INTERRUPT REQUEST REGISTER

bit 7 **RXDONE:** Receive Done Interrupt bit(2)

1 = RX packet was successfully received
0 = No interrupt pending

This bit is set whenever an RX packet is successfully received. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 6 **PKTPEND:** Packet Pending Interrupt bit(2)

1 = RX packet pending in memory
0 = RX packet is not pending in memory

This bit is set when the BUFCNT counter has a value other than '0'. It is cleared by either a Reset or by writing the BUFCDEC bit to decrement the BUFCNT counter. Writing a '0' or a '1' has no effect.

bit 5 **RXACT:** Receive Activity Interrupt bit(2)

1 = RX packet data was successfully received
0 = No interrupt pending

This bit is set whenever RX packet data is stored in the RXBM FIFO. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 4 **Unimplemented:** Read as '0'

bit 3 **TXDONE:** Transmit Done Interrupt bit(2)

1 = TX packet was successfully sent
0 = No interrupt pending

This bit is set when the currently transmitted TX packet completes transmission, and the Transmit Status Vector is loaded into the first descriptor used for the packet. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 2 **TXABORT:** Transmit Abort Condition Interrupt bit(2)

1 = TX abort condition occurred on the last TX packet
0 = No interrupt pending

This bit is set when the MAC aborts the transmission of a TX packet for one of the following reasons:

- Jumbo TX packet abort
- Underrun abort
- Excessive defer abort
- Late collision abort
- Excessive collisions abort

This bit is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 1 **RXBUFNA:** Receive Buffer Not Available Interrupt bit(2)

1 = RX Buffer Descriptor Not Available condition has occurred
0 = No interrupt pending

This bit is set by a RX Buffer Descriptor Overrun condition. It is cleared by either a Reset or a CPU write of a '1' to the CLR register.

bit 0 **RXOVFLW:** Receive FIFO Over Flow Error bit(2)

1 = RX FIFO Overflow Error condition has occurred
0 = No interrupt pending

RXOVFLW is set by the RXBM Logic for an RX FIFO Overflow condition. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

Note 1: This bit is only used for TX operations.
2: This bit is are only used for RX operations.

Note:	It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 30-39: EMAC1SA2: ETHERNET CONTROLLER MAC STATION ADDRESS 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR2<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR1<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Reserved:** Maintain as '0'; ignore read

bit 15-8 **STNADDR2<7:0>:** Station Address Octet 2 bits
These bits hold the second transmitted octet of the station address.

bit 7-0 **STNADDR1<7:0>:** Station Address Octet 1 bits
These bits hold the most significant (first transmitted) octet of the station address.

Note 1: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

2: This register is loaded at reset from the factory preprogrammed station address.

REGISTER 34-6: DEVCFG3/ADEVCFG3: DEVICE CONFIGURATION WORD 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	R/P	R/P	R/P	R/P	r-1	R/P	R/P
	—	FUSBIDIO	IOL1WAY	PMDL1WAY	PGL1WAY	—	FETHIO	FMIIEN
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** Write as '1'

bit 30 **FUSBIDIO:** USB USBID Selection bit
1 = USBID pin is controlled by the USB module
0 = USBID pin is controlled by the port function

If USBMD is '1', USBID reverts to port control.

bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 28 **PMDL1WAY:** Peripheral Module Disable Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 27 **PGL1WAY:** Permission Group Lock One Way Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 26 **Reserved:** Write as '1'

bit 25 **FETHIO:** Ethernet I/O Pin Selection Configuration bit
1 = Default Ethernet I/O pins
0 = Alternate Ethernet I/O pins

This bit is ignored for devices that do not have an alternate Ethernet pin selection.

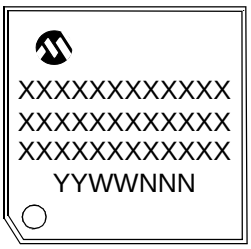
bit 24 **FMIIEN:** Ethernet MII Enable Configuration bit
1 = MII is enabled
0 = RMII is enabled

bit 23-16 **Reserved:** Write as '1'

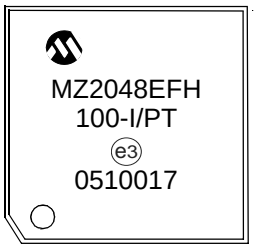
bit 15-0 **USERID<15:0>:** This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG

41.1 Package Marking Information (Continued)

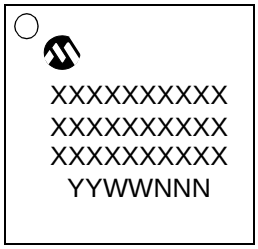
100-Lead TQFP (12x12x1 mm)



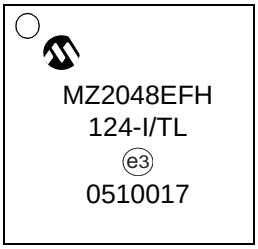
Example



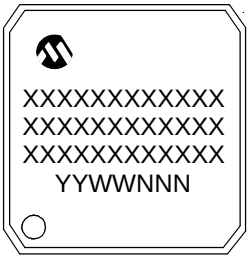
124-Lead VTLA (9x9x0.9 mm)



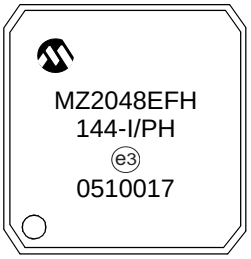
Example



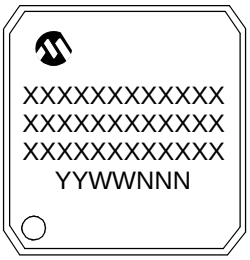
144-Lead TQFP (16x16x1 mm)



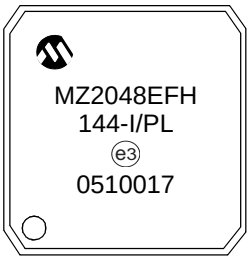
Example



144-Lead LQFP (20x20x1.40 mm)



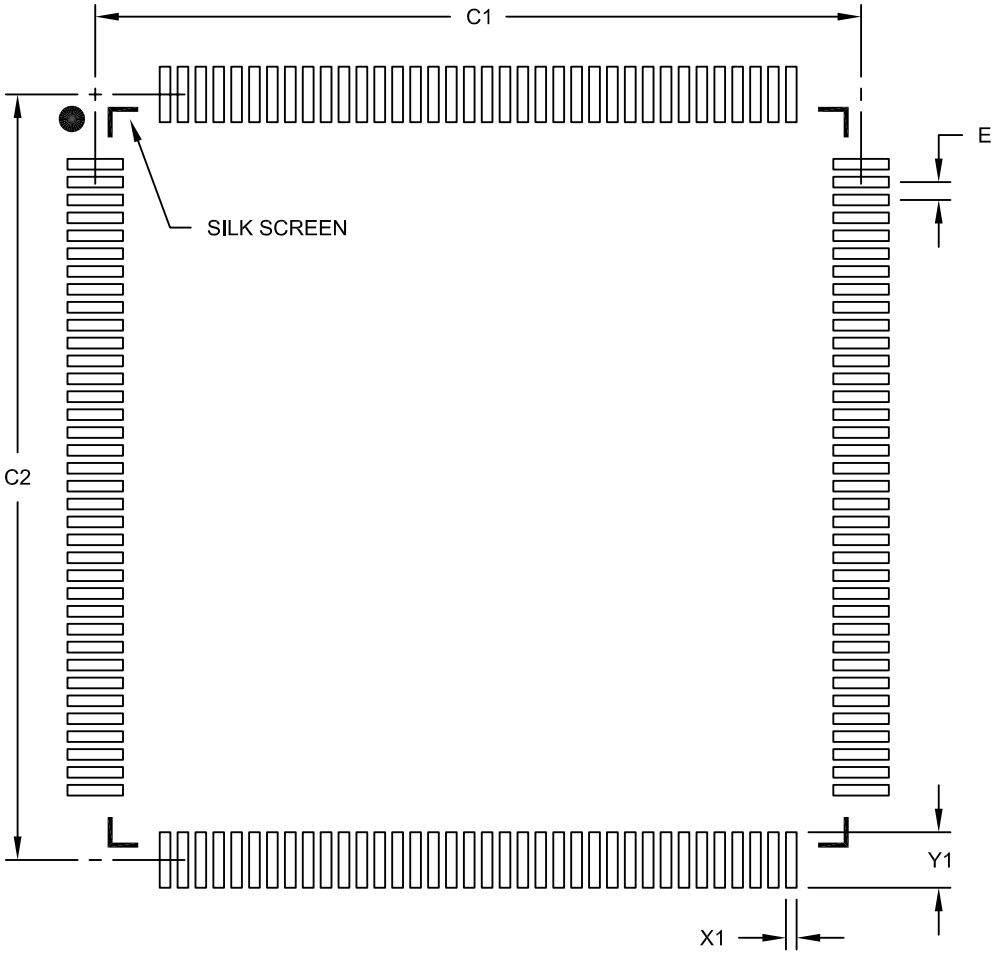
Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

144-Lead Plastic Low Profile Quad Flatpack (PL) - 20x20x1.40 mm Body [LQFP]
2.00 mm Footprint

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		21.40	
Contact Pad Spacing	C2		21.40	
Contact Pad Width (X144)	X1			0.30
Contact Pad Length (X144)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2044B

TABLE C-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
37.0 "Electrical Characteristics"	The DC Characteristics: Operating Current (I_{DD}) and Note 6 were updated (see Table 37-6). The DC Characteristics: Idle Current (I_{IDLE}) and Note 4 were updated (see Table 37-7). Parameter DC40m and Note 5 in the DC Characteristics: Power-down Current (I_{PD}) were updated (see Table 37-8). Parameter DO50 (Cosco) was removed from the Capacitive Loading Requirements on Output Pins (see Table 37-16). The Internal FRC Accuracy and Internal LPRC conditions were updated for 125ºC (see Table 37-20 and Table 37-21). Parameter SP15 and Note 5 of the SPIx Module Master Mode Timing Requirements were updated (see Table 37-30 and Table 37-31). The Temperature Sensor Specifications were updated (see Table 37-41).
38.0 "Extended Temperature Electrical Characteristics"	New chapter for Extended Temperature devices was added.
39.0 "AC and DC Characteristics Graphs"	The Typical Temperature Sensor Voltage graph was updated (see Figure 39-7).
40.0 "Packaging Information"	The package drawings and land pattern for the 64-Lead Plastic Quad Flat, No Lead Package (MR) were updated.
Appendix A: "Migrating from PIC32MX5XX/6XX/7XX to PIC32MZ EF"	The Primary Oscillator Configuration section in the Oscillator Configuration Differences was updated (see Table A-1).
Appendix B: "Migrating from PIC32MZ EC to PIC32MZ EF"	Boot Flashing aliasing was updated for PIC32MZ EF devices (see Table B-4).