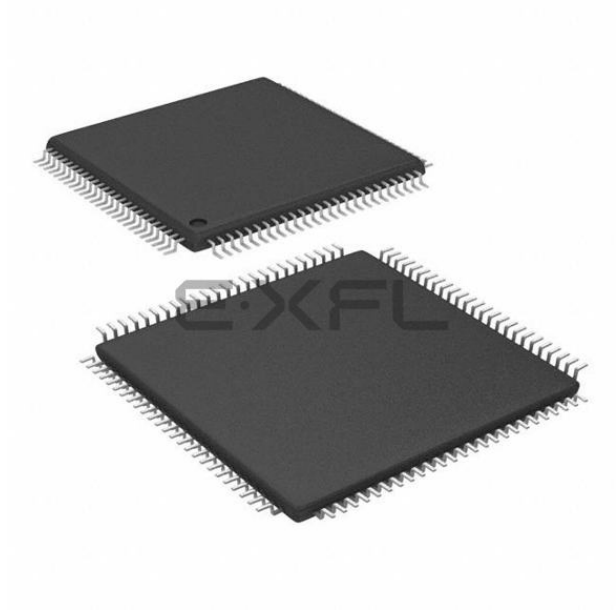
Microchip Technology - PIC32MZ1024EFE100-I/PF Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efe100-i-pf

TABLE 3: PIN NAMES FOR 100-PIN DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)100
PIC32MZ1024EF(G/H/M)100
PIC32MZ1024EF(E/F/K)100
PIC32MZ2048EF(G/H/M)100

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
71	EMDIO/AEMDIO/RPD0/RTCC/INT0/RD0	86	EBID10/ETXD0/RPF1/PMD10/RF1
72	SOSCI/RPC13/RC13	87	EBID9/ETXERR/RPG1/PMD9/RG1
73	SOSCO/RPC14/T1CK/RC14	88	EBID8/RPG0/PMD8/RG0
74	VDD	89	TRCLK/SQICLK/RA6
75	VSS	90	TRD3/SQID3/RA7
76	RPD1/SCK1/RD1	91	EBID0/PMD0/RE0
77	EBID14/ETXEN/RPD2/PMD14/RD2	92	VSS
78	EBID15/ETXCLK/RPD3/PMD15/RD3	93	VDD
79	EBID12/ETXD2/RPD12/PMD12/RD12	94	EBID1/PMD1/RE1
80	EBID13/ETXD3/PMD13/RD13	95	TRD2/SQID2/RG14
81	$\overline{\text{SQICS0}}$/RPD4/RD4	96	TRD1/SQID1/RG12
82	$\overline{\text{SQICS1}}$/RPD5/RD5	97	TRD0/SQID0/RG13
83	VDD	98	EBID2/PMD2/RE2
84	VSS	99	EBID3/RPE3/PMD3/RE3
85	EBID11/ETXD1/RPF0/PMD11/RF0	100	EBID4/AN18/PMD4/RE4

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

TABLE 1-12: PMP PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PMA0	30	44	B24	30	I/O	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)
PMA1	29	43	A28	51	I/O	TTL/ST	Parallel Master Port Address bit 1 Input (Buffered Slave modes) and Output (Master modes)
PMA2	10	16	B9	21	O	—	Parallel Master Port Address (Demultiplexed Master modes)
PMA3	6	12	B7	52	O	—	
PMA4	5	11	A8	68	O	—	
PMA5	4	2	B1	2	O	—	
PMA6	16	6	B3	6	O	—	
PMA7	22	33	A23	48	O	—	
PMA8	42	65	A44	91	O	—	
PMA9	41	64	B36	90	O	—	
PMA10	21	32	B18	47	O	—	
PMA11	27	41	A27	29	O	—	
PMA12	24	7	A6	11	O	—	
PMA13	23	34	B19	28	O	—	
PMA14	45	61	A42	87	O	—	
PMA15	43	68	B38	97	O	—	
PMCS1	45	61	A42	87	O	—	Parallel Master Port Chip Select 1 Strobe
PMCS2	43	68	B38	97	O	—	Parallel Master Port Chip Select 2 Strobe
PMD0	58	91	B52	135	I/O	TTL/ST	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMD1	61	94	A64	138	I/O	TTL/ST	
PMD2	62	98	A66	142	I/O	TTL/ST	
PMD3	63	99	B56	143	I/O	TTL/ST	
PMD4	64	100	A67	144	I/O	TTL/ST	
PMD5	1	3	A3	3	I/O	TTL/ST	
PMD6	2	4	B2	4	I/O	TTL/ST	
PMD7	3	5	A4	5	I/O	TTL/ST	
PMD8	—	88	B50	128	I/O	TTL/ST	
PMD9	—	87	A60	127	I/O	TTL/ST	
PMD10	—	86	B49	125	I/O	TTL/ST	
PMD11	—	85	A59	124	I/O	TTL/ST	
PMD12	—	79	B43	112	I/O	TTL/ST	
PMD13	—	80	A54	113	I/O	TTL/ST	
PMD14	—	77	B42	110	I/O	TTL/ST	
PMD15	—	78	A53	111	I/O	TTL/ST	
PMALL	30	44	B24	30	O	—	Parallel Master Port Address Latch Enable Low Byte (Multiplexed Master modes)
PMALH	29	43	A28	51	O	—	Parallel Master Port Address Latch Enable High Byte (Multiplexed Master modes)
PMRD	53	9	A7	13	O	—	Parallel Master Port Read Strobe
PMWR	52	8	B5	12	O	—	Parallel Master Port Write Strobe

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

6.0 RESETS

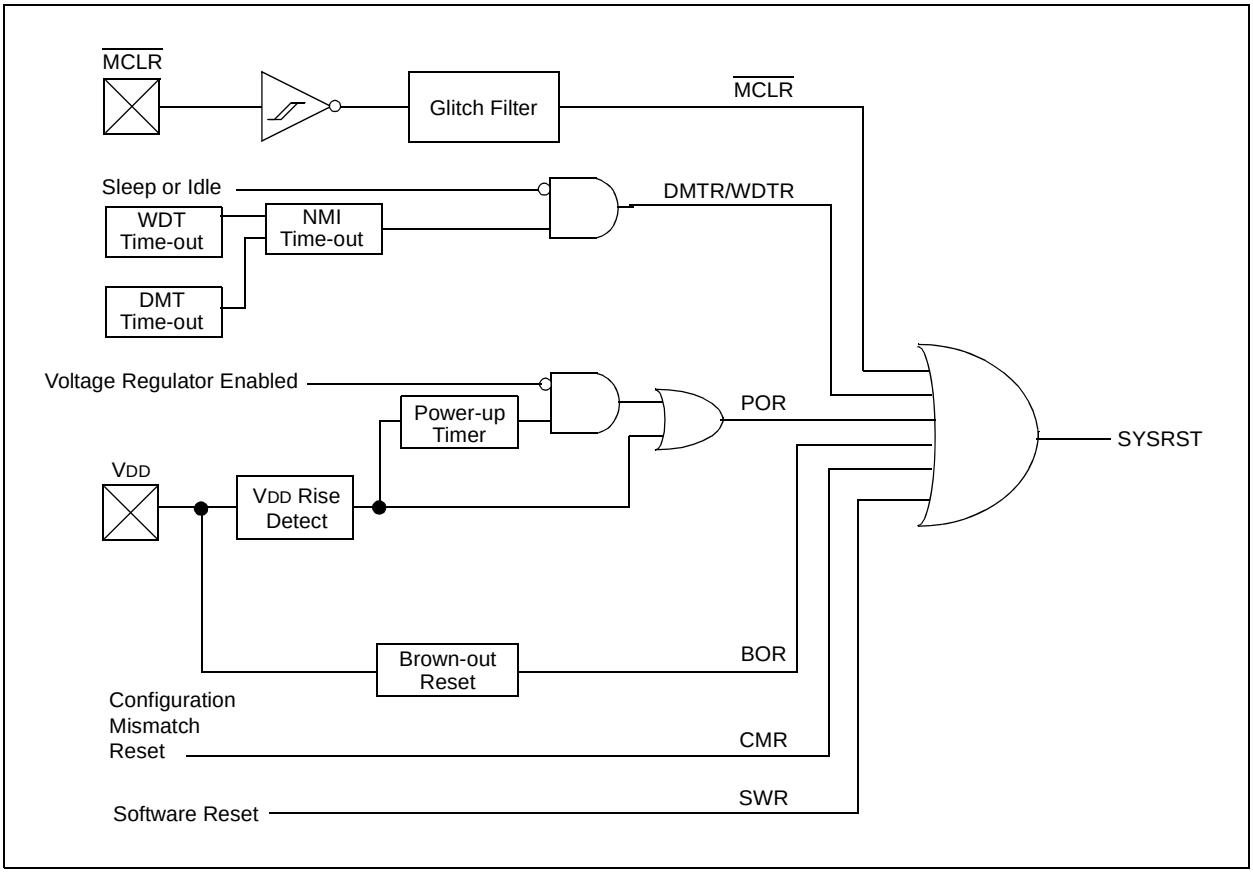
Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Master Clear Reset pin ($\overline{\text{MCLR}}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)
- Deadman Timer Reset (DMTR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM



7.1 CPU Exceptions

CPU coprocessor 0 contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events or program errors. Table 7-1 lists the exception types in order of priority.

TABLE 7-1: MIPS32® M-CLASS MICROPROCESSOR CORE EXCEPTION TYPES

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Highest Priority						
Reset	Assertion $\overline{\text{MCLR}}$ or a Power-on Reset (POR).	0xBFC0_0000	BEV, ERL	—	—	_on_reset
Soft Reset	Assertion of a software Reset.	0xBFC0_0000	BEV, SR, ERL	—	—	_on_reset
DSS	EJTAG debug single step.	0xBFC0_0480	—	DSS	—	—
DINT	EJTAG debug interrupt. Caused by the assertion of the external EJ_DINT input or by setting the EjtagBrk bit in the ECR register.	0xBFC0_0480	—	DINT	—	—
NMI	Assertion of NMI signal.	0xBFC0_0000	BEV, NMI, ERL	—	—	_nmi_handler
Machine Check	TLB write that conflicts with an existing entry.	EBASE+0x180	MCHECK, EXL	—	0x18	_general_exception_handler
Interrupt	Assertion of unmasked hardware or software interrupt signal.	See Table 7-2.	IPL<2:0>	—	0x00	See Table 7-2.
Deferred Watch	Deferred watch (unmasked by K|DM=>!(K|DM) transition).	EBASE+0x180	WP, EXL	—	0x17	_general_exception_handler
DIB	EJTAG debug hardware instruction break matched.	0xBFC0_0480	—	DIB	—	—
WATCH	A reference to an address that is in one of the Watch registers (fetch).	EBASE+0x180	EXL	—	0x17	_general_exception_handler
AdEL	Fetch address alignment error. Fetch reference to protected address.	EBASE+0x180	EXL	—	0x04	_general_exception_handler
TLBL	Fetch TLB miss or fetch TLB hit to page with V = 0.	EBASE if Status.EXL = 0	—	—	0x02	—
		EBASE+0x180 if Status.EXL == 1	—	—	0x02	_general_exception_handler
TLBL Execute Inhibit	An instruction fetch matched a valid TLB entry that had the XI bit set.	EBASE+0x180	EXL	—	0x14	_general_exception_handler
IBE	Instruction fetch bus error.	EBASE+0x180	EXL	—	0x06	_general_exception_handler

REGISTER 11-8: USBIENCSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 1-7) (CONTINUED)

bit 23 **INCOMPTX:** Incomplete TX Status bit (Device mode)

1 = For high-bandwidth Isochronous endpoint, a large packet has been split into 2 or 3 packets for transmission but insufficient IN tokens have been received to send all the parts

0 = Normal operation

In anything other than isochronous transfers, this bit will always return 0.

NAKTMOUT: NAK Time-out status bit (Host mode)

1 = TX endpoint is halted following the receipt of NAK responses for longer than the NAKLIM setting

0 = Written by software to clear this bit

bit 22 **CLRDT:** Clear Data Toggle Control bit

1 = Resets the endpoint data toggle to 0

0 = Do not clear the data toggle

bit 21 **SENTSTALL:** STALL handshake transmission status bit (Device mode)

1 = STALL handshake is transmitted. The FIFO is flushed and the TXPKTRDY bit is cleared.

0 = Written by software to clear this bit

RXSTALL: STALL receipt bit (Host mode)

1 = STALL handshake is received. Any DMA request in progress is stopped, the FIFO is completely flushed and the TXPKTRDY bit is cleared.

0 = Written by software to clear this bit

bit 20 **SENDSTALL:** STALL handshake transmission control bit (Device mode)

1 = Issue a STALL handshake to an IN token

0 = Terminate stall condition

This bit has no effect when the endpoint is being used for Isochronous transfers.

SETUPPKT: Definition bit (Host mode)

1 = When set at the same time as the TXPKTRDY bit is set, send a SETUP token instead of an OUT token for the transaction. This also clears the Data Toggle.

0 = Normal OUT token for the transaction

bit 19 **FLUSH:** FIFO Flush control bit

1 = Flush the latest packet from the endpoint TX FIFO. The FIFO pointer is reset, TXPKTRDY is cleared and an interrupt is generated.

0 = Do not flush the FIFO

bit 18 **UNDERRUN:** Underrun status bit (Device mode)

1 = An IN token has been received when TXPKTRDY is not set.

0 = Written by software to clear this bit.

ERROR: Handshake failure status bit (Host mode)

1 = Three attempts have been made to send a packet and no handshake packet has been received

0 = Written by software to clear this bit.

bit 17 **FIFONE:** FIFO Not Empty status bit

1 = There is at least 1 packet in the TX FIFO

0 = TX FIFO is empty

bit 16 **TXPKTRDY:** TX Packet Ready Control bit

The software sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. This bit is also automatically cleared prior to loading a second packet into a double-buffered FIFO.

REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)

bit 26 **DATATWEN:** Data Toggle Write Enable Control bit (*Host mode*)
1 = DATATGGL can be written
0 = DATATGGL is not writable

bit 25 **DATATGGL:** Data Toggle bit (*Host mode*)
When read, this bit indicates the current state of the endpoint data toggle.
If DATATWEN = 1, this bit may be written with the required setting of the data toggle.
If DATATWEN = 0, any value written to this bit is ignored.

bit 24 **INCOMPRX:** Incomplete Packet Status bit
1 = The packet in the RX FIFO during a high-bandwidth Isochronous/Interrupt transfer is incomplete because parts of the data were not received
0 = Written by then software to clear this bit
In anything other than Isochronous transfer, this bit will always return 0.

bit 23 **CLRDT:** Clear Data Toggle Control bit
1 = Reset the endpoint data toggle to 0
0 = Leave endpoint data toggle alone

bit 22 **SENTSTALL:** STALL Handshake Status bit (*Device mode*)
1 = STALL handshake is transmitted
0 = Written by the software to clear this bit

RXSTALL: STALL Handshake Receive Status bit (*Host mode*)
1 = A STALL handshake has been received. An interrupt is generated.
0 = Written by the software to clear this bit

bit 21 **SENDSTALL:** STALL Handshake Control bit (*Device mode*)
1 = Issue a STALL handshake
0 = Terminate stall condition

REQPKT: IN Transaction Request Control bit (*Host mode*)
1 = Request an IN transaction.
0 = No request
This bit is cleared when RXPKTRDY is set.

bit 20 **FLUSH:** Flush FIFO Control bit
1 = Flush the next packet to be read from the endpoint RX FIFO. The FIFO pointer is reset and the RXPKTRDY bit is cleared. This should only be used when RXPKTRDY is set. If the FIFO is double-buffered, FLUSH may need to be set twice to completely clear the FIFO.
0 = Normal FIFO operation
This bit is automatically cleared.

bit 19 **DATAERR:** Data Packet Error Status bit (*Device mode*)
1 = The data packet has a CRC or bit-stuff error.
0 = No data error
This bit is cleared when RXPKTRDY is cleared. This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.

DERRNAKT: Data Error/NAK Time-out Status bit (*Host mode*)
1 = The data packet has a CRC or bit-stuff error. In Bulk mode, the RX endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK limit.
0 = No data or NAK time-out error

13.0 TIMER1

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MZ EF devices feature one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the Low-Power Secondary Oscillator (SOSC) for real-time clock applications.

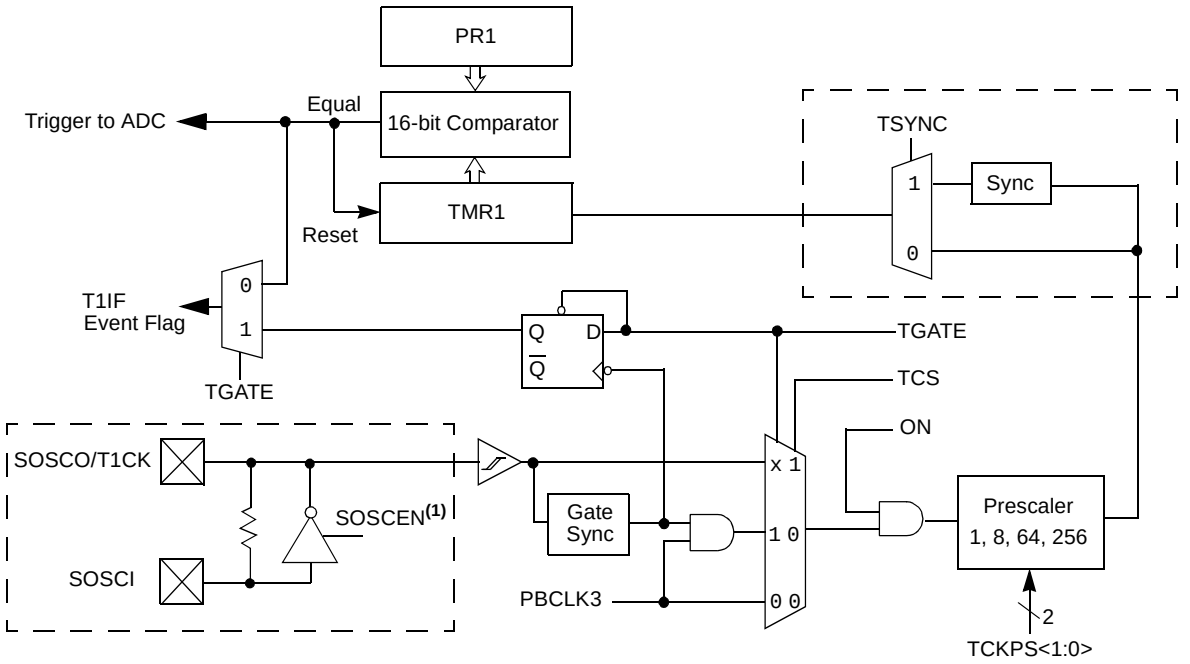
The following modes are supported by Timer1:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

13.1 Additional Supported Features

- Selectable clock prescaler
- Timer operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the SOSC to function as a real-time clock
- ADC event trigger

FIGURE 13-1: TIMER1 BLOCK DIAGRAM



Note 1: The default state of the SOSCEN bit (OSCCON<1>) during a device Reset is controlled by the FSOSCEN bit in Configuration Word, DEVCFG1.

REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON(1)	—	SIDL(2)	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
	TGATE(1)	TCKPS<2:0>(1)			T32(3)	—	TCS(1)	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit(1)
- 1 = Module is enabled
- 0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit(2)
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation even in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit(1)

When TCS = 1:
This bit is ignored and is read as '0'.

When TCS = 0:
- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits(1)
- 111 = 1:256 prescale value
- 110 = 1:64 prescale value
- 101 = 1:32 prescale value
- 100 = 1:16 prescale value
- 011 = 1:8 prescale value
- 010 = 1:4 prescale value
- 001 = 1:2 prescale value
- 000 = 1:1 prescale value

bit 3 **T32:** 32-Bit Timer Mode Select bit(3)
- 1 = Odd numbered and even numbered timers form a 32-bit timer
- 0 = Odd numbered and even numbered timers form separate 16-bit timers

Note 1: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, Timer5, Timer7, and Timer9). All timer functions are set through the even numbered timers.

2: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

3: This bit is available only on even numbered timers (Timer2, Timer4, Timer6, and Timer8).

NOTES:

REGISTER 20-7: SQI1INTTHR: SQI INTERRUPT THRESHOLD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TXINTTHR<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RXINTTHR<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **TXINTTHR<4:0>:** Transmit Interrupt Threshold bits

A transmit interrupt is set when the transmit FIFO has more space than the set number of bytes. For 16-bit mode, the value should be a multiple of 2.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RXINTTHR<4:0>:** Receive Interrupt Threshold bits

A receive interrupt is set when the receive FIFO count is larger than or equal to the set number of bytes. For 16-bit mode, the value should be multiple of 2.

23.1 PMP Control Registers

TABLE 23-1: PARALLEL MASTER PORT REGISTER MAP

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
E000	PMCON	31:16	—	—	—	—	—	—	—	—	RDSTART	—	—	—	—	—	DUALBUF	—	0000
		15:0	ON	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN	CSF<1:0>		ALP	CS2P	CS1P	—	WRSP	RDSP	0000
E010	PMMODE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>		WAITB<1:0>		WAITM<3:0>				WAITE<1:0>		0000
E020	PMADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CS2	CS1	ADDR<13:0>														0000
			ADDR15	ADDR14															0000
E030	PMDOUT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DATAOUT<15:0>																0000
E040	PMDIN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DATAIN<15:0>																0000
E050	PMAEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PTEN<15:0>																0000
E060	PMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F
E070	PMWADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WCS2	WCS1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
			WADDR15	WADDR14	WADDR<13:0>														0000
E080	PMRADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RCS2	RCS1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
			RADDR15	RADDR14	RADDR<13:0>														0000
E090	PMRDIN	31:16	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	15:0	RDATAIN<15:0>															0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

TABLE 28-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B04C	ADCCMP3	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B050	ADCCMPEN4	31:16	CMPE31(1)	CMPE30(1)	CMPE29(1)	CMPE28(1)	CMPE27(1)	CMPE26(1)	CMPE25(1)	CMPE24(1)	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19(1)	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B054	ADCCMP4	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B058	ADCCMPEN5	31:16	CMPE31(1)	CMPE30(1)	CMPE29(1)	CMPE28(1)	CMPE27(1)	CMPE26(1)	CMPE25(1)	CMPE24(1)	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19(1)	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B05C	ADCCMP5	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B060	ADCCMPEN6	31:16	CMPE31(1)	CMPE30(1)	CMPE29(1)	CMPE28(1)	CMPE27(1)	CMPE26(1)	CMPE25(1)	CMPE24(1)	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19(1)	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B064	ADCCMP6	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B068	ADCFLTR1	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B06C	ADCFLTR2	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B070	ADCFLTR3	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B074	ADCFLTR4	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B078	ADCFLTR5	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B07C	ADCFLTR6	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B080	ADCTRG1	31:16	—	—	—	TRGSRC3<4:0>					—	—	—	TRGSRC2<4:0>					0000
		15:0	—	—	—	TRGSRC1<4:0>					—	—	—	TRGSRC0<4:0>					0000
B084	ADCTRG2	31:16	—	—	—	TRGSRC7<4:0>					—	—	—	TRGSRC6<4:0>					0000
		15:0	—	—	—	TRGSRC5<4:0>					—	—	—	TRGSRC4<4:0>					0000
B088	ADCTRG3	31:16	—	—	—	TRGSRC11<4:0>					—	—	—	TRGSRC10<4:0>					0000
		15:0	—	—	—	TRGSRC9<4:0>					—	—	—	TRGSRC8<4:0>					0000
B0A0	ADCCMPCON1	31:16	CVDDATA<15:0>																0000
		15:0	—	—	AINID<5:0>						ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0A4	ADCCMPCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0A8	ADCCMPCON3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000

Note 1: This bit or register is not available on 64-pin devices.
2: This bit or register is not available on 64-pin and 100-pin devices.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

REGISTER 28-6: ADCIMCON2: ADC INPUT MODE CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF31(1)	SIGN31(1)	DIFF30(1)	SIGN30(1)	DIFF29(1)	SIGN29(1)	DIFF28(1)	SIGN28(1)
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF27(1)	SIGN27(1)	DIFF26(1)	SIGN26(1)	DIFF25(1)	SIGN25(1)	DIFF24(1)	SIGN24(1)
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF23(1)	SIGN23(1)	DIFF22(1)	SIGN22(1)	DIFF21(1)	SIGN21(1)	DIFF20(1)	SIGN20(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF19(1)	SIGN19(1)	DIFF18	SIGN18	DIFF17	SIGN17	DIFF16	SIGN16

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **DIFF31:** AN31 Mode bit(1)
1 = AN31 is using Differential mode
0 = AN31 is using Single-ended mode

bit 30 **SIGN31:** AN31 Signed Data Mode bit(1)
1 = AN31 is using Signed Data mode
0 = AN31 is using Unsigned Data mode

bit 29 **DIFF30:** AN30 Mode bit(1)
1 = AN30 is using Differential mode
0 = AN30 is using Single-ended mode

bit 28 **SIGN30:** AN30 Signed Data Mode bit(1)
1 = AN30 is using Signed Data mode
0 = AN30 is using Unsigned Data mode

bit 27 **DIFF29:** AN29 Mode bit(1)
1 = AN29 is using Differential mode
0 = AN29 is using Single-ended mode

bit 26 **SIGN29:** AN29 Signed Data Mode bit(1)
1 = AN29 is using Signed Data mode
0 = AN29 is using Unsigned Data mode

bit 25 **DIFF28:** AN28 Mode bit(1)
1 = AN28 is using Differential mode
0 = AN28 is using Single-ended mode

bit 24 **SIGN28:** AN28 Signed Data Mode bit(1)
1 = AN28 is using Signed Data mode
0 = AN28 is using Unsigned Data mode

bit 23 **DIFF27:** AN27 Mode bit(1)
1 = AN27 is using Differential mode
0 = AN27 is using Single-ended mode

bit 22 **SIGN27:** AN27 Signed Data Mode bit(1)
1 = AN27 is using Signed Data mode
0 = AN27 is using Unsigned Data mode

Note 1: This bit is not available on 64-pin devices.

REGISTER 30-1: ETHCON1: ETHERNET CONTROLLER CONTROL REGISTER 1 (CONTINUED)

bit 7 **AUTOFC:** Automatic Flow Control bit

1 = Automatic Flow Control enabled
0 = Automatic Flow Control disabled

Setting this bit will enable automatic Flow Control. If set, the full and empty watermarks are used to automatically enable and disable the Flow Control, respectively. When the number of received buffers BUFCNT (ETHSTAT<16:23>) rises to the full watermark, Flow Control is automatically enabled. When the BUFCNT falls to the empty watermark, Flow Control is automatically disabled.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **MANFC:** Manual Flow Control bit

1 = Manual Flow Control is enabled
0 = Manual Flow Control is disabled

Setting this bit will enable manual Flow Control. If set, the Flow Control logic will send a PAUSE frame using the PAUSE timer value in the PTV register. It will then resend a PAUSE frame every 128 * PTV<15:0>/2 TX clock cycles until the bit is cleared.

Note: For 10 Mbps operation, TX clock runs at 2.5 MHz. For 100 Mbps operation, TX clock runs at 25 MHz.

When this bit is cleared, the Flow Control logic will automatically send a PAUSE frame with a 0x0000 PAUSE timer value to disable Flow Control.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **BUFCDEC:** Descriptor Buffer Count Decrement bit

The BUFCDEC bit is a write-1 bit that reads as '0'. When written with a '1', the Descriptor Buffer Counter, BUFCNT, will decrement by one. If BUFCNT is incremented by the RX logic at the same time that this bit is written, the BUFCNT value will remain unchanged. Writing a '0' will have no effect.

This bit is only used for RX operations.

Note 1: It is not recommended to clear the RXEN bit and then make changes to any RX related field/register. The Ethernet Controller must be reinitialized (ON cleared to '0'), and then the RX changes applied.

REGISTER 30-3: ETHTXST: ETHERNET CONTROLLER TX PACKET DESCRIPTOR START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXSTADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXSTADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXSTADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	TXSTADDR<7:2>						—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-2 **TXSTADDR<31:2>:** Starting Address of First Transmit Descriptor bits
This register should not be written while any transmit, receive or DMA operations are in progress.
This address must be 4-byte aligned (bits 1-0 must be '00').

bit 1-0 **Unimplemented:** Read as '0'

Note 1: This register is only used for TX operations.
2: This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

REGISTER 30-4: ETHRXST: ETHERNET CONTROLLER RX PACKET DESCRIPTOR START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXSTADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXSTADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXSTADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	RXSTADDR<7:2>						—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-2 **RXSTADDR<31:2>:** Starting Address of First Receive Descriptor bits
This register should not be written while any transmit, receive or DMA operations are in progress.
This address must be 4-byte aligned (bits 1-0 must be '00').

bit 1-0 **Unimplemented:** Read as '0'

Note 1: This register is only used for RX operations.
2: This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

36.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

36.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

36.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

36.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

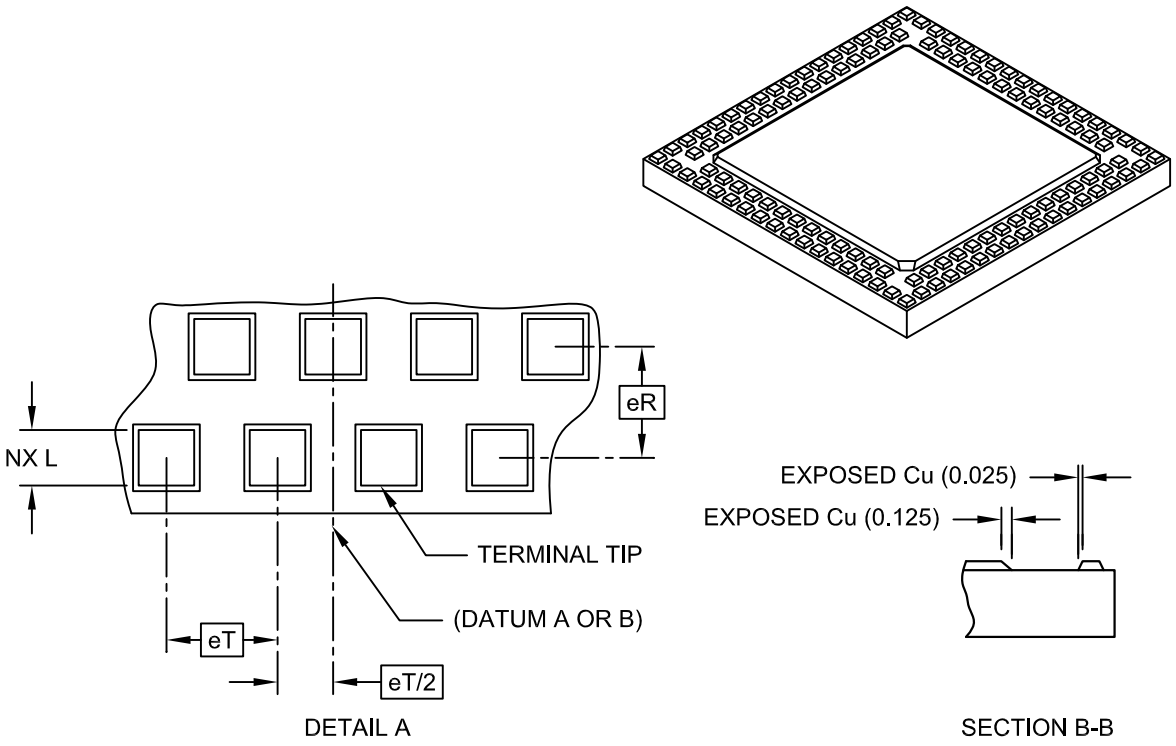
TABLE 37-36: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	**Symbol**	**Characteristics**		**Min.**	**Max.**	**Units**	**Conditions**
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 1)**	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 1)**	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode **(Note 1)**	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	—
			400 kHz mode	0	0.9	µs	
			1 MHz mode **(Note 1)**	0	0.3	µs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	250	—	ns	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	250	—	ns	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	600	—	ns	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	250		ns	
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	—
			400 kHz mode	0	1000	ns	
			1 MHz mode **(Note 1)**	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode **(Note 1)**	0.5	—	µs	
IS50	CB	Bus Capacitive Loading		—	—	pF	See parameter DO58

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		124	
Pitch	eT		0.50 BSC	
Pitch (Inner to outer terminal ring)	eR		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	-	0.05
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	6.40	6.55	6.70
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	6.40	6.55	6.70
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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TABLE A-10: PERIPHERAL DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Ethernet	
	On PIC32MZ EF devices, the input clock divider for the Ethernet module has expanded options to accommodate the faster peripheral bus clock.
CLKSEL<3:0> (EMAC1MCFG<5:2>) 1000 = SYSCLK divided by 40 0111 = SYSCLK divided by 28 0110 = SYSCLK divided by 20 0101 = SYSCLK divided by 14 0100 = SYSCLK divided by 10 0011 = SYSCLK divided by 8 0010 = SYSCLK divided by 6 000x = SYSCLK divided by 4	CLKSEL<3:0> (EMAC1MCFG<5:2>) **1010 = PBCLK5 divided by 50** **1001 = PBCLK5 divided by 48** 1000 = PBCLK5 divided by 40 0111 = PBCLK5 divided by 28 0110 = PBCLK5 divided by 20 0101 = PBCLK5 divided by 14 0100 = PBCLK5 divided by 10 0011 = PBCLK5 divided by 8 0010 = PBCLK5 divided by 6 000x = PBCLK5 divided by 4
Comparator/Comparator Voltage Reference	
On PIC32MX devices, it was possible to select the VREF+ pin as the output to the CVREFOUT pin. VREFSEL (CVRCON<10>) 1 = CVREF = VREF+ 0 = CVREF is generated by the resistor network	On PIC32MZ EF devices, the CVREFOUT pin must come from the resistor network. This bit is not available.
On PIC32MX devices, the internal voltage reference (IVREF) could be chosen by the BGSEL<1:0> bits. BGSEL<1:0> (CVRCON<9:8>) 11 = IVREF = VREF+ 10 = Reserved 01 = IVREF = 0.6V (nominal, default) 00 = IVREF = 1.2V (nominal)	On PIC32MZ EF devices, IVREF is fixed and cannot be changed. These bits are not available.
Change Notification	
On PIC32MX devices, Change Notification is controlled by the **CNCON, CNEN, and CNPUE** registers.	On PIC32MZ EF devices, Change Notification functionality has been relocated into each I/O port and is controlled by the **CNPUx, CNPDx, CNCONx, CNENx, and CNSTATx** registers.
System Bus	
On PIC32MX devices, the System Bus registers can be used to configure RAM memory for data and program memory partitions, cacheability of Flash memory, and RAM Wait states. These registers are: **BMXCON, BMXDKPBA, BMXDUDBA, BMXDUPBA, BMXPUPBA, BMXDRMSZ, BMXPFMSZ, and BMXBOOTSZ.**	On PIC32MZ EF devices, a new System Bus is utilized that supports using RAM memory for program or data without the need for special configuration. Therefore, no special registers are associated with the System Bus to configure these features.
On PIC32MX devices, various arbitration modes are used as initiators on the System Bus. These modes can be selected by the **BMXARB<2:0> (BMXCON<2:0>)** bits.	On PIC32MZ EF devices, a new arbitration scheme has been implemented on the System Bus. All initiators use the Least Recently Serviced (LRS) scheme, with the exception of the DMA, CPU, and the Flash Controller. The Flash Controller always has High priority over LRS initiators. The DMA and CPU (when servicing an interrupt) can be selected to have LRS or High priority using the **DMAPRI (CFGCON<25>)** and **CPUPRI (CFGCON<24>)** bits.

APPENDIX C: REVISION HISTORY

Revision A (January 2015)

This is the initial released version of the document.

Revision B (July 2015)

The document status was updated from Advance Information to Preliminary.

The revision includes the following major changes, which are referenced by their respective chapter in Table C-1.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE C-1: MAJOR SECTION UPDATES

Section Name	Update Description
32-bit MCUs (up to 2 MB Live-Update Flash and 512 KB SRAM) with FPU, Audio and Graphics Interfaces, HS USB, Ethernet, and Advanced Analog	The Operating Conditions were updated to: 2.1V to 3.6V.
4.0 "Memory Organization"	Legal information on the System Bus was added (see **4.2 "System Bus Arbitration"**).
5.0 "Flash Program Memory"	The BOOTSWAP bit in the NVMCON register was changed to: BFSWAP (see Register 5-1).
6.0 "Resets"	The NVMLTA bit was removed from the RCON register (see Register 6-1). The GNMI bit was added to the RNMICON register (see Register 6-3).
7.0 "CPU Exceptions and Interrupt Controller"	The ADC FIFO Data Ready Interrupt, IRQ 45, was added (see Table 7-2). ADC FIFO bits were added, and Note 7 regarding devices without a Crypto module was added to the Interrupt Register Map (see Table 7-3). The NMIKEY<7:0> bits were added to the INTCON register (see Register 7-1).
8.0 "Oscillator Configuration"	The SPLLRDY bit was removed and the SPLLDIVRDY bit was added to the CLKSTAT register (see Register 8-8
11.0 "Hi-Speed USB with On-The-Go (OTG)"	The VBUSIE and VBUSIF bits were changed to: VBUSERRIE and VBUSERRIF, respectively in the USBCSR2 register (see Register 11-3).
15.0 "Deadman Timer (DMT)"	The POR values were updated for the PSCNT<4:0> bits in the Post Status Configure DMT Count Status register (see Register 15-6). The POR values were updated for the PSINTV<2:0> bits in the Post Status Configure DMT Interval Status register (see Register 15-7).
16.0 "Watchdog Timer (WDT)"	The WDTCON register was updated (see Register 16-1).
23.0 "Parallel Master Port (PMP)"	The PMDOUT, PMDIN, and PMRDIN registers were added (see Register 23-4, Register 23-4, and Register 23-10). The PMADDR, PMWADDR, and PMRADDR registers were updated (see Register 23-3, Register 23-8, and Register 23-9). The PMRDATA register was removed.
24.0 "External Bus Interface (EBI)"	Reset values for the EBIMSK2, EBIMSK3, EBISMT0-EBISMT2, and EBIFTRPD registers were updated in the EBI Register Map (see Table 24-2). POR value changes were implemented to the EBI Static Memory Timing Register (see Register 24-3).