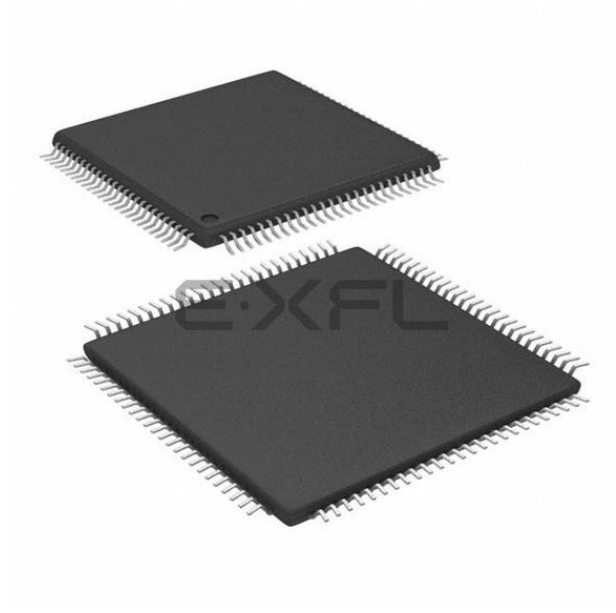
Microchip Technology - PIC32MZ1024EFE100-I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efe100-i-pt

The System Bus arbitration scheme implements a non-programmable, Least Recently Serviced (LRS) priority, which provides Quality Of Service (QOS) for most initiators. However, some initiators can use Fixed High Priority (HIGH) arbitration to guarantee their access to data.

The arbitration scheme for the available initiators is shown in Table 4-5.

TABLE 4-5: INITIATOR ID AND QOS

Name	ID	QOS
CPU	1	LRS(1)
CPU	2	HIGH(1,2)
DMA Read	3	LRS(1)
DMA Read	4	HIGH(1,2)
DMA Write	5	LRS(1)
DMA Write	6	HIGH(1,2)
USB	7	LRS
Ethernet Read	8	LRS
Ethernet Write	9	LRS
CAN1	10	LRS
CAN2	11	LRS
SQI1	12	LRS
Flash Controller	13	HIGH(2)
Crypto	14	LRS

Note 1: When accessing SRAM, the DMAPRI bit (CFGCON<25>) and the CPUPRI bit (CFGCON<24>) provide arbitration control for the DMA and CPU (when servicing an interrupt (i.e., EXL = 1)), respectively, by selecting the use of LRS or HIGH When using HIGH, the DMA and CPU get arbitration preference over all initiators using LRS.

2: Using HIGH arbitration can have serious negative effects on other initiators. Therefore, it is recommended to not enable this type of arbitration for an initiator that uses significant system bandwidth. HIGH arbitration is intended to be used for low bandwidth applications that require low latency, such as LCC graphics applications.

4.3 Permission Access and System Bus Registers

The System Bus on PIC32MZ EF family of microcontrollers provides access control capabilities for the transaction initiators on the System Bus.

The System Bus divides the entire memory space into fourteen target regions and permits access to each target by initiators via permission groups. Four Permission Groups (0 through 3) can be assigned to each initiator. Each permission group is independent of the others and can have exclusive or shared access to a region.

Using the CFGPG register (see Register 34-10 in **Section 34.0 “Special Features”**), Boot firmware can assign a permission group to each initiator, which can make requests on the System Bus.

The available targets and their regions, as well as the associated control registers to assign protection, are described and listed in Table 4-6.

Register 4-2 through Register 4-10 are used for setting and controlling access permission groups and regions.

To change these registers, they must be unlocked in hardware. The register lock is controlled by the PGLOCK Configuration bit (CFGCON<11>). Setting PGLOCK prevents writes to the control registers; clearing PGLOCK allows writes.

To set or clear the PGLOCK bit, an unlock sequence must be executed. Refer to **Section 42. “Oscillators with Enhanced PLL”** in the *“PIC32 Family Reference Manual”* for details.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
01F0	IPC11	31:16	—	—	—	ADCDC2IP<2:0>			ADCDC2IS<1:0>		—	—	—	ADCDC1IP<2:0>			ADCDC1IS<1:0>		0000
		15:0	—	—	—	ADCFIFOIP<2:0>			ADCFIFOIS<1:0>		—	—	—	ADCIP<2:0>			ADCIS<1:0>		0000
0200	IPC12	31:16	—	—	—	ADCDC6IP<2:0>			ADCDC6IS<1:0>		—	—	—	ADCDC5IP<2:0>			ADCDC5IS<1:0>		0000
		15:0	—	—	—	ADCDC4IP<2:0>			ADCDC4IS<1:0>		—	—	—	ADCDC3IP<2:0>			ADCDC3IS<1:0>		0000
0210	IPC13	31:16	—	—	—	ADCDF4IP<2:0>			ADCDF4IS<1:0>		—	—	—	ADCDF3IP<2:0>			ADCDF3IS<1:0>		0000
		15:0	—	—	—	ADCDF2IP<2:0>			ADCDF2IS<1:0>		—	—	—	ADCDF1IP<2:0>			ADCDF1IS<1:0>		0000
0220	IPC14	31:16	—	—	—	ADCD0IP<2:0>			ADCD0IS<1:0>		—	—	—	ADCDFLTIP<2:0>			ADCDFLTIS<1:0>		0000
		15:0	—	—	—	ADCDF6IP<2:0>			ADCDF6IS<1:0>		—	—	—	ADCDF5IP<2:0>			ADCDF5IS<1:0>		0000
0230	IPC15	31:16	—	—	—	ADCD4IP<2:0>			ADCD4IS<1:0>		—	—	—	ADCD3IP<2:0>			ADCD3IS<1:0>		0000
		15:0	—	—	—	ADCD2IP<2:0>			ADCD2IS<1:0>		—	—	—	ADCD1IP<2:0>			ADCD1IS<1:0>		0000
0240	IPC16	31:16	—	—	—	ADCD8IP<2:0>			ADCD8IS<1:0>		—	—	—	ADCD7IP<2:0>			ADCD7IS<1:0>		0000
		15:0	—	—	—	ADCD6IP<2:0>			ADCD6IS<1:0>		—	—	—	ADCD5IP<2:0>			ADCD5IS<1:0>		0000
0250	IPC17	31:16	—	—	—	ADCD12IP<2:0>			ADCD12IS<1:0>		—	—	—	ADCD11IP<2:0>			ADCD11IS<1:0>		0000
		15:0	—	—	—	ADCD10IP<2:0>			ADCD10IS<1:0>		—	—	—	ADCD9IP<2:0>			ADCD9IS<1:0>		0000
0260	IPC18	31:16	—	—	—	ADCD16IP<2:0>			ADCD16IS<1:0>		—	—	—	ADCD15IP<2:0>			ADCD15IS<1:0>		0000
		15:0	—	—	—	ADCD14IP<2:0>			ADCD14IS<1:0>		—	—	—	ADCD13IP<2:0>			ADCD13IS<1:0>		0000
0270	IPC19	31:16	—	—	—	ADCD20IP<2:0>(2)			ADCD20IS<1:0>(2)		—	—	—	ADCD19IP<2:0>(2)			ADCD19IS<1:0>(2)		0000
		15:0	—	—	—	ADCD18IP<2:0>			ADCD18IS<1:0>		—	—	—	ADCD17IP<2:0>			ADCD17IS<1:0>		0000
0280	IPC20	31:16	—	—	—	ADCD24IP<2:0>(2)			ADCD24IS<1:0>(2)		—	—	—	ADCD23IP<2:0>(2)			ADCD23IS<1:0>(2)		0000
		15:0	—	—	—	ADCD22IP<2:0>(2)			ADCD22IS<1:0>(2)		—	—	—	ADCD21IP<2:0>(2)			ADCD21IS<1:0>(2)		0000
0290	IPC21	31:16	—	—	—	ADCD28IP<2:0>(2)			ADCD28IS<1:0>(2)		—	—	—	ADCD27IP<2:0>(2)			ADCD27IS<1:0>(2)		0000
		15:0	—	—	—	ADCD26IP<2:0>(2)			ADCD26IS<1:0>(2)		—	—	—	ADCD25IP<2:0>(2)			ADCD25IS<1:0>(2)		0000
02A0	IPC22	31:16	—	—	—	ADCD32IP<2:0>(2)			ADCD32IS<1:0>(2)		—	—	—	ADCD31IP<2:0>(2)			ADCD31IS<1:0>(2)		0000
		15:0	—	—	—	ADCD30IP<2:0>(2)			ADCD30IS<1:0>(2)		—	—	—	ADCD29IP<2:0>(2)			ADCD29IS<1:0>(2)		0000
02B0	IPC23	31:16	—	—	—	ADCD36IP<2:0>(2,4)			ADCD36IS<1:0>(2,4)		—	—	—	ADCD35IP<2:0>(2,4)			ADCD35IS<1:0>(2,4)		0000
		15:0	—	—	—	ADCD34IP<2:0>(2)			ADCD34IS<1:0>(2)		—	—	—	ADCD33IP<2:0>(2)			ADCD33IS<1:0>(2)		0000
02C0	IPC24	31:16	—	—	—	ADCD40IP<2:0>(2,4)			ADCD40IS<1:0>(2,4)		—	—	—	ADCD39IP<2:0>(2,4)			ADCD39IS<1:0>(2,4)		0000
		15:0	—	—	—	ADCD38IP<2:0>(2,4)			ADCD38IS<1:0>(2,4)		—	—	—	ADCD37IP<2:0>(2,4)			ADCD37IS<1:0>(2,4)		0000
02D0	IPC25	31:16	—	—	—	ADCD44IP<2:0>			ADCD44IS<1:0>		—	—	—	ADCD43IP<2:0>			ADCD43IS<1:0>		0000
		15:0	—	—	—	ADCD42IP<2:0>(2,4)			ADCD42IS<1:0>(2,4)		—	—	—	ADCD41IP<2:0>(2,4)			ADCD41IS<1:0>(2,4)		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
06EC	OFF107(7)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06F4	OFF109	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06F8	OFF110	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06FC	OFF111	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0700	OFF112	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0704	OFF113	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0708	OFF114	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
070C	OFF115	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0710	OFF116	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0714	OFF117	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0718	OFF118(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
071C	OFF119	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0720	OFF120	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0724	OFF121	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0728	OFF122	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
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3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

REGISTER 8-7: SLEWCON: OSCILLATOR SLEW CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	SYSDIV<3:0>(1)			
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-0
	—	—	—	—	—	SLWDIV<2:0>		
7:0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R-0, HS, HC
	—	—	—	—	—	UPEN	DNEN	BUSY

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 **Unimplemented:** Read as '0'

bit 19-16 **SYSDIV<3:0>:** System Clock Divide Control bits(1)

1111 = SYSCLK is divided by 16
1110 = SYSCLK is divided by 15
•
•
•
0010 = SYSCLK is divided by 3
0001 = SYSCLK is divided by 2
0000 = SYSCLK is not divided

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **SLWDIV<2:0>:** Slew Divisor Steps Control bits

These bits control the maximum division steps used when slewing during a frequency change.
111 = Steps are divide by 128, 64, 32, 16, 8, 4, 2, and then no divisor
110 = Steps are divide by 64, 32, 16, 8, 4, 2, and then no divisor
101 = Steps are divide by 32, 16, 8, 4, 2, and then no divisor
100 = Steps are divide by 16, 8, 4, 2, and then no divisor
011 = Steps are divide by 8, 4, 2, and then no divisor
010 = Steps are divide by 4, 2, and then no divisor
001 = Steps are divide by 2, and then no divisor
000 = No divisor is used during slewing

Note: The steps apply in reverse order (i.e., 2, 4, 8, etc.) during a downward frequency change.

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **UPEN:** Upward Slew Enable bit

1 = Slewing enabled for switching to a higher frequency
0 = Slewing disabled for switching to a higher frequency

bit 1 **DNEN:** Downward Slew Enable bit

1 = Slewing enabled for switching to a lower frequency
0 = Slewing disabled for switching to a lower frequency

bit 0 **BUSY:** Clock Switching Slewing Active Status bit

1 = Clock frequency is being actively slewed to the new frequency
0 = Clock switch has reached its final value

Note 1: The SYSDIV<3:0> bit settings are ignored if both UPEN and DNEN = 0, and SYSCLK will be divided by 1.

TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3028	USB FIFO2	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
302C	USB FIFO3	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3030	USB FIFO4	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3034	USB FIFO5	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3038	USB FIFO6	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
303C	USB FIFO7	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3060	USBOTG	31:16	—	—	—	RXDPB	RXFIFOSZ<3:0>				—	—	—	TXDPB	TXFIFOSZ<3:0>				0000
		15:0	—	—	—	—	—	—	TXEDMA	RXEDMA	BDEV	FSDEV	LSDEV	VBUS<1:0>		HOSTMODE	HOSTREQ	SESSION	0080
3064	USB FIFOA	31:16	—	—	—	RXFIFOAD<12:0>													0000
		15:0	—	—	—	TXFIFOAD<12:0>													0000
306C	USB HWVER	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC	VERMAJOR<4:0>					VERMINOR<9:0>										0800
3078	USB INFO	31:16	VPLEN<7:0>								WTCON<3:0>				WTID<3:0>				3C5C
		15:0	DMACHANS<3:0>				RAMBITS<3:0>				RXENDPTS<3:0>				TXENDPTS<3:0>				8C77
307C	USB EOFRST	31:16	—	—	—	—	—	—	NRSTX	NRST	LSEOF<7:0>								0072
		15:0	FSEOF<7:0>								HSEOF<7:0>								7780
3080	USB E0TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
3084	USB E0RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
3088	USB E1TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
308C	USB E1RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
3090	USB E2TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
3094	USB E2RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
3098	USB E3TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

REGISTER 11-8: USBIENCSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AUTOSET	ISO	MODE	DMAREQEN	FRCDATTG	DMAREQMD	—	—
		—					DATAWEN	DATATGGL
23:16	R/W-0, HS	R/W-0, HC	R/W-0, HS	R/W-0	R/W-0	R/W-0, HS	R/W-0	R/W-0, HC
	INCOMPTX	CLRDT	SENTSTALL	SENDSTALL	FLUSH	UNDERRUN	FIFONE	TXPKTRDY
	NAKTMOUT		RXSTALL	SETUPPKT		ERROR		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MULT<4:0>					TXMAXP<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXMAXP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **AUTOSET:** Auto Set Control bit

1 = TXPKTRDY will be automatically set when data of the maximum packet size (value in TXMAXP) is loaded into the TX FIFO. If a packet of less than the maximum packet size is loaded, then TXPKTRDY will have to be set manually.
0 = TXPKTRDY must be set manually for all packet sizes

bit 30 **ISO:** Isochronous TX Endpoint Enable bit (Device mode)

1 = Enables the endpoint for Isochronous transfers
0 = Disables the endpoint for Isochronous transfers and enables it for Bulk or Interrupt transfers.
This bit only has an effect in Device mode. In Host mode, it always returns zero.

bit 29 **MODE:** Endpoint Direction Control bit

1 = Endpoint is TX
0 = Endpoint is RX

This bit only has any effect where the same endpoint FIFO is used for both TX and RX transactions.

bit 28 **DMAREQEN:** Endpoint DMA Request Enable bit

1 = DMA requests are enabled for this endpoint
0 = DMA requests are disabled for this endpoint

bit 27 **FRCDATTG:** Force Endpoint Data Toggle Control bit

1 = Forces the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received.
0 = No forced behavior

bit 26 **DMAREQMD:** Endpoint DMA Request Mode Control bit

1 = DMA Request Mode 1
0 = DMA Request Mode 0

This bit must not be cleared either before or in the same cycle as the above DMAREQEN bit is cleared.

bit 25 **DATAWEN:** Data Toggle Write Enable bit (Host mode)

1 = Enable the current state of the TX Endpoint data toggle (DATATGGL) to be written
0 = Disables writing the DATATGGL bit

bit 24 **DATATGGL:** Data Toggle Control bit (Host mode)

When read, this bit indicates the current state of the TX Endpoint data toggle. If DATAWEN = 1, this bit may be written with the required setting of the data toggle. If DATAWEN = 0, any value written to this bit is ignored.

REGISTER 11-20: USBDMAINT: USB DMA INTERRUPT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS
	DMA8IF	DMA7IF	DMA6IF	DMA5IF	DMA4IF	DMA3IF	DMA2IF	DMA1IF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **DMAxIF:** DMA Channel 'x' Interrupt bit

1 = The DMA channel has an interrupt event
0 = No interrupt event

All bits are cleared on a read of the register.

REGISTER 11-28: USBLPMR1: USB LINK POWER MANAGEMENT CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	LPMERRIE	LPMRESIE	LPMACKIE	LPMNYIE	LPMSTIE	LPMTOIE
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC
	—	—	—	LPMNAK	LPMEN<1:0>		LPMRES	LPMXMT
15:8	R-0	R-0	R-0	R-0	U-0	U-0	U-0	R-0
	ENDPOINT<3:0>				—	—	—	RMTWAK
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	HIRD<3:0>				LNKSTATE<3:0>			

Legend:	HC = Hardware Cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29 **LPMERRIE:** LPM Error Interrupt Enable bit
1 = LPMERR interrupt is enabled
0 = LPMERR interrupt is disabled

bit 28 **LPMRESIE:** LPM Resume Interrupt Enable bit
1 = LPMRES interrupt is enabled
0 = LPMRES interrupt is disabled

bit 27 **LPMACKIE:** LPM Acknowledge Interrupt Enable bit
1 = Enable the LPMACK Interrupt
0 = Disable the LPMACK Interrupt

bit 26 **LPMNYIE:** LPM NYET Interrupt Enable bit
1 = Enable the LPMNYET Interrupt
0 = Disable the LPMNYET Interrupt

bit 25 **LPMSTIE:** LPM STALL Interrupt Enable bit
1 = Enable the LPMST Interrupt
0 = Disable the LPMST Interrupt

bit 24 **LPMTOIE:** LPM Time-out Interrupt Enable bit
1 = Enable the LPMTO Interrupt
0 = Disable the LPMTO Interrupt

bit 23-21 **Unimplemented:** Read as '0'

bit 20 **LPMNAK:** LPM-only Transaction Setting bit
1 = All endpoints will respond to all transactions other than a LPM transaction with a NAK
0 = Normal transaction operation
Setting this bit to '1' will only take effect after the USB module as been LPM suspended.

bit 19-18 **LPMEN<1:0>:** LPM Enable bits (*Device mode*)
11 = LPM Extended transactions are supported
10 = LPM and Extended transactions are not supported
01 = LPM mode is not supported but Extended transactions are supported
00 = LPM Extended transactions are supported

bit 17 **LPMRES:** LPM Resume bit
1 = Initiate resume (remote wake-up). Resume signaling is asserted for 50 µs.
0 = No resume operation
This bit is self-clearing.

TABLE 12-21: PORTK REGISTER MAP FOR 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0910	TRISK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRISK7	TRISK6	TRISK5	TRISK4	TRISK3	TRISK2	TRISK1	TRISK0	00FF
0920	PORTK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	RK7	RK6	RK5	RK4	RK3	RK2	RK1	RK0	xxxx
0930	LATK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LATK7	LATK6	LATK5	LATK4	LATK3	LATK2	LATK1	LATK0	xxxx
0940	ODCK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ODCK7	ODCK6	ODCK5	ODCK4	ODCK3	ODCK2	ODCK1	ODCK0	0000
0950	CNPUK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPUK7	CNPUK6	CNPUK5	CNPUK4	CNPUK3	CNPUK2	CNPUK1	CNPUK0	0000
0960	CNPDK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPDK7	CNPDK6	CNPDK5	CNPDK4	CNPDK3	CNPDK2	CNPDK1	CNPDK0	0000
0970	CNCONK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0980	CNENK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNENK7	CNENK6	CNENK5	CNENK4	CNENK3	CNENK2	CNENK1	CNENK0	0000
0990	CNSTATK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CN STATK7	CN STATK6	CN STATK5	CN STATK4	CN STATK3	CN STATK2	CN STATK1	CN STATK0	0000
09A0	CNNEK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNNEK7	CNNEK6	CNNEK5	CNNEK4	CNNEK3	CNNEK2	CNNEK1	CNNEK0	0000
09B0	CNFK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNFK7	CNFK6	CNFK5	CNFK4	CNFK3	CNFK2	CNFK1	CNFK0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

TABLE 12-22: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
14DC	SS6R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS6R<3:0>				0000
14E0	C1RXR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C1RXR<3:0>				0000
14E4	C2RXR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C2RXR<3:0>				0000
14E8	REFCLKI1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFCLKI1R<3:0>				0000
14F0	REFCLKI3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFCLKI3R<3:0>				0000
14F4	REFCLKI4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFCLKI4R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

2: This register is not available on devices without a CAN module.

TABLE 14-1: TIMER2 THROUGH TIMER9 REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0C10	TMR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR7<15:0>																0000
0C20	PR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR7<15:0>																FFFF
0E00	T8CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0E10	TMR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR8<15:0>																0000
0E20	PR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR8<15:0>																FFFF
1000	T9CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
1010	TMR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR9<15:0>																0000
1020	PR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR9<15:0>																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 20-25: SQI1XCON3: SQI XIP CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INIT1SCHECK	INIT1COUNT<1:0>		INIT1TYPE<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT1CMD3<7:0>(1)							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT1CMD2<7:0>(1)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT1CMD1<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **INIT1SCHECK:** Flash Initialization 1 Command Status Check bit
1 = Check the status after executing the INIT1 command
0 = Do not check the status

bit 27-26 **INIT1COUNT<1:0>:** Flash Initialization 1 Command Count bits
11 = INIT1CMD1, INIT1CMD2, and INIT1CMD3 are sent
10 = INIT1CMD1 and INIT1CMD2 are sent, but INIT1CMD3 is still pending
01 = INIT1CMD1 is sent, but INIT1CMD2 and INIT1CMD3 are still pending
00 = No commands are sent

bit 25-24 **INIT1TYPE<1:0>:** Flash Initialization 1 Command Type bits
11 = Reserved
10 = INIT1 commands are sent in Quad Lane mode
01 = INIT1 commands are sent in Dual Lane mode
00 = INIT1 commands are sent in Single Lane mode

bit 24-16 **INIT1CMD3<7:0>:** Flash Initialization Command 3 bits(1)
Third command of the Flash initialization.

bit 15-8 **INIT1CMD2<7:0>:** Flash Initialization Command 2 bits(1)
Second command of the Flash initialization.

bit 7-0 **INIT1CMD1<7:0>:** Flash Initialization Command 1 bits(1)
First command of the Flash initialization.

Note 1: INIT1CMD1 can be WEN and INIT1CMD2 can be SECTOR UNPROTECT.

Note:	Some Flash devices require Write Enable and Sector Unprotect commands before read/write operations and this register is useful in working with those Flash types (XIP mode only)

REGISTER 26-5: CESTAT: CRYPTO ENGINE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ERRMODE<2:0>			ERROP<2:0>			ERRPHASE<1:0>	
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	BDSTATE<3:0>				START	ACTIVE
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDCTRL<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDCTRL<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **ERRMODE<2:0>:** Internal Error Mode Status bits
- 111 = Reserved
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CEK operation
- 010 = KEK operation
- 001 = Preboot authentication
- 000 = Normal operation

bit 28-26 **ERROP<2:0>:** Internal Error Operation Status bits
- 111 = Reserved
- 110 = Reserved
- 101 = Reserved
- 100 = Authentication
- 011 = Reserved
- 010 = Decryption
- 001 = Encryption
- 000 = Reserved

bit 25-24 **ERRPHASE<1:0>:** Internal Error Phase of DMA Status bits
- 11 = Destination data
- 10 = Source data
- 01 = Security Association (SA) access
- 00 = Buffer Descriptor (BD) access

bit 23-22 **Unimplemented:** Read as '0'

bit 21-18 **BDSTATE<3:0>:** Buffer Descriptor Processor State Status bits

The current state of the BDP:
- 1111 = Reserved
- •
- •
- •
- 0111 = Reserved
- 0110 = SA fetch
- 0101 = Fetch BDP is disabled
- 0100 = Descriptor is done
- 0011 = Data phase
- 0010 = BDP is loading
- 0001 = Descriptor fetch request is pending
- 0000 = BDP is idle

bit 17 **START:** DMA Start Status bit
- 1 = DMA start has occurred
- 0 = DMA start has not occurred

TABLE 28-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B04C	ADCCMP3	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B050	ADCCMPEN4	31:16	CMPE31(1)	CMPE30(1)	CMPE29(1)	CMPE28(1)	CMPE27(1)	CMPE26(1)	CMPE25(1)	CMPE24(1)	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19(1)	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B054	ADCCMP4	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B058	ADCCMPEN5	31:16	CMPE31(1)	CMPE30(1)	CMPE29(1)	CMPE28(1)	CMPE27(1)	CMPE26(1)	CMPE25(1)	CMPE24(1)	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19(1)	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B05C	ADCCMP5	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B060	ADCCMPEN6	31:16	CMPE31(1)	CMPE30(1)	CMPE29(1)	CMPE28(1)	CMPE27(1)	CMPE26(1)	CMPE25(1)	CMPE24(1)	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19(1)	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B064	ADCCMP6	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B068	ADCFLTR1	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B06C	ADCFLTR2	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B070	ADCFLTR3	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B074	ADCFLTR4	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B078	ADCFLTR5	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B07C	ADCFLTR6	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B080	ADCTRG1	31:16	—	—	—	TRGSRC3<4:0>					—	—	—	TRGSRC2<4:0>					0000
		15:0	—	—	—	TRGSRC1<4:0>					—	—	—	TRGSRC0<4:0>					0000
B084	ADCTRG2	31:16	—	—	—	TRGSRC7<4:0>					—	—	—	TRGSRC6<4:0>					0000
		15:0	—	—	—	TRGSRC5<4:0>					—	—	—	TRGSRC4<4:0>					0000
B088	ADCTRG3	31:16	—	—	—	TRGSRC11<4:0>					—	—	—	TRGSRC10<4:0>					0000
		15:0	—	—	—	TRGSRC9<4:0>					—	—	—	TRGSRC8<4:0>					0000
B0A0	ADCCMPCON1	31:16	CVDDATA<15:0>																0000
		15:0	—	—	AINID<5:0>						ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0A4	ADCCMPCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0A8	ADCCMPCON3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000

Note 1: This bit or register is not available on 64-pin devices.
2: This bit or register is not available on 64-pin and 100-pin devices.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

REGISTER 28-2: ADCCON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BGVRRDY	REFFLT	EOSRDY	CVDCPL<2:0>			SAMC<9:8>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SAMC<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	BGVRIEN	REFFLTIEN	EOSIEN	ADCEIOVR	—	ADCEIS<2:0>		
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	ADCDIV<6:0>						

Legend:	HC = Hardware Set	HS = Hardware Cleared	r = Reserved
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **BGVRRDY:** Band Gap Voltage/ADC Reference Voltage Status bit

1 = Both band gap voltage and ADC reference voltages (V_{REF}) are ready
0 = Either or both band gap voltage and ADC reference voltages (V_{REF}) are not ready

Data processing is valid only after BGVRRDY is set by hardware, so the application code must check that the BGVRRDY bit is set to ensure data validity. This bit set to '0' when ON (ADCCON1<15>) = 0.

bit 30 **REFFLT:** Band Gap/V_{REF}/AV_{DD} BOR Fault Status bit

1 = Fault in band gap or the V_{REF} voltage while the ON bit (ADCCON1<15>) was set. Most likely a band gap or V_{REF} fault will be caused by a BOR of the analog V_{DD} supply.
0 = Band gap and V_{REF} voltage are working properly

This bit is cleared when the ON bit (ADCCON1<15>) = 0 and the BGVRRDY bit = 1.

bit 29 **EOSRDY:** End of Scan Interrupt Status bit

1 = All analog inputs are considered for scanning through the scan trigger (all analog inputs specified in the ADCCSS1 and ADCCSS2 registers) have completed scanning
0 = Scanning has not completed

This bit is cleared when ADCCON2<31:24> are read in software.

bit 28-26 **CVDCPL<2:0>:** Capacitor Voltage Divider (CVD) Setting bit

111 = 7 * 2.5 pF = 17.5 pF
110 = 6 * 2.5 pF = 15 pF
101 = 5 * 2.5 pF = 12.5 pF
100 = 4 * 2.5 pF = 10 pF
011 = 3 * 2.5 pF = 7.5 pF
010 = 2 * 2.5 pF = 5 pF
001 = 1 * 2.5 pF = 2.5 pF
000 = 0 * 2.5 pF = 0 pF

bit 25-16 **SAMC<9:0>:** Sample Time for the Shared ADC (ADC7) bits

1111111111 = 1025 T_{AD7}
•
•
•
0000000001 = 3 T_{AD7}
0000000000 = 2 T_{AD7}

Where T_{AD7} = period of the ADC conversion clock for the Shared ADC (ADC7) controlled by the ADCDIV<6:0> bits.

bit 15 **BGVRIEN:** Band Gap/V_{REF} Voltage Ready Interrupt Enable bit

1 = Interrupt will be generated when the BGVRDDY bit is set
0 = No interrupt is generated when the BGVRRDY bit is set

REGISTER 29-5: CiTREC: CAN TRANSMIT/RECEIVE ERROR COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	TERRCNT<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RERRCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21 **TXBO:** Transmitter in Error State Bus OFF (TERRCNT ≥ 256)

bit 20 **TXBP:** Transmitter in Error State Bus Passive (TERRCNT ≥ 128)

bit 19 **RXBP:** Receiver in Error State Bus Passive (RERRCNT ≥ 128)

bit 18 **TXWARN:** Transmitter in Error State Warning (128 > TERRCNT ≥ 96)

bit 17 **RXWARN:** Receiver in Error State Warning (128 > RERRCNT ≥ 96)

bit 16 **EWARN:** Transmitter or Receiver is in Error State Warning

bit 15-8 **TERRCNT<7:0>:** Transmit Error Counter

bit 7-0 **RERRCNT<7:0>:** Receive Error Counter

REGISTER 29-6: CiFSTAT: CAN FIFO STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **FIFOIP<31:0>:** FIFOx Interrupt Pending bits

1 = One or more enabled FIFO interrupts are pending

0 = No FIFO interrupts are pending

REGISTER 30-13: ETHIEN: ETHERNET CONTROLLER INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	TXBUSEIE(1)	RXBUSEIE(2)	—	—	—	EWMARKIE(2)	FWMARKIE(2)
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXDONEIE(2)	PKTPENDIE(2)	RXACTIE(2)	—	TXDONEIE(1)	TXABORTIE(1)	RXBUFNAIE(2)	RXOVFLWIE(2)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14 **TXBUSEIE:** Transmit BVCI Bus Error Interrupt Enable bit(1)
1 = Enable TXBUS Error Interrupt
0 = Disable TXBUS Error Interrupt

bit 13 **RXBUSEIE:** Receive BVCI Bus Error Interrupt Enable bit(2)
1 = Enable RXBUS Error Interrupt
0 = Disable RXBUS Error Interrupt

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **EWMARKIE:** Empty Watermark Interrupt Enable bit(2)
1 = Enable EWMARK Interrupt
0 = Disable EWMARK Interrupt

bit 8 **FWMARKIE:** Full Watermark Interrupt Enable bit(2)
1 = Enable FWMARK Interrupt
0 = Disable FWMARK Interrupt

bit 7 **RXDONEIE:** Receiver Done Interrupt Enable bit(2)
1 = Enable RXDONE Interrupt
0 = Disable RXDONE Interrupt

bit 6 **PKTPENDIE:** Packet Pending Interrupt Enable bit(2)
1 = Enable PKTPEND Interrupt
0 = Disable PKTPEND Interrupt

bit 5 **RXACTIE:** RX Activity Interrupt Enable bit
1 = Enable RXACT Interrupt
0 = Disable RXACT Interrupt

bit 4 **Unimplemented:** Read as '0'

bit 3 **TXDONEIE:** Transmitter Done Interrupt Enable bit(1)
1 = Enable TXDONE Interrupt
0 = Disable TXDONE Interrupt

bit 2 **TXABORTIE:** Transmitter Abort Interrupt Enable bit(1)
1 = Enable TXABORT Interrupt
0 = Disable TXABORT Interrupt

bit 1 **RXBUFNAIE:** Receive Buffer Not Available Interrupt Enable bit(2)
1 = Enable RXBUFNA Interrupt
0 = Disable RXBUFNA Interrupt

bit 0 **RXOVFLWIE:** Receive FIFO Overflow Interrupt Enable bit(2)
1 = Enable RXOVFLW Interrupt
0 = Disable RXOVFLW Interrupt

Note 1: This bit is only used for TX operations.
2: This bit is only used for RX operations.

TABLE 37-10: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
DI60a	IICL	**Input Low Injection Current**	0	—	-5(2,5)	mA	This parameter applies to all pins, with the exception of RB10. Maximum IICH current for this exception is 0 mA.
DI60b	IICH	**Input High Injection Current**	0	—	+5(3,4,5)	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, OSCI, OSCO, SOSCI, SOSCO, D+, D- and RB10. Maximum IICH current for these exceptions is 0 mA.
DI60c	∑IICT	**Total Input Injection Current (sum of all I/O and control pins)**	-20(6)	—	+20(6)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL + | IICH |) ≤ ∑IICT

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: VIL source < (VSS - 0.3). Characterized but not tested.

3: VIH source > (VDD + 0.3) for non-5V tolerant pins only.

4: Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any “positive” input injection current.

5: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

6: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. If **Note 2**, IICL = (((Vss - 0.3) - VIL source) / Rs). If **Note 3**, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

TABLE 37-20: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Internal FRC Accuracy @ 8.00 MHz(1)						
F20	FRC	-5	—	+5	%	0°C ≤ TA ≤ +85°C
		-8	—	+8	%	-40°C ≤ TA ≤ +85°C
		-10	—	+10	%	-40°C ≤ TA ≤ +125°C

Note 1: Frequency calibrated at +25°C and 3.3V. The TUN bits (OSCTUN<5:0>) can be used to compensate for temperature drift.

TABLE 37-21: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Internal LPRC @ 32.768 kHz(1)						
F21	LPRC	-8	—	+8	%	0°C ≤ TA ≤ +85°C
		-25	—	+25	%	-40°C ≤ TA ≤ +125°C

Note 1: Change of LPRC frequency as VDD changes.

TABLE 37-22: INTERNAL BACKUP FRC (BFRC) ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Internal BFRC Accuracy @ 8 MHz						
F22	BFRC	—	±30	—	%	—

39.0 252 MHz ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MZ EF electrical characteristics for devices running at 252 MHz. Additional information will be provided in future revisions of this document as it becomes available.

The specifications for 252 MHz are identical to those shown in **37.0 "Electrical Characteristics"** including absolute maximum ratings, with the exception of the parameters listed in this chapter.

Parameters in this chapter begin with the letter "M", which denotes 252 MHz operation. For example, parameter DC27a in **37.0 "Electrical Characteristics"**, is the up to 200 MHz operation equivalent for MDC27a.