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Details

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Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efe100t-i-pt

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

		Pin Nu	mber					
Pin Name	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP	Pin Type	Buffer Type	Description	
					Output	Compare		
OC1	PPS	PPS	PPS	PPS	0	—	Output Compare Outputs 1-9	
OC2	PPS	PPS	PPS	PPS	0	—		
OC3	PPS	PPS	PPS	PPS	0	—	1	
OC4	PPS	PPS	PPS	PPS	0	—	1	
OC5	PPS	PPS	PPS	PPS	0	—	1	
OC6	PPS	PPS	PPS	PPS	0	—	1	
OC7	PPS	PPS	PPS	PPS	0	—	1	
OC8	PPS	PPS	PPS	PPS	0	—	1	
OC9	PPS	PPS	PPS	PPS	0	—	1	
OCFA	PPS	PPS	PPS	PPS	I	ST	Output Compare Fault A Input	
OCFB	30	44	B24	62	I	ST	Output Compare Fault B Input	
Legend:	CMOS = C	MOS-comp	atible input	or output	-	Analog =	Analog input P = Power	

TABLE 1-4: OC1 THROUGH OC9 PINOUT I/O DESCRIPTIONS

d: CMOS = CMOS-compatible input or output ST = Schmitt Trigger input with CMOS levels TTL = Transistor-transistor Logic input buffer

Analog = Analog input	P = Power
O = Output	I = Input
PPS = Peripheral Pin Select	

TABLE 1-5: EXTERNAL INTERRUPTS PINOUT I/O DESCRIPTIONS

		Pin Nu	mber							
Pin Name	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP	Pin Type	Buffer Type	Description			
	External Interrupts									
INT0	46	71	A48	104	I	ST	External Interrupt 0			
INT1	PPS	PPS	PPS	PPS	I	ST	External Interrupt 1			
INT2	PPS	PPS	PPS	PPS	I	ST	External Interrupt 2			
INT3	PPS	PPS	PPS	PPS	I	ST	External Interrupt 3			
INT4	PPS	PPS	PPS	PPS	I	ST	External Interrupt 4			
Logond	CMOS = CI	MOS-comp	atible input		•	Analog -	Analog input P - Power			

Legend: CMOS = CMOS-compatible input or output ST = Schmitt Trigger input with CMOS levels TTL = Transistor-transistor Logic input buffer Analog = Analog inputP = PowerO = OutputI = InputPPS = Peripheral Pin Select

REGISTER 4-3: SBTxELOG1: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 1 ('x' = 0-13) (CONTINUED)

- bit 7-4 REGION<3:0>: Requested Region Number bits
 - 1111 0000 = Target's region that reported a permission group violation
- bit 3 Unimplemented: Read as '0'
- bit 2-0 CMD<2:0>: Transaction Command of the Requester bits
 - 111 = Reserved
 - 110 = Reserved
 - 101 = Write (a non-posted write)
 - 100 = Reserved
 - 011 = Read (a locked read caused by a Read-Modify-Write transaction)
 - 010 = Read
 - 001 = Write
 - 000 = Idle

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
45.0	R/W-0, HC	R/W-0	R-0, HS, HC	R-0, HS, HC	U-0	U-0	U-0	U-0
15:8	WR ⁽¹⁾	WREN ⁽¹⁾	WRERR ⁽¹⁾	LVDERR ⁽¹⁾	—	—	—	—
7.0	R/W-0	R/W-x	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	PFSWAP	BFSWAP	—	—		NVMOP	<3:0>	

REGISTER 5-1: NVMCON: FLASH PROGRAMMING CONTROL REGISTER

Legend:	HC = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 WR: Write Control bit⁽¹⁾

This bit cannot be cleared and can be set only when WREN = 1 and the unlock sequence has been performed.

- 1 = Initiate a Flash operation
- 0 = Flash operation is complete or inactive

bit 14 WREN: Write Enable bit⁽¹⁾

- 1 = Enable writes to the WR bit and disables writes to the NVMOP<3:0> bits
- 0 = Disable writes to WR bit and enables writes to the NVMOP<3:0> bits

bit 13 WRERR: Write Error bit⁽¹⁾

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.

- 1 = Program or erase sequence did not complete successfully
- 0 = Program or erase sequence completed normally

bit 12 LVDERR: Low-Voltage Detect Error bit⁽¹⁾

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation. 1 = Low-voltage detected (possible data corruption, if WRERR is set)

0 =Voltage level is acceptable for programming

bit 11-8 Unimplemented: Read as '0'

bit 7 **PFSWAP:** Program Flash Bank Swap Control bit

This bit is only writable when WREN = 0 and the unlock sequence has been performed.

- 1 = Program Flash Bank 2 is mapped to the lower mapped region and program Flash Bank 1 is mapped to the upper mapped region
- 0 = Program Flash Bank 1 is mapped to the lower mapped region and program Flash Bank 2 is mapped to the upper mapped region
- Note 1: These bits are only reset by a Power-on Reset (POR) and are not affected by other reset sources.
 - 2: This operation results in a "no operation" (NOP) when the Dynamic Flash ECC Configuration bits = 00 (FECCCON<1:0> (DVCFG0<9:8>)), which enables ECC at all times. For all other FECCCON<1:0> bit settings, this command will execute, but will not write the ECC bits for the word and can cause DED errors if dynamic Flash ECC is enabled (FECCCON<1:0> = 01). Refer to Section 52. "Flash Program Memory with Support for Live Update" (DS60001193) for information regarding ECC and Flash programming.

		IRQ		Interrupt Bit Location				Persistent
Interrupt Source ⁽¹⁾	XC32 Vector Name	#	Vector #	Flag	Enable	Priority	Sub-priority	Interrupt
ADC Data 19 ⁽²⁾	_ADC_DATA19_VECTOR	78	OFF078<17:1>	• IFS2<14>	IEC2<14>	IPC19<20:18>	IPC19<17:16>	Yes
ADC Data 20 ⁽²⁾	_ADC_DATA20_VECTOR	79	OFF079<17:1>	IFS2<15>	IEC2<15>	IPC19<28:26>	IPC19<25:24>	Yes
ADC Data 21 ⁽²⁾	_ADC_DATA21_VECTOR	80	OFF080<17:1>	IFS2<16>	IEC2<16>	IPC20<4:2>	IPC20<1:0>	Yes
ADC Data 22 ⁽²⁾	_ADC_DATA22_VECTOR	81	OFF081<17:1>	IFS2<17>	IEC2<17>	IPC20<12:10>	IPC20<9:8>	Yes
ADC Data 23 ⁽²⁾	_ADC_DATA23_VECTOR	82	OFF082<17:1>	IFS2<18>	IEC2<18>	IPC20<20:18>	IPC20<17:16>	Yes
ADC Data 24 ⁽²⁾	_ADC_DATA24_VECTOR	83	OFF083<17:1>	IFS2<19>	IEC2<19>	IPC20<28:26>	IPC20<25:24>	Yes
ADC Data 25 ⁽²⁾	_ADC_DATA25_VECTOR	84	OFF084<17:1>	IFS2<20>	IEC2<20>	IPC21<4:2>	IPC21<1:0>	Yes
ADC Data 26 ⁽²⁾	_ADC_DATA26_VECTOR	85	OFF085<17:1>	IFS2<21>	IEC2<21>	IPC21<12:10>	IPC21<9:8>	Yes
ADC Data 27 ⁽²⁾	_ADC_DATA27_VECTOR	86	OFF086<17:1>	IFS2<22>	IEC2<22>	IPC21<20:18>	IPC21<17:16>	Yes
ADC Data 28 ⁽²⁾	_ADC_DATA28_VECTOR	87	OFF087<17:1>	IFS2<23>	IEC2<23>	IPC21<28:26>	IPC21<25:24>	Yes
ADC Data 29 ⁽²⁾	_ADC_DATA29_VECTOR	88	OFF088<17:1>	IFS2<24>	IEC2<24>	IPC22<4:2>	IPC22<1:0>	Yes
ADC Data 30 ⁽²⁾	_ADC_DATA30_VECTOR	89	OFF089<17:1>	IFS2<25>	IEC2<25>	IPC22<12:10>	IPC22<9:8>	Yes
ADC Data 31 ⁽²⁾	_ADC_DATA31_VECTOR	90	OFF090<17:1>	IFS2<26>	IEC2<26>	IPC22<20:18>	IPC22<17:16>	Yes
ADC Data 32 ⁽²⁾	_ADC_DATA32_VECTOR	91	OFF091<17:1>	IFS2<27>	IEC2<27>	IPC22<28:26>	IPC22<25:24>	Yes
ADC Data 33 ⁽²⁾	_ADC_DATA33_VECTOR	92	OFF092<17:1>	IFS2<28>	IEC2<28>	IPC23<4:2>	IPC23<1:0>	Yes
ADC Data 34 ⁽²⁾	_ADC_DATA34_VECTOR	93	OFF093<17:1>	IFS2<29>	IEC2<29>	IPC23<12:10>	IPC23<9:8>	Yes
ADC Data 35 ^(2,3)	_ADC_DATA35_VECTOR	94	OFF094<17:1>	IFS2<30>	IEC2<30>	IPC23<20:18>	IPC23<17:16>	Yes
ADC Data 36 ^(2,3)	_ADC_DATA36_VECTOR	95	OFF095<17:1>	IFS2<31>	IEC2<31>	IPC23<28:26>	IPC23<25:24>	Yes
ADC Data 37 ^(2,3)	_ADC_DATA37_VECTOR	96	OFF096<17:1>	IFS3<0>	IEC3<0>	IPC24<4:2>	IPC24<1:0>	Yes
ADC Data 38 ^(2,3)	_ADC_DATA38_VECTOR	97	OFF097<17:1>	IFS3<1>	IEC3<1>	IPC24<12:10>	IPC24<9:8>	Yes
ADC Data 39 ^(2,3)	_ADC_DATA39_VECTOR	98	OFF098<17:1>	IFS3<2>	IEC3<2>	IPC24<20:18>	IPC24<17:16>	Yes
ADC Data 40 ^(2,3)	_ADC_DATA40_VECTOR	99	OFF099<17:1>	IFS3<3>	IEC3<3>	IPC24<28:26>	IPC24<25:24>	Yes
ADC Data 41 ^(2,3)	_ADC_DATA41_VECTOR	100	OFF100<17:1>	IFS3<4>	IEC3<4>	IPC25<4:2>	IPC25<1:0>	Yes
ADC Data 42 ^(2,3)	_ADC_DATA42_VECTOR	101	OFF101<17:1>	IFS3<5>	IEC3<5>	IPC25<12:10>	IPC25<9:8>	Yes
ADC Data 43	_ADC_DATA43_VECTOR	102	OFF102<17:1>	IFS3<6>	IEC3<6>	IPC25<20:18>	IPC25<17:16>	Yes
ADC Data 44	_ADC_DATA44_VECTOR	103	OFF103<17:1>	IFS3<7>	IEC3<7>	IPC25<28:26>	IPC25<25:24>	Yes
Core Performance Counter Interrupt	_CORE_PERF_COUNT_VECTOR	104	OFF104<17:1>	IFS3<8>	IEC3<8>	IPC26<4:2>	IPC26<1:0>	No
Core Fast Debug Channel Interrupt	_CORE_FAST_DEBUG_CHAN_VECTOR	105	OFF105<17:1>	IFS3<9>	IEC3<9>	IPC26<12:10>	IPC26<9:8>	Yes

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION (CONTINUED)

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MZ EF Family Features" for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

4: This interrupt source is not available on 124-pin devices.

9.0 PREFETCH MODULE

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 41. "Prefetch Module for Devices with L1 CPU Cache" (DS60001183) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The Prefetch module is a performance enhancing module that is included in the PIC32MZ EF family of devices. When running at high-clock rates, Wait states must be inserted into Program Flash Memory (PFM) read transactions to meet the access time of the PFM. Wait states can be hidden to the core by prefetching and storing instructions in a temporary holding area that the CPU can access quickly. Although the data path to the CPU is 32 bits wide, the data path to the PFM is 128 bits wide. This wide data path provides the same bandwidth to the CPU as a 32-bit path running at four times the frequency.

The Prefetch module holds a subset of PFM in temporary holding spaces known as lines. Each line contains a tag and data field. Normally, the lines hold a copy of what is currently in memory to make instructions or data available to the CPU without Flash Wait states.

The following are key features of the Prefetch module:

- 4x16 byte fully-associative lines
- One line for CPU instructions
- · One line for CPU data
- Two lines for peripheral data
- 16-byte parallel memory fetch
- Configurable predictive prefetch
- Error detection and correction

A simplified block diagram of the Prefetch module is shown in Figure 9-1.

FIGURE 9-1: PREFETCH MODULE BLOCK DIAGRAM



REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)

bit 18 **OVERRUN:** Data Overrun Status bit (*Device mode*)

- 1 = An OUT packet cannot be loaded into the RX FIFO.
- 0 = Written by software to clear this bit

This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.

ERROR: No Data Packet Received Status bit (Host mode)

- 1 = Three attempts have been made to receive a packet and no data packet has been received. An interrupt is generated.
- 0 = Written by the software to clear this bit.

This bit is only valid when the RX endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns zero.

- bit 17 FIFOFULL: FIFO Full Status bit
 - 1 = No more packets can be loaded into the RX FIFO
 - 0 = The RX FIFO has at least one free space
- bit 16 RXPKTRDY: Data Packet Reception Status bit
 - 1 = A data packet has been received. An interrupt is generated.
 - 0 = Written by software to clear this bit when the packet has been unloaded from the RX FIFO.
- bit 15-11 MULT<4:0>: Multiplier Control bits

For Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints, multiplies TXMAXP by MULT+1 for the payload size.

For Bulk endpoints, MULT can be up to 32 and defines the number of "USB" packets of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. The data packet is required to be an exact multiple of the payload specified by TXMAXP.

For Isochronous/Interrupts endpoints operating in Hi-Speed mode, MULT may be either 2 or 3 and specifies the maximum number of such transactions that can take place in a single microframe.

bit 10-0 RXMAXP<10:0>: Maximum RX Payload Per Transaction Control bits

This field sets the maximum payload (in bytes) transmitted in a single transaction. The value is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-Speed and Hi-Speed operations.

RXMAXP must be set to an even number of bytes for proper interrupt generation in DMA Mode 1.

REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER (CONTINUED)

bit 0 SESSION: Active Session Control/Status bit

- 'A' device:
- 1 = Start a session
- 0 = End a session

'B' device:

1 = (Read) Session has started or is in progress, (Write) Initiate the Session Request Protocol
 0 = When USB module is in Suspend mode, clearing this bit will cause a software disconnect

Clearing this bit when the USB module is not suspended will result in undefined behavior.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	_	—	—	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7.0	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	U-0	U-0	U-0	U-0	R-0, HC, HS
7:0	BAD1	BAD2	DMTEVENT	_		_		WINOPN

REGISTER 15-4: DMTSTAT: DEADMAN TIMER STATUS REGISTER

Legend:	HC = Hardware Cleared	HS = Hardware Set
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	0' = Bit is cleared $x = Bit is unknown$

bit 31-8	Unimplemented: Read as '0'
bit 7	BAD1: Bad STEP1<7:0> Value Detect bit
	1 = Incorrect STEP1<7:0> value was detected
	0 = Incorrect STEP1<7:0> value was not detected
bit 6	BAD2: Bad STEP2<7:0> Value Detect bit
	1 = Incorrect STEP2<7:0> value was detected
	0 = Incorrect STEP2<7:0> value was not detected
bit 5	DMTEVENT: Deadman Timer Event bit
	1 = Deadman timer event was detected (counter expired or bad STEP1<7:0> or STEP2<7:0> value was entered prior to counter increment)
	0 = Deadman timer even was not detected
bit 4-1	Unimplemented: Read as '0'
bit 0	WINOPN: Deadman Timer Clear Window bit
	1 = Deadman timer clear window is open
	0 = Deadman timer clear window is not open

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	—	—	—	—	—	—	_	—			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23:16	—	—	—	—	—	—	_	—			
45.0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	—	—	—	—	DEVSEL<1:0>		MODEBY	MODEBYTES<1:0>			
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0		MODECODE<7:0>									

REGISTER 20-2: SQI1XCON2: SQI XIP CONTROL REGISTER 2

Legend:

5			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 Unimplemented: Read as '0'

bit 11-10 **DEVSEL<1:0>:** Device Select bits

- 11 = Reserved
- 10 = Reserved
- 01 = Device 1 is selected
- 00 = Device 0 is selected

bit 9-8 MODEBYTES<1:0>: Mode Byte Cycle Enable bits

- 11 = Three cycles
- 10 = Two cycles
- 01 = One cycle
- 00 = Zero cycles

bit 7-0 MODECODE<7:0>: Mode Code Value bits

These bits contain the 8-bit code value for the mode bits.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC							
31.24		CVDDATA<15:8>								
22.16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC							
23:16	CVDDATA<7:0>									
15.0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC		
15.6		_	AINID<5:0>							
7.0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7:0	ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO		

REGISTER 28-20: ADCCMPCON1: ADC DIGITAL COMPARATOR 1 CONTROL REGISTER

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 CVDDATA<15:0>: CVD Data Status bits

In CVD mode, these bits obtain the CVD differential output data (subtraction of CVD positive and negative measurement), whenever a Digital Comparator interrupt is generated. The value in these bits is compliant with the FRACT bit (ADCCON1<23>) and is always signed.

bit 15-14 Unimplemented: Read as '0'

bit 13-8 AINID<5:0>: Digital Comparator 0 Analog Input Identification (ID) bits

When a digital comparator event occurs (DCMPED = 1), these bits identify the analog input being monitored by Digital Comparator 0.

Note: In normal ADC mode, only analog inputs <31:0> can be processed by the Digital Comparator 0. The Digital Comparator 0 also supports the CVD mode, in which all Class 2 and Class 3 analog inputs may be stored in the AINID<5:0> bits.

111111 = Reserved
•
- 101101 - Reserved
101100 - ANAI is being monitored
101100 - AN43 is being monitored
•
000001 = AN1 is being monitored
000000 = ANO is being monitored
ENDCMP: Digital Comparator 0 Enable bit
1 = Digital Comparator 0 is enabled
0 = Digital Comparator 0 is not enabled, and the DCMPED status bit (ADCCMP0CON<5>) is cleared
DCMPGIEN: Digital Comparator 0 Global Interrupt Enable bit
1 = A Digital Comparator 0 interrupt is generated when the DCMPED status bit (ADCCMP0CON<5>) is set $0 = A$ Digital Comparator 0 interrupt is disabled
DCMPED: Digital Comparator 0 "Output True" Event Status bit
The logical conditions under which the digital comparator gets "True" are defined by the IEBTWN IEHIHI
IEHILO, IELOHI, and IELOLO bits.
Note: This bit is cleared by reading the AINID<5:0> bits or by disabling the Digital Comparator module (by setting ENDCMP to '0').
1 = Digital Comparator 0 output true event has occurred (output of Comparator is '1')
0 = Digital Comparator 0 output is false (output of comparator is '0')
IEBTWN: Between Low/High Digital Comparator 0 Event bit
1 = Generate a digital comparator event when DCMPLO<15:0> \leq DATA<31:0> \leq DCMPHI<15:0>

REGISTER 29-1: CICON: CAN MODULE CONTROL REGISTER (CONTINUED)

- bit 13 SIDLE: CAN Stop in Idle bit 1 = CAN Stops operation when system enters Idle mode 0 = CAN continues operation when system enters Idle mode
 bit 12 Unimplemented: Read as '0'
 bit 11 CANBUSY: CAN Module is Busy bit 1 = The CAN module is active
 - 0 = The CAN module is completely disabled
- bit 10-5 Unimplemented: Read as '0'

bit 4-0 **DNCNT<4:0>:** Device Net Filter Bit Number bits

10011-11111 = Invalid Selection (compare up to 18-bits of data with EID)

- 10010 = Compare up to data byte 2 bit 6 with EID17 (CiRXFn<17>)
- •
- •
- •

00001 = Compare up to data byte 0 bit 7 with EID0 (CiRXFn<0>) 00000 = Do not compare data bytes

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
31:24	—	—	—	—	_	TXNFULLIE	TXHALFIE	TXEMPTYIE
00.40	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXNEMPTYIE
45.0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
15:8	—	—	—	—		TXNFULLIF ⁽¹⁾	TXHALFIF	TXEMPTYIF ⁽¹⁾
	U-0	U-0	U-0	U-0	R/W-0	R-0	R-0	R-0
7:0					RXOVFLIF	RXFULLIF ⁽¹⁾	RXHALFIF ⁽¹⁾	RXNEMPTYIF ⁽¹⁾

REGISTER 29-21: CiFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' ('n' = 0-31)

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented b	it, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 Unimplemented: Read as '0'

bit 26	TXNFULLIE: Transmit FIFO Not Full Interrupt Enable bit
	1 = Interrupt enabled for FIFO not full
	0 = Interrupt disabled for FIFO not full
bit 25	TXHALFIE: Transmit FIFO Half Full Interrupt Enable bit
	1 = Interrupt enabled for FIFO half full
	0 = Interrupt disabled for FIFO half full
bit 24	TXEMPTYIE: Transmit FIFO Empty Interrupt Enable bit
	1 = Interrupt enabled for FIFO empty
	0 = Interrupt disabled for FIFO empty
bit 23-20	Unimplemented: Read as '0'
bit 19	RXOVFLIE: Overflow Interrupt Enable bit
	1 = Interrupt enabled for overflow event
	0 = Interrupt disabled for overflow event
bit 18	RXFULLIE: Full Interrupt Enable bit
	1 = Interrupt enabled for FIFO full
	0 = Interrupt disabled for FIFO full
bit 17	RXHALFIE: FIFO Half Full Interrupt Enable bit
	1 = Interrupt enabled for FIFO half full
	0 = Interrupt disabled for FIFO half full
bit 16	RXNEMPTYIE: Empty Interrupt Enable bit
	1 = Interrupt enabled for FIFO not empty
	0 = Interrupt disabled for FIFO not empty
bit 15-11	Unimplemented: Read as '0'
bit 10	TXNFULLIF: Transmit FIFO Not Full Interrupt Flag bit ⁽¹⁾
	TXEN = 1: (FIFO configured as a Transmit Buffer)
	IXEN = 0: (FIFO configured as a Receive Buffer)
	Ulluseu, leaus U

Note 1: This bit is read-only and reflects the status of the FIFO.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
51.24				PMM<	31:24>				
00:40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23.10	PMM<23:16>								
15.9	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15.6	PMM<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7.0				PMM	<7:0>				

REGISTER 30-7: ETHPMM0: ETHERNET CONTROLLER PATTERN MATCH MASK 0 REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24	PMM<31:24>: Pattern Match Mask 3 bits
hit 22 16	DMM -22:16 - Dattorn Match Mack 2 hits

- bit 23-16 PMM<23:16>: Pattern Match Mask 2 bits
- bit 15-8 **PMM<15:8>:** Pattern Match Mask 1 bits
- bit 7-0 PMM<7:0>: Pattern Match Mask 0 bits
- Note 1: This register is only used for RX operations.
 2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 30-8: ETHPMM1: ETHERNET CONTROLLER PATTERN MATCH MASK 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31.24	PMM<63:56>								
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23.10	PMM<55:48>								
15.9	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15.6	PMM<47:40>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7.0				PMM<	39:32>		1 1		

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented b	it, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

24 PM	M<63:56>:	Pattern	Match	Mask	7 bits
16 PM	M<55:48>:	Pattern	Match	Mask	6 bits
3 PM	M<47:40>:	Pattern	Match	Mask	5 bits
PM	M<39:32>:	Pattern	Match	Mask	4 bits
	24 PM 16 PM 3 PM PM	 PMM<63:56>: PMM<55:48>: PMM<47:40>: PMM<39:32>: 	 PMM<63:56>: Pattern PMM<55:48>: Pattern PMM<47:40>: Pattern PMM<39:32>: Pattern 	 PMM<63:56>: Pattern Match PMM<55:48>: Pattern Match PMM<47:40>: Pattern Match PMM<39:32>: Pattern Match 	 PMM<63:56>: Pattern Match Mask PMM<55:48>: Pattern Match Mask PMM<47:40>: Pattern Match Mask PMM<39:32>: Pattern Match Mask

Note 1: This register is only used for RX operations. 2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04-04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
	MACMAXF<15:8> ⁽¹⁾							
7:0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0
				MACMAXF	<7:0> ⁽¹⁾			

REGISTER 30-28: EMAC1MAXF: ETHERNET CONTROLLER MAC MAXIMUM FRAME LENGTH REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 MACMAXF<15:0>: Maximum Frame Length bits⁽¹⁾ These bits reset to 0x05EE, which represents a maximum receive frame o

These bits reset to 0x05EE, which represents a maximum receive frame of 1518 octets. An untagged maximum size Ethernet frame is 1518 octets. A tagged frame adds four octets for a total of 1522 octets. If a shorter/longer maximum length restriction is desired, program this 16-bit field.

Note 1: If a proprietary header is allowed, this bit should be adjusted accordingly. For example, if 4-byte headers are prepended to frames, MACMAXF could be set to 1527 octets. This would allow the maximum VLAN tagged frame plus the 4-byte header.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

35.0 INSTRUCTION SET

The PIC32MZ EF family instruction set complies with the MIPS32[®] Release 5 instruction set architecture. The PIC32MZ EF device family *does not* support the following features:

- Core extend instructions
- Coprocessor 2 instructions

Note: Refer to "MIPS32[®] Architecture for Programmers Volume II: The MIPS32[®] Instruction Set" at www.imgtec.com for more information.

37.1 DC Characteristics

TABLE 37-1: OPERATING MIPS VS. VOLTAGE

	VDD Range Temp. Range		Max. Frequency		
Characteristic	(in voits) (Note 1)	(in °C)	PIC32MZ EF Devices	Comment	
DC5	2.1V-3.6V	-40°C to +85°C	200 MHz		

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is guaranteed, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 37-5 for BOR values.

TABLE 37-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typical	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD - S IOH)	PD	PINT + PI/O		w	
I/O Pin Power Dissipation: PI/O = S (({VDD – VOH} x IOH) + S (VOL x IOL))					
Maximum Allowed Power Dissipation	PDMAX	(TJ — TA)/θJ	A	W

TABLE 37-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 64-pin QFN (9x9x0.9 mm)	θJA	28	—	°C/W	1
Package Thermal Resistance, 64-pin TQFP (10x10x1 mm)	θJA	49		°C/W	1
Package Thermal Resistance, 100-pin TQFP (12x12x1 mm)	θJA	43		°C/W	1
Package Thermal Resistance, 100-pin TQFP (14x14x1 mm)	θJA	40	—	°C/W	1
Package Thermal Resistance, 124-pin VTLA (9x9x0.9 mm)	θJA	30	—	°C/W	1
Package Thermal Resistance, 144-pin TQFP (16x16x1 mm)	θJA	42		°C/W	1
Package Thermal Resistance, 144-pin LQFP (20x20x1.4 mm)	θJA	39	_	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ JA) numbers are achieved by package simulations.



FIGURE 37-22: PARALLEL MASTER PORT READ TIMING DIAGRAM

TABLE 37-43: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.1V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPBCLK2	_	_	_
PM2	TADSU	Address Out Valid to PMALL/ PMALH Invalid (address setup time)		2 TPBCLK2	—	_	
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)		1 TPBCLK2	_	_	
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	_	ns	_
PM5	Trd	PMRD Pulse Width	—	1 TPBCLK2	—	—	—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	_		ns	
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)		80		ns	

Note 1: These parameters are characterized, but not tested in manufacturing.

144-Lead Plastic Thin Quad Flat Pack (PH) - 16x16 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		17.40	
Contact Pad Spacing	C2		17.40	
Contact Pad Width (X144)	X1			0.20
Contact Pad Length (X144)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2155B

A.10 Package Differences

In general, PIC32MZ EF devices are mostly pin compatible with PIC32MX5XX/6XX/7XX devices; however, some pins are not. In particular, the VDD and Vss pins have been added and moved to different pins. In addition, I/O functions that were on fixed pins now will largely be on remappable pins.

TABLE A-11: PACKAGE DIFFERENCES

FIG52WZ EF Fealule
P Pin
On PIC32MZ EF devices, this requirement has been removed.
No VCAP pin.
I Vss Pins
There are more VDD pins on PIC32MZ EF devices, and many are located on different pins.
VDD on 64-pin packages: 8, 26, 39, 54, 60 VDD on 100-pin packages: 14, 37, 46, 62, 74, 83, 93
There are more Vss pins on PIC32MZ EF devices, and many are located on different pins.
Vss on 64-pin packages: 7, 25, 35, 40, 55, 59 Vss on 100-pin packages: 13, 36, 45, 53, 63, 75, 84, 92
/O Pins
Peripheral functions on PIC32MZ EF devices are now routed through a PPS module, which routes the signals to the desired pins. When migrating software, it is necessary to initialize the PPS I/O functions in order to get the signal to and from the correct pin.
 PPS functionality for the following peripherals: CAN UART SPI (except SCK) Input Capture Output Compare External Interrupt (except INT0) Timer Clocks (except Timer1)

APPENDIX B: MIGRATING FROM PIC32MZ EC TO PIC32MZ EF

This appendix provides an overview of considerations for migrating from PIC32MZ EC devices to the PIC32MZ EF family of devices. The code developed for PIC32MZ EC devices can be ported to PIC32MZ EF devices after making the appropriate changes outlined in the following sections. The PIC32MZ EF devices are similar to PIC32MZ EC devices, with many feature improvements and new capabilities.

B.1 Oscillator and PLL Configuration

A number of new features have been added to the oscillator and PLL to enhance their ability to work with crystals and to change frequencies.

Table B-1 summarizes the differences (indicated by **Bold** type) between the family differences for the oscillator.

PIC32MZ EC Feature	PIC32MZ EF Feature
Primary Oscillat	or Crystal Power
On PIC32MZ EC devices, the crystal HS Posc mode is only functional with crystals that have certain characteristics, such as very low ESR.	On PIC32MZ EF devices, some DEVCFG0 bits have been added to allow control over the strength of the oscillator and to add a kick start boost. POSCBOOST (DEVCFG0<21>) 1 = Boost the kick start of the oscillator 0 = Normal start of the oscillator POSCGAIN<1:0> (DEVCFG0<20:19>) 11 = 2x gain setting 10 = 1.5x gain setting 01 = 0.5x gain setting 00 = 1x gain setting Note that the default for POSCGAIN (2x gain setting) may over- drive crystals and shorten their life. It is the responsibility of the designer to ensure crystals are operated properly.
Secondary Oscilla	ator Crystal Power
On PIC32MZ EC devices, the Secondary Oscillator (Sosc) is not functional.	On PIC32MZ EF devices, the Secondary Oscillator is now functional, and provides similar strength and kick start boost features as the POSC. SOSCBOOST (DEVCFG0<18>) 1 = Boost the kick start of the oscillator 0 = Normal start of the oscillator SOSCGAIN<1:0> (DEVCFG0<17:16>) 11 = 2x gain setting 10 = 1.5x gain setting 01 = 0.5x gain setting 00 = 1x gain setting Note that the default for SOSCGAIN (2x gain setting) may over- drive crystals and shorten their life. It is the responsibility of the designer to ensure crystals are operated properly.
Clock St	atus Bits
On PIC32MZ EC devices, the SOSCRDY bit (OSCCON<22>) indicates when the Secondary Oscillator is ready. There are no indications of other oscillator status.	A new register, CLKSTAT, has been added, which includes the SOSCRDY bit (CLKSTAT<4>). In addition, new status bits are available: • LPRCRDY (CLKSTAT<5>) • POSCRDY (CLKSTAT<2>) • DIVSPLLRDY (CLKSTAT<1>) • FRCRDY (CLKSTAT<0>)
Clock S	witching
On PIC32MZ EC devices, clock switches occur as soon as the switch command is issued. Also, the only clock sources that can be divided are the output of the PLL, and the FRC.	To reduce power spikes during clock switches, PIC32MZ EF devices add a clock slewing feature, so that clock switches can be controlled in their rate and size. The SLEWCON register controls this feature. The SLEWCON register also features a SYSCLK divider, so that all of the possible clock sources may be divided further as needed.

TABLE B-1: OSCILLATOR DIFFERENCES