# Microchip Technology - PIC32MZ1024EFE144T-I/PH Datasheet

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## What is "Embedded - Microcontrollers"?

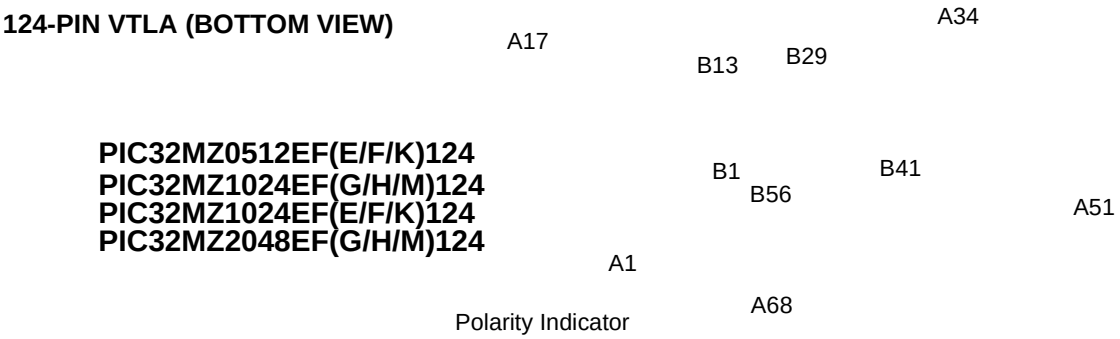
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M-Class |
| Core Size | 32-Bit Single-Core |
| Speed | 200MHz |
| Connectivity | EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 120 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.1V ~ 3.6V |
| Data Converters | A/D 48x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-TQFP |
| Supplier Device Package | 144-TQFP (16x16) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efe144t-i-ph |

**TABLE 4: PIN NAMES FOR 124-PIN DEVICES (CONTINUED)**

**124-PIN VTLA (BOTTOM VIEW)**




| Package Pin # | Full Pin Name | Package Pin # | Full Pin Name |
|---|---|---|---|
| B1 | EBIA5/AN34/PMA5/RA5 | B29 | VSS |
| B2 | EBID6/AN16/PMD6/RE6 | B30 | D+ |
| B3 | EBIA6/AN22/RPC1/PMA6/RC1 | B31 | RPF2/SDA3/RF2 |
| B4 | AN36/ETXD1/RJ9 | B32 | ERXD0/RH8 |
| B5 | $\overline{\text{EBIWE}}$/AN20/RPC3/PMWR/RC3 | B33 | ECOL/RH10 |
| B6 | AN14/C1IND/RPG6/SCK2/RG6 | B34 | EBIRDY1/SDA2/RA3 |
| B7 | EBIA3/AN12/C2IND/RPG8/SCL4/PMA3/RG8 | B35 | VDD |
| B8 | VDD | B36 | EBIA9/RPF4/SDA5/PMA9/RF4 |
| B9 | EBIA2/AN11/C2INC/RPG9/PMA2/RG9 | B37 | RPA14/SCL1/RA14 |
| B10 | AN25/RPE8/RE8 | B38 | EBIA15/RPD9/PMCS2/PMA15/RD9 |
| B11 | AN45/C1INA/RPB5/RB5 | B39 | EMDC/RPD11/RD11 |
| B12 | AN37/ERXCLK/EREFCLK/RJ11 | B40 | ERXDV/ECRSDV/RH13 |
| B13 | VSS | B41 | SOSCI/RPC13/RC13 |
| B14 | PGEC2/AN46/RPB6/RB6 | B42 | EBID14/RPD2/PMD14/RD2 |
| B15 | VREF-/CVREF-/AN27/RA9 | B43 | EBID12/RPD12/PMD12/RD12 |
| B16 | AVDD | B44 | ETXERR/RJ0 |
| B17 | AN38/ETXD2/RH0 | B45 | EBIRDY3/RJ2 |
| B18 | EBIA10/AN48/RPB8/PMA10/RB8 | B46 | $\overline{\text{SQICS1}}$/RPD5/RD5 |
| B19 | EBIA13/CVREFOUT/AN5/RPB10/PMA13/RB10 | B47 | ETXCLK/RPD7/RD7 |
| B20 | VSS | B48 | VSS |
| B21 | TCK/EBIA19/AN29/RA1 | B49 | EBID10/RPF1/PMD10/RF1 |
| B22 | TDO/EBIA17/AN31/RPF12/RF12 | B50 | EBID8/RPG0/PMD8/RG0 |
| B23 | AN8/RB13 | B51 | TRD3/SQID3/RA7 |
| B24 | EBIA0/AN10/RPB15/OCFB/PMA0/RB15 | B52 | EBID0/PMD0/RE0 |
| B25 | VDD | B53 | VDD |
| B26 | AN41/ERXD1/RH5 | B54 | TRD2/SQID2/RG14 |
| B27 | AN32/AETXD0/RPD14/RD14 | B55 | TRD0/SQID0/RG13 |
| B28 | OSC1/CLKI/RC12 | B56 | EBID3/RPE3/PMD3/RE3 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

**2:** Every I/O port pin (RAx-RJx) can be used as a change notification pin (CNAx-CNJx). See **Section 12.0 "I/O Ports"** for more information.

**3:** Shaded pins are 5V tolerant.

**4:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**TABLE 1-13: EBI PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | 124-pin VTLA | 144-pin TQFP/ LQFP | | | |
| $\overline{\text{EBIOE}}$ | — | 9 | A7 | 13 | O | — | External Bus Interface Output Enable |
| EBIRDY1 | — | 60 | B34 | 86 | I | ST | External Bus Interface Ready Input |
| EBIRDY2 | — | 58 | A39 | 84 | I | ST | |
| EBIRDY3 | — | 57 | B45 | 116 | I | ST | |
| $\overline{\text{EBIRP}}$ | — | — | — | 45 | O | — | External Bus Interface Flash Reset Pin |
| $\overline{\text{EBIWE}}$ | — | 8 | B5 | 12 | O | — | External Bus Interface Write Enable |

**Legend:** CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

**TABLE 4-11: SYSTEM BUS TARGET 3 REGISTER MAP**

| Virtual Address (BF8F_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 8C20 | SBT3ELOG1 | 31:16 | MULTI | — | — | — | CODE<3:0> | | | | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | INITID<7:0> | | | | | | | | REGION<3:0> | | | | — | CMD<2:0> | | | 0000 |
| 8C24 | SBT3ELOG2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | GROUP<1:0> | | 0000 |
| 8C28 | SBT3ECON | 31:16 | — | — | — | — | — | — | — | ERRP | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 8C30 | SBT3ECLRS | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | CLEAR | 0000 |
| 8C38 | SBT3ECLRM | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | CLEAR | 0000 |
| 8C40 | SBT3REG0 | 31:16 | BASE<21:6> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | BASE<5:0> | | | | | | PRI | — | SIZE<4:0> | | | | | — | — | — | xxxx |
| 8C50 | SBT3RD0 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | GROUP3 | GROUP2 | GROUP1 | GROUP0 | xxxx |
| 8C58 | SBT3WR0 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | GROUP3 | GROUP2 | GROUP1 | GROUP0 | xxxx |
| 8C60 | SBT3REG1 | 31:16 | BASE<21:6> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | BASE<5:0> | | | | | | PRI | — | SIZE<4:0> | | | | | — | — | — | xxxx |
| 8C70 | SBT3RD1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | GROUP3 | GROUP2 | GROUP1 | GROUP0 | xxxx |
| 8C78 | SBT3WR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | GROUP3 | GROUP2 | GROUP1 | GROUP0 | xxxx |
| 8C80 | SBT3REG2 | 31:16 | BASE<21:6> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | BASE<5:0> | | | | | | PRI | — | SIZE<4:0> | | | | | — | — | — | xxxx |
| 8C90 | SBT3RD2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | GROUP3 | GROUP2 | GROUP1 | GROUP0 | xxxx |
| 8C98 | SBT3WR2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | GROUP3 | GROUP2 | GROUP1 | GROUP0 | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
**Note:** For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

**REGISTER 4-3: SBTxELOG1: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 1 ('x' = 0-13)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0, C | U-0 | U-0 | U-0 | R/W-0, C | R/W-0, C | R/W-0, C | R/W-0, C |
| | MULTI | — | — | — | CODE<3:0> | | | |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | INITID<7:0> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | U-0 | R-0 | R-0 | R-0 |
| | REGION<3:0> | | | | — | CMD<2:0> | | |

| Legend: | C = Clearable bit | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |

bit 31 **MULTI:** Multiple Permission Violations Status bit
This bit is cleared by writing a '1'.
1 = Multiple errors have been detected
0 = No multiple errors have been detected

bit 30-28 **Unimplemented:** Read as '0'

bit 27-24 **CODE<3:0>:** Error Code bits
Indicates the type of error that was detected. These bits are cleared by writing a '1'.
1111 = Reserved
1101 = Reserved
•
•
•
0011 = Permission violation
0010 = Reserved
0001 = Reserved
0000 = No error

bit 23-16 **Unimplemented:** Read as '0'

bit 15-8 **INITID<7:0>:** Initiator ID of Requester bits
11111111 = Reserved
•
•
•
00001111 = Reserved
00001110 = Crypto Engine
00001101 = Flash Controller
00001100 = SQI1
00001011 = CAN2
00001010 = CAN1
00001001 = Ethernet Write
00001000 = Ethernet Read
00000111 = USB
00000110 = DMA Write (DMAPRI (CFGCON<25>) = 1)
00000101 = DMA Write (DMAPRI (CFGCON<25>) = 0)
00000100 = DMA Read (DMAPRI (CFGCON<25>) = 1)
00000011 = DMA Read (DMAPRI (CFGCON<25>) = 0)
00000010 = CPU (CPUPRI (CFGCON<24>) = 1)
00000001 = CPU (CPUPRI (CFGCON<25>) = 0)
00000000 = Reserved

**Note:** Refer to Table 4-6 for the list of available targets and their descriptions.

## 7.0 CPU EXCEPTIONS AND INTERRUPT CONTROLLER

**Note:** This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupt Controller"** (DS60001108) and **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MZ EF devices generate interrupt requests in response to interrupt events from peripheral modules. The Interrupt Controller module exists outside of the CPU and prioritizes the interrupt events before presenting them to the CPU.

The CPU handles interrupt events as part of the exception handling mechanism, which is described in **Section 7.1 "CPU Exceptions"**.

The Interrupt Controller module includes the following features:

- Up to 213 interrupt sources and vectors with dedicated programmable offsets, eliminating the need for redirection
- Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable subpriority levels within each priority
- Seven shadow register sets that can be used for any priority level, eliminating software context switch and reducing interrupt latency
- Software can generate any interrupt

Figure 7-1 shows the block diagram for the Interrupt Controller and CPU exceptions.

**FIGURE 7-1: CPU EXCEPTIONS AND INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM**

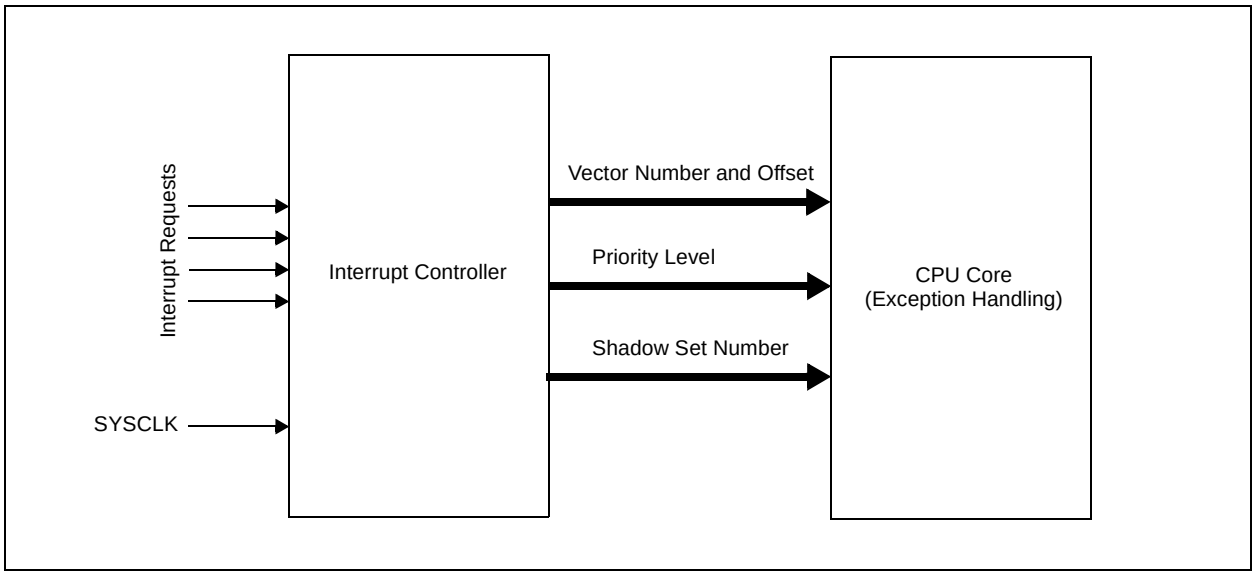


**TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)**

| Virtual Address (BF81_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 05C0 | OFF032 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 05C4 | OFF033 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 05C8 | OFF034 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 05CC | OFF035 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 05D0 | OFF036 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 05D4 | OFF037 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 05D8 | OFF038 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 05DC | OFF039 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 05E0 | OFF040 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 05E4 | OFF041 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 05E8 | OFF042 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 05EC | OFF043 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 05F0 | OFF044 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 05F4 | OFF045 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 05F8 | OFF046 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
**2:** This bit or register is not available on 64-pin devices.
**3:** This bit or register is not available on devices without a CAN module.
**4:** This bit or register is not available on 100-pin devices.
**5:** Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
**6:** Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
**7:** This bit or register is not available on devices without a Crypto module.
**8:** This bit or register is not available on 124-pin devices.

**TABLE 8-1: SYSTEM AND PERIPHERAL CLOCK DISTRIBUTION**

| Peripheral | Clock Source | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | FRC | LPRC | SOSC | SYSCLK | USBCLK | PBCLK1(1) | PBCLK2 | PBCLK3 | PBCLK4 | PBCLK5 | PBCLK7 | PBCLK8 | REFCLKO1 | REFCLKO2 | REFCLKO3 |
| CPU | | | | | | | | | | | X | | | | |
| WDT | | X | | | | X(2) | | | | | | | | | |
| Deadman Timer | | | | | | X(2) | | | | | X | | | | |
| Flash | X(2) | | | X(2) | | X(2) | | | | | | | | | |
| ADC | X | | | X | | | | X(3) | | | | | | | X |
| Comparator | | | | | | | | X | | | | | | | |
| Crypto | | | | | | | | | | X | | | | | |
| RNG | | | | | | | | | | X | | | | | |
| USB | | | | | X | | | | | X(3) | | | | | |
| CAN | | | | | | | | | | X | | | | | |
| Ethernet | | | | | | | | | | X(3) | | | | | |
| PMP | | | | | | | X | | | | | | | | |
| $I^2C$ | | | | | | | X | | | | | | | | |
| UART | | | | | | | X | | | | | | | | |
| RTCC | | X | X | | | X(2) | | | | | | | | | |
| EBI | | | | | | | | | | | | X | | | |
| SQI | | | | | | | | | | X(3) | | | | X | |
| SPI | | | | | | | X | | | | | | X | | |
| Timers | | | X(4) | | | | | X | | | | | | | |
| Output Compare | | | | | | | | X | | | | | | | |
| Input Capture | | | | | | | | X | | | | | | | |
| Ports | | | | | | | | | X | | | | | | |
| DMA | | | | X | | | | | | | | | | | |
| Interrupts | | | | X | | | | | | | | | | | |
| Prefetch | | | | X | | | | | | | | | | | |
| OSC2 Pin | | | | | | X(5) | | | | | | | | | |

**Note 1:** PBCLK1 is used by system modules and cannot be turned off.

**2:** SYSCLK/PBCLK1 is used to fetch data from/to the Flash Controller, while the FRC clock is used for programming.

**3:** Special Function Register (SFR) access only.

**4:** Timer1 only.

**5:** PBCLK1 divided by 2 is available on the OSC2 pin in certain clock modes.

## 8.1 Fail-Safe Clock Monitor (FSCM)

The PIC32MZ EF oscillator system includes a Fail-safe Clock Monitor (FSCM). The FSCM monitors the SYSCLK for continuous operation. If it detects that the SYSCLK has failed, it switches the SYSCLK over to the BFRC oscillator and triggers a NMI. The BFRC is an untuned 8 MHz oscillator that will drive the SYSCLK during FSCM event. When the NMI is executed, software can attempt to restart the main oscillator or shut down the system.

In Sleep mode both the SYSCLK and the FSCM halt, which prevents FSCM detection.

**TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP**

| Virtual Address (BF81_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1060 | DCH0CON | 31:16 | CHPIGN<7:0> | | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | CHPIGNEN | — | CHPATLEN | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 1070 | DCH0ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FF00 |
| 1080 | DCH0INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 1090 | DCH0SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 10A0 | DCH0DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 10B0 | DCH0SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 10C0 | DCH0DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 10D0 | DCH0SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 10E0 | DCH0DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 10F0 | DCH0CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 1100 | DCH0CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 1110 | DCH0DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHPDAT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 1120 | DCH1CON | 31:16 | CHPIGN<7:0> | | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | CHPIGNEN | — | CHPATLEN | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 1130 | DCH1ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FF00 |
| 1140 | DCH1INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 1150 | DCH1SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 1160 | DCH1DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

**NOTES:**

**TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)**

| Virtual Address (BF8E_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3248 | USB DMA5A | 31:16 | DMAADDR<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DMAADDR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 324C | USB DMA5N | 31:16 | DMACOUNT<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DMACOUNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3254 | USB DMA6C | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | DMABRSTM<1:0> | | DMAERR | DMAEP<3:0> | | | | DMAIE | DMAMODE | DMADIR | DMAEN | 0000 |
| 3258 | USB DMA6A | 31:16 | DMAADDR<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DMAADDR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 325C | USB DMA6N | 31:16 | DMACOUNT<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DMACOUNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3264 | USB DMA7C | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | DMABRSTM<1:0> | | DMAERR | DMAEP<3:0> | | | | DMAIE | DMAMODE | DMADIR | DMAEN | 0000 |
| 3268 | USB DMA7A | 31:16 | DMAADDR<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DMAADDR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 326C | USB DMA7N | 31:16 | DMACOUNT<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DMACOUNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3274 | USB DMA8C | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | DMABRSTM<1:0> | | DMAERR | DMAEP<3:0> | | | | DMAIE | DMAMODE | DMADIR | DMAEN | 0000 |
| 3278 | USB DMA8A | 31:16 | DMAADDR<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DMAADDR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 327C | USB DMA8N | 31:16 | DMACOUNT<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | DMACOUNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3304 | USB E1RPC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RQPKTCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3308 | USB E2RPC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RQPKTCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 330C | USB E3RPC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RQPKTCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3310 | USB E4RPC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RQPKTCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3314 | USB E5RPC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RQPKTCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3318 | USB E6RPC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RQPKTCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 331C | USB E7RPC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RQPKTCNT<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Device mode.
**2:** Host mode.
**3:** Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
**4:** Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

**REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0, HC | R-0 | R/W-0 |
| | AUTOCLR | ISO<br>AUTORQ | DMAREQEN | DISNYET<br>PIDERR | DMAREQMD | —<br>DATATWEN | —<br>DATATGGL | INCOMPRX |
| 23:16 | R/W-0, HC | R/W-0, HS | R/W-0 | R/W-0, HC | R-0, HS | R/W-0, HS | R-0, HS, HC | R/W-0, HS |
| | CLRDT | SENTSTALL<br>RXSTALL | SENDSTALL<br>REQPKT | FLUSH | DATAERR<br>DERRNAKT | OVERRUN<br>ERROR | FIFOFULL | RXPKTRDY |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | MULT<4:0> | | | | | RXMAXP<10:8> | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXMAXP<7:0> | | | | | | | |

| **Legend:** | HC = Hardware Cleared | HS = Hardware Set | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **AUTOCLR:** RXPKTRDY Automatic Clear Control bit

1 = RXPKTRDY will be automatically cleared when a packet of RXMAXP bytes has been unloaded from the RX FIFO. When packets of less than the maximum packet size are unloaded, RXPKTRDY will have to be cleared manually. When using a DMA to unload the RX FIFO, data is read from the RX FIFO in 4-byte chunks regardless of the RXMAXP.

0 = No automatic clearing of RXPKTRDY

This bit should not be set for high-bandwidth Isochronous endpoints.

bit 30 **ISO:** Isochronous Endpoint Control bit (*Device mode*)

1 = Enable the RX endpoint for Isochronous transfers

0 = Enable the RX endpoint for Bulk/Interrupt transfers

**AUTORQ:** Automatic Packet Request Control bit (*Host mode*)

1 = REQPKT will be automatically set when RXPKTRDY bit is cleared.

0 = No automatic packet request

This bit is automatically cleared when a short packet is received.

bit 29 **DMAREQEN:** DMA Request Enable Control bit

1 = Enable DMA requests for the RX endpoint.

0 = Disable DMA requests for the RX endpoint.

bit 28 **DISNYET:** Disable NYET Handshakes Control/PID Error Status bit (*Device mode*)

1 = In Bulk/Interrupt transactions, disables the sending of NYET handshakes. All successfully received RX packets are ACKed including at the point at which the FIFO becomes full.

0 = Normal operation.

In Bulk/Interrupt transactions, this bit only has any effect in Hi-Speed mode, in which mode it should be set for all Interrupt endpoints.

**PIDERR:** PID Error Status bit (*Host mode*)

1 = In ISO transactions, this indicates a PID error in the received packet.

0 = No error

bit 27 **DMAREQMD:** DMA Request Mode Selection bit

1 = DMA Request Mode 1

0 = DMA Request Mode 0

**REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)**

bit 18 **OVERRUN:** Data Overrun Status bit (*Device mode*)

1 = An OUT packet cannot be loaded into the RX FIFO.
0 = Written by software to clear this bit

This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.

**ERROR:** No Data Packet Received Status bit (*Host mode*)

1 = Three attempts have been made to receive a packet and no data packet has been received. An interrupt is generated.

0 = Written by the software to clear this bit.

This bit is only valid when the RX endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns zero.

bit 17 **FIFOFULL:** FIFO Full Status bit

1 = No more packets can be loaded into the RX FIFO
0 = The RX FIFO has at least one free space

bit 16 **RXPKTRDY:** Data Packet Reception Status bit

1 = A data packet has been received. An interrupt is generated.
0 = Written by software to clear this bit when the packet has been unloaded from the RX FIFO.

bit 15-11 **MULT<4:0>:** Multiplier Control bits

For Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints, multiplies TXMAXP by MULT+1 for the payload size.

For Bulk endpoints, MULT can be up to 32 and defines the number of “USB” packets of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. The data packet is required to be an exact multiple of the payload specified by TXMAXP.

For Isochronous/Interrupts endpoints operating in Hi-Speed mode, MULT may be either 2 or 3 and specifies the maximum number of such transactions that can take place in a single microframe.

bit 10-0 **RXMAXP<10:0>:** Maximum RX Payload Per Transaction Control bits

This field sets the maximum payload (in bytes) transmitted in a single transaction. The value is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-Speed and Hi-Speed operations.

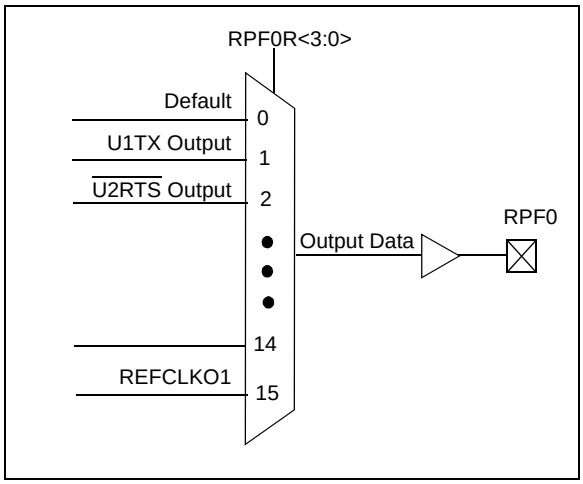
RXMAXP must be set to an even number of bytes for proper interrupt generation in DMA Mode 1.

### 12.4.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the PPS options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPnR registers (Register 12-2) are used to control output mapping. Like the [*pin name*]R registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 12-3 and Figure 12-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

**FIGURE 12-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPF0**




### 12.4.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32MZ EF devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

#### 12.4.6.1 Control Register Lock

Under normal operation, writes to the RPnR and [*pin name*]R registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK Configuration bit (CFGCON<13>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** in the *"PIC32 Family Reference Manual"* for details.

#### 12.4.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPnR and [*pin name*]R registers. The IOL1WAY Configuration bit (DEVCFG3<29>) blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.

**TABLE 29-1: CAN1 REGISTER SUMMARY FOR PIC32MZXXXXECF AND PIC32MZXXXXECH DEVICES (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 00F0 | C1FLTCON3 | 31:16 | FLTEN15 | MSEL15<1:0> | | FSEL15<4:0> | | | | | FLTEN14 | MSEL14<1:0> | | FSEL14<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN13 | MSEL13<1:0> | | FSEL13<4:0> | | | | | FLTEN12 | MSEL12<1:0> | | FSEL12<4:0> | | | | | 0000 |
| 0100 | C1FLTCON4 | 31:16 | FLTEN19 | MSEL19<1:0> | | FSEL19<4:0> | | | | | FLTEN18 | MSEL18<1:0> | | FSEL18<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN17 | MSEL17<1:0> | | FSEL17<4:0> | | | | | FLTEN16 | MSEL16<1:0> | | FSEL16<4:0> | | | | | 0000 |
| 0110 | C1FLTCON5 | 31:16 | FLTEN23 | MSEL23<1:0> | | FSEL23<4:0> | | | | | FLTEN22 | MSEL22<1:0> | | FSEL22<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN21 | MSEL21<1:0> | | FSEL21<4:0> | | | | | FLTEN20 | MSEL20<1:0> | | FSEL20<4:0> | | | | | 0000 |
| 0120 | C1FLTCON6 | 31:16 | FLTEN27 | MSEL27<1:0> | | FSEL27<4:0> | | | | | FLTEN26 | MSEL26<1:0> | | FSEL26<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN25 | MSEL25<1:0> | | FSEL25<4:0> | | | | | FLTEN24 | MSEL24<1:0> | | FSEL24<4:0> | | | | | 0000 |
| 0130 | C1FLTCON7 | 31:16 | FLTEN31 | MSEL31<1:0> | | FSEL31<4:0> | | | | | FLTEN30 | MSEL30<1:0> | | FSEL30<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN29 | MSEL29<1:0> | | FSEL29<4:0> | | | | | FLTEN28 | MSEL28<1:0> | | FSEL28<4:0> | | | | | 0000 |
| 0140-0330 | C1RXFn (n = 0-31) | 31:16 | SID<10:0> | | | | | | | | | | | -— | EXID | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| 0340 | C1FIFOBA | 31:16 | C1FIFOBA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 0350 | C1FIFOCONn (n = 0) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | FSIZE<4:0> | | | | | 0000 |
| | | 15:0 | — | FRESET | UINC | DONLY | — | — | — | — | TXEN | TXABAT | TXLARB | TXERR | TXREQ | RTREN | TXPRI<1:0> | | 0000 |
| 0360 | C1FIFOINTn (n = 0) | 31:16 | — | — | — | — | — | TXNFULLIE | TXHALFIE | TXEMPTYIE | — | — | — | — | RXOVFLIE | RXFULLIE | RXHALFIE | RXN EMPTYIE | 0000 |
| | | 15:0 | — | — | — | — | — | TXNFULLIF | TXHALFIF | TXEMPTYIF | — | — | — | — | RXOVFLIF | RXFULLIF | RXHALFIF | RXN EMPTYIF | 0000 |
| 0370 | C1FIFOUAn (n = 0) | 31:16 | C1FIFOUA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 0380 | C1FIFOCIn (n = 0) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | C1FIFOCI<4:0> | | | | | 0000 |
| 0390-0B40 | C1FIFOCONn C1FIFOINTn C1FIFOUAn C1FIFOCIn (n = 1-31) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | FSIZE<4:0> | | | | | 0000 |
| | | 15:0 | — | FRESET | UINC | DONLY | — | — | — | — | TXEN | TXABAT | TXLARB | TXERR | TXREQ | RTREN | TXPRI<1:0> | | 0000 |
| | | 31:16 | — | — | — | — | — | TXNFULLIE | TXHALFIE | TXEMPTYIE | — | — | — | — | RXOVFLIE | RXFULLIE | RXHALFIE | RXN EMPTYIE | 0000 |
| | | 15:0 | — | — | — | — | — | TXNFULLIF | TXHALFIF | TXEMPTYIF | — | — | — | — | RXOVFLIF | RXFULLIF | RXHALFIF | RXN EMPTYIF | 0000 |
| | | 31:16 | C1FIFOUA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| | | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | C1FIFOCI<4:0> | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

**REGISTER 29-11: CiFLTCON1: CAN FILTER CONTROL REGISTER 1 (CONTINUED)**

bit 15 **FLTEN5:** Filter 17 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL5<1:0>:** Filter 5 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL5<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN4:** Filter 4 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL4<1:0>:** Filter 4 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL4<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 30-38: EMAC1SA1: ETHERNET CONTROLLER MAC STATION ADDRESS 1 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P |
| | STNADDR4<7:0> | | | | | | | |
| 7:0 | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P |
| | STNADDR3<7:0> | | | | | | | |

| **Legend:** | | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STNADDR4<7:0>:** Station Address Octet 4 bits
These bits hold the fourth transmitted octet of the station address.

bit 7-0 **STNADDR3<7:0>:** Station Address Octet 3 bits
These bits hold the third transmitted octet of the station address.

**Note 1:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**2:** This register is loaded at reset from the factory preprogrammed station address.

**REGISTER 34-4: DEVCFG1/ADEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)**

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits

111 = FRC divided by FRCDIV<2:0> bits (FRCDIV)
110 = Reserved
101 = LPRC
100 = SOSC
011 = Reserved
010 = POSC (HS, EC)
001 = SPLL
000 = FRC divided by FRCDIV<2:0> bits (FRCDIV)

**TABLE 37-14: COMPARATOR SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions (see Note 3): 2.1V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Comments** |
| D300 | VIOFF | Input Offset Voltage | — | ±10 | — | mV | AVDD = VDD, AVSS = VSS |
| D301 | VICM | Input Common Mode Voltage | 0 | — | VDD | V | AVDD = VDD, AVSS = VSS **(Note 2)** |
| D302 | CMRR | Common Mode Rejection Ratio | 55 | — | — | dB | Max VICM = (VDD – 1)V **(Note 2, 4)** |
| D303 | TRESP | Response Time | — | 150 | — | ns | AVDD = VDD, AVSS = VSS **(Notes 1, 2)** |
| D304 | ON2OV | Comparator Enabled to Output Valid | — | — | 10 | µs | Comparator module is configured before setting the comparator ON bit **(Note 2)** |
| D305 | IVREF | Internal Voltage Reference | 1.194 | 1.2 | 1.206 | V | — |

**Note 1:** Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

**2:** These parameters are characterized but not tested.

**3:** The Comparator module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

**4:** CMRR measurement characterized with a 1 MΩ resistor in parallel with a 25 pF capacitor to VSS.

**TABLE 37-15: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions (see Note 3): 2.1V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Comments** |
| D312 | TSET | Internal 4-bit DAC Comparator Reference Settling time | — | — | 10 | µs | See **Note 1** |
| D313 | DACREFH | CVREF Input Voltage Reference Range | AVSS | — | AVDD | V | CVRSRC with CVRSS = 0 |
| | | | VREF- | — | VREF+ | V | CVRSRC with CVRSS = 1 |
| D314 | DVREF | CVREF Programmable Output Range | 0 | — | 0.625 x DACREFH | V | 0 to 0.625 DACREFH with DACREFH/24 step size |
| | | | 0.25 x DACREFH | — | 0.719 x DACREFH | V | 0.25 x DACREFH to 0.719 DACREFH with DACREFH/32 step size |
| D315 | DACRES | Resolution | — | — | DACREFH/24 | | CVRCON<CVRR> = 1 |
| | | | — | — | DACREFH/32 | | CVRCON<CVRR> = 0 |
| D316 | DACACC | Absolute Accuracy(2) | — | — | 1/4 | LSB | DACREFH/24, CVRCON<CVRR> = 1 |
| | | | — | — | 1/2 | LSB | DACREFH/32, CVRCON<CVRR> = 0 |

**Note 1:** Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

**2:** These parameters are characterized but not tested.

**FIGURE 37-28: EBI PAGE READ TIMING**

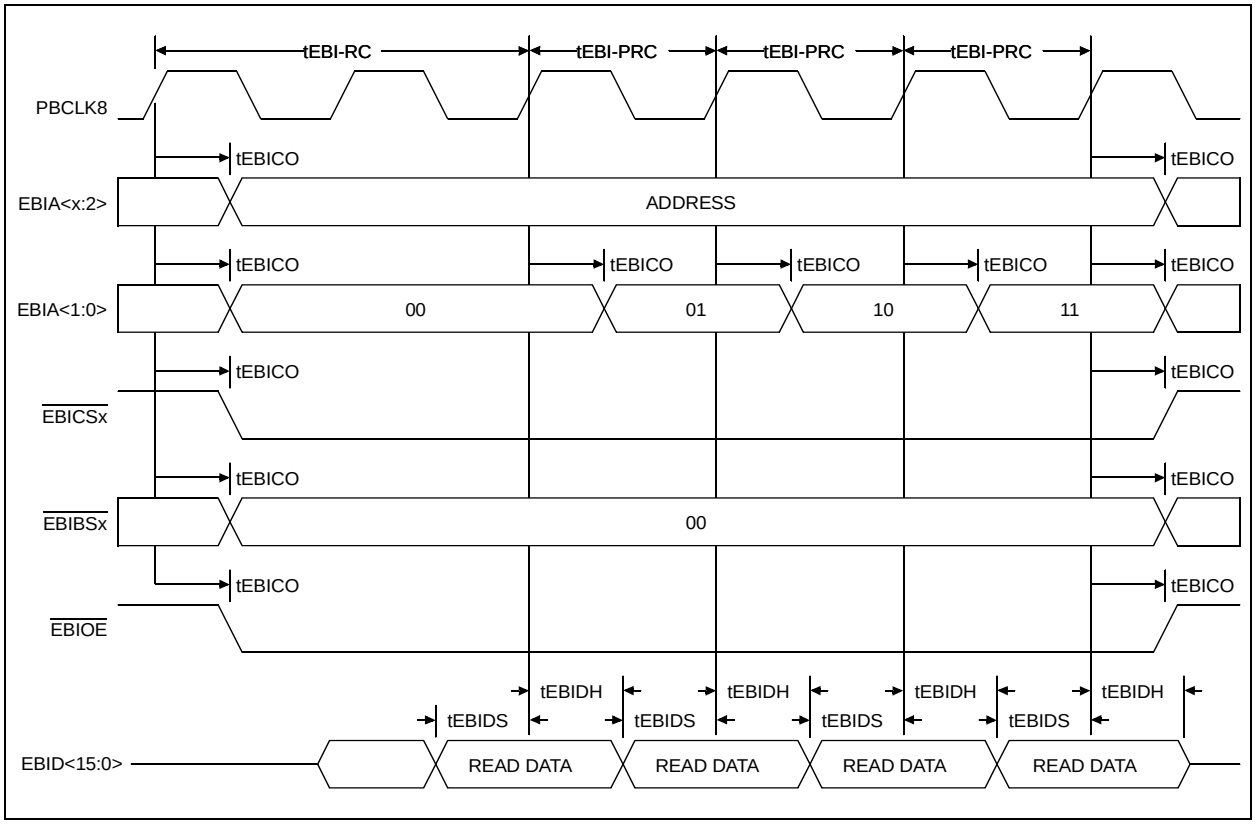



**FIGURE 37-29: EBI WRITE TIMING**

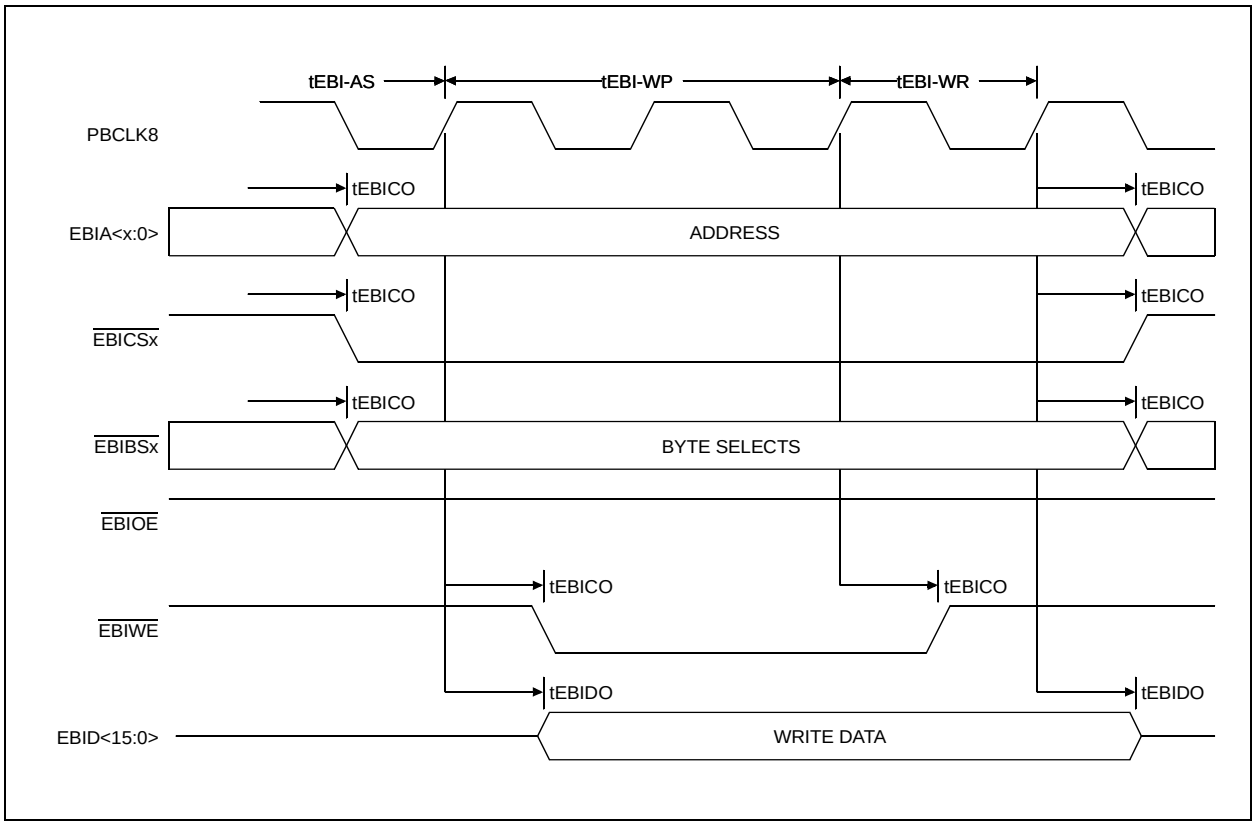


**TABLE 39-4: DC CHARACTERISTICS: PROGRAM FLASH MEMORY WAIT STATES**

| DC CHARACTERISTICS | Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | |
|---|---|---|---|
| **Required Flash Wait States(1)** | **SYSCLK** | **Units** | **Conditions** |
| **With ECC:** | | | |
| 0 Wait states | 0 < SYSCLK ≤ 60 | MHz | — |
| 1 Wait state | 60 < SYSCLK ≤ 120 | | |
| 2 Wait states | 120 < SYSCLK ≤ 200 | | |
| 4 Wait states | 200 < SYSCLK ≤ 252 | | |
| **Without ECC:** | | | |
| 0 Wait states | 0 < SYSCLK ≤ 74 | MHz | — |
| 1 Wait state | 74 < SYSCLK ≤ 140 | | |
| 2 Wait states | 140 < SYSCLK ≤ 200 | | |
| 4 Wait states | 200 < SYSCLK ≤ 252 | | |

**Note 1:** To use Wait states, the Prefetch module must be enabled (PREFEN<1:0> ≠ 00) and the PFMWS<2:0> bits must be written with the desired Wait state value.