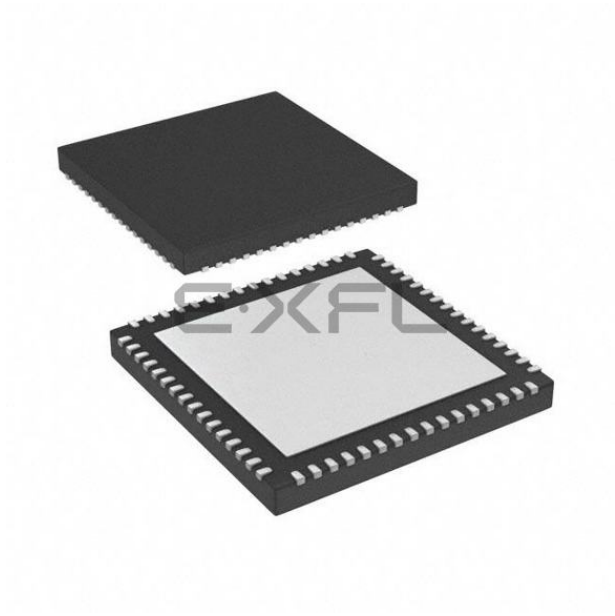


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	46
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024eff064-i-mr

TABLE 5: PIN NAMES FOR 144-PIN DEVICES

144-PIN LQFP AND TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)144
PIC32MZ1024EF(G/H/M)144
PIC32MZ1024EF(E/F/K)144
PIC32MZ2048EF(G/H/M)144

144

1

Pin Number	Full Pin Name	Pin Number	Full Pin Name
1	AN23/RG15	37	PGEC2/AN46/RPB6/RB6
2	EBIA5/AN34/PMA5/RA5	38	PGED2/AN47/RPB7/RB7
3	EBID5/AN17/RPE5/PMD5/RE5	39	VREF-/CVREF-/AN27/RA9
4	EBID6/AN16/PMD6/RE6	40	VREF+/CVREF+/AN28/RA10
5	EBID7/AN15/PMD7/RE7	41	AVDD
6	EBIA6/AN22/RPC1/PMA6/RC1	42	AVSS
7	AN35/ETXD0/RJ8	43	AN38/ETXD2/RH0
8	AN36/ETXD1/RJ9	44	AN39/ETXD3/RH1
9	EBIBS0/RJ12	45	EBIRP/RH2
10	EBIBS1/RJ10	46	RH3
11	EBIA12/AN21/RPC2/PMA12/RC2	47	EBIA10/AN48/RPB8/PMA10/RB8
12	EBIWE/AN20/RPC3/PMWR/RC3	48	EBIA7/AN49/RPB9/PMA7/RB9
13	EBIOE/AN19/RPC4/PMRD/RC4	49	CVREFOUT/AN5/RPB10/RB10
14	AN14/C1IND/RPG6/SCK2/RG6	50	AN6/RB11
15	AN13/C1INC/RPG7/SDA4/RG7	51	EBIA1/PMA1/RK1
16	AN12/C2IND/RPG8/SCL4/RG8	52	EBIA3/PMA3/RK2
17	VSS	53	EBIA17/RK3
18	VDD	54	VSS
19	EBIA16/RK0	55	VDD
20	MCLR	56	TCK/AN29/RA1
21	EBIA2/AN11/C2INC/RPG9/PMA2/RG9	57	TDI/AN30/RPF13/SCK5/RF13
22	TMS/AN24/RA0	58	TDO/AN31/RPF12/RF12
23	AN25/RPE8/RE8	59	AN7/RB12
24	AN26/RPE9/RE9	60	AN8/RB13
25	AN45/C1INA/RPB5/RB5	61	AN9/RPB14/SCK3/RB14
26	AN4/C1INB/RB4	62	AN10/RPB15/OCFB/RB15
27	AN37/ERXCLK/EREFCLK/RJ11	63	VSS
28	EBIA13/PMA13/RJ13	64	VDD
29	EBIA11/PMA11/RJ14	65	AN40/ERXERR/RH4
30	EBIA0/PMA0/RJ15	66	AN41/ERXD1/RH5
31	AN3/C2INA/RPB3/RB3	67	AN42/ERXD2/RH6
32	VSS	68	EBIA4/PMA4/RH7
33	VDD	69	AN32/RPD14/RD14
34	AN2/C2INB/RPB2/RB2	70	AN33/RPD15/SCK6/RD15
35	PGEC1/AN1/RPB1/RB1	71	OSC1/CLKI/RC12
36	PGED1/AN0/RPB0/RB0	72	OSC2/CLKO/RC15

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

TABLE 1-1: ADC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
AN0	16	25	A18	36	I	Analog	Analog Input Channels
AN1	15	24	A17	35	I	Analog	
AN2	14	23	A16	34	I	Analog	
AN3	13	22	A14	31	I	Analog	
AN4	12	21	A13	26	I	Analog	
AN5	23	34	B19	49	I	Analog	
AN6	24	35	A24	50	I	Analog	
AN7	27	41	A27	59	I	Analog	
AN8	28	42	B23	60	I	Analog	
AN9	29	43	A28	61	I	Analog	
AN10	30	44	B24	62	I	Analog	
AN11	10	16	B9	21	I	Analog	
AN12	6	12	B7	16	I	Analog	
AN13	5	11	A8	15	I	Analog	
AN14	4	10	B6	14	I	Analog	
AN15	3	5	A4	5	I	Analog	
AN16	2	4	B2	4	I	Analog	
AN17	1	3	A3	3	I	Analog	
AN18	64	100	A67	144	I	Analog	
AN19	—	9	A7	13	I	Analog	
AN20	—	8	B5	12	I	Analog	
AN21	—	7	A6	11	I	Analog	
AN22	—	6	B3	6	I	Analog	
AN23	—	1	A2	1	I	Analog	
AN24	—	17	A11	22	I	Analog	
AN25	—	18	B10	23	I	Analog	
AN26	—	19	A12	24	I	Analog	
AN27	—	28	B15	39	I	Analog	
AN28	—	29	A20	40	I	Analog	
AN29	—	38	B21	56	I	Analog	
AN30	—	39	A26	57	I	Analog	
AN31	—	40	B22	58	I	Analog	
AN32	—	47	B27	69	I	Analog	
AN33	—	48	A32	70	I	Analog	
AN34	—	2	B1	2	I	Analog	
AN35	—	—	A5	7	I	Analog	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

REGISTER 4-3: SBTxELOG1: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 1 ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0, C	U-0	U-0	U-0	R/W-0, C	R/W-0, C	R/W-0, C	R/W-0, C
	MULTI	—	—	—	CODE<3:0>			
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	INITID<7:0>							
7:0	R-0	R-0	R-0	R-0	U-0	R-0	R-0	R-0
	REGION<3:0>				—	CMD<2:0>		

Legend:	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31 **MULTI:** Multiple Permission Violations Status bit
This bit is cleared by writing a '1'.
1 = Multiple errors have been detected
0 = No multiple errors have been detected

bit 30-28 **Unimplemented:** Read as '0'

bit 27-24 **CODE<3:0>:** Error Code bits
Indicates the type of error that was detected. These bits are cleared by writing a '1'.
1111 = Reserved
1101 = Reserved
•
•
•
0011 = Permission violation
0010 = Reserved
0001 = Reserved
0000 = No error

bit 23-16 **Unimplemented:** Read as '0'

bit 15-8 **INITID<7:0>:** Initiator ID of Requester bits
11111111 = Reserved
•
•
•
00001111 = Reserved
00001110 = Crypto Engine
00001101 = Flash Controller
00001100 = SQI1
00001011 = CAN2
00001010 = CAN1
00001001 = Ethernet Write
00001000 = Ethernet Read
00000111 = USB
00000110 = DMA Write (DMAPRI (CFGCON<25>) = 1)
00000101 = DMA Write (DMAPRI (CFGCON<25>) = 0)
00000100 = DMA Read (DMAPRI (CFGCON<25>) = 1)
00000011 = DMA Read (DMAPRI (CFGCON<25>) = 0)
00000010 = CPU (CPUPRI (CFGCON<24>) = 1)
00000001 = CPU (CPUPRI (CFGCON<25>) = 0)
00000000 = Reserved

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

7.3 Interrupt Control Registers

TABLE 7-3: INTERRUPT REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	INTCON	31:16	NMIKEY<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
0010	PRISS	31:16	PRI7SS<3:0>				PRI6SS<3:0>				PRI5SS<3:0>				PRI4SS<3:0>				0000
		15:0	PRI3SS<3:0>				PRI2SS<3:0>				PRI1SS<3:0>				—	—	—	SS0	0000
0020	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			SIRQ<7:0>								0000
0030	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
0040	IFS0	31:16	OC6IF	IC6IF	IC6EIF	T6IF	OC5IF	IC5IF	IC5EIF	T5IF	INT4IF	OC4IF	IC4IF	IC4EIF	T4IF	INT3IF	OC3IF	IC3IF	0000
		15:0	IC3EIF	T3IF	INT2IF	OC2IF	IC2IF	IC2EIF	T2IF	INT1IF	OC1IF	IC1IF	IC1EIF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
0050	IFS1	31:16	ADCD4IF	ADCD3IF	ADCD2IF	ADCD1IF	ADCD0IF	ADCFLTIF	ADCDF6IF	ADCDF5IF	ADCDF4IF	ADCDF3IF	ADCDF2IF	ADCDF1IF	ADCDC6IF	ADCDC5IF	ADCDC4IF	ADCDC3IF	0000
		15:0	ADCDC2IF	ADCDC1IF	ADCFIFOIF	ADCIF	OC9IF	IC9IF	IC9EIF	T9IF	OC8IF	IC8IF	IC8EIF	T8IF	OC7IF	IC7IF	IC7EIF	T7IF	0000
0060	IFS2(5)	31:16	ADCD36IF	ADCD35IF	ADCD34IF	ADCD33IF	ADCD32IF	ADCD31IF	ADCD30IF	ADCD29IF	ADCD28IF	ADCD27IF	ADCD26IF	ADCD25IF	ADCD24IF	ADCD23IF	ADCD22IF	ADCD21IF	0000
		15:0	ADCD20IF	ADCD19IF	ADCD18IF	ADCD17IF	ADCD16IF	ADCD15IF	ADCD14IF	ADCD13IF	ADCD12IF	ADCD11IF	ADCD10IF	ADCD9IF	ADCD8IF	ADCD7IF	ADCD6IF	ADCD5IF	0000
0070	IFS3(6)	31:16	CNKIF(8)	CNJIF	CNHIF	CNGIF	CNFIF	CNEIF	CNDIF	CNCIF	CNBIF	CNAIF	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	0000
		15:0	SPI1TXIF	SPI1RXIF	SPI1EIF	—	CRPTIF(7)	SBIF	CFDCIF	CPCIF	ADCD44IF	ADCD43IF	ADCD42IF	ADCD41IF	ADCD40IF	ADCD39IF	ADCD38IF	ADCD37IF	0000
0080	IFS4	31:16	U3TXIF	U3RXIF	U3EIF	SPI3TXIF	SPI3RXIF	SPI3EIF	ETHIF	CAN2IF(3)	CAN1IF(3)	I2C2MIF(2)	I2C2SIF(2)	I2C2BIF(2)	U2TXIF	U2RXIF	U2EIF	SPI2TXIF	0000
		15:0	SPI2RXIF	SPI2EIF	DMA7IF	DMA6IF	DMA5IF	DMA4IF	DMA3IF	DMA2IF	DMA1IF	DMA0IF	USBDMAIF	USBIF	CMP2IF	CMP1IF	PMPEIF	PMPIF	0000
0090	IFS5	31:16	—	U6TXIF	U6RXIF	U6EIF	SPI6TX(2)	SPI6RXIF(2)	SPI6IF(2)	I2C5MIF	I2C5SIF	I2C5BIF	U5TXIF	U5RXIF	U5EIF	SPI5TXIF(2)	SPI5RXIF(2)	SPI5EIF(2)	0000
		15:0	I2C4MIF	I2C4SIF	I2C4BIF	U4TXIF	U4RXIF	U4EIF	SQI1IF	PREIF	FCEIF	RTCCIF	SPI4TXIF	SPI4RXIF	SPI4EIF	I2C3MIF	I2C3SIF	I2C3BIF	0000
00A0	IFS6	31:16	—	—	—	—	—	—	—	—	—	—	ADC7WIF	—	—	ADC4WIF	ADC3WIF	ADC2WIF	0000
		15:0	ADC1WIF	ADC0WIF	ADC7EIF	—	—	ADC4EIF	ADC3EIF	ADC2EIF	ADC1EIF	ADC0EIF	—	ADCGRPIF	—	ADCURDYIF	ADCARDYIF	ADCEOSIF	0000
00C0	IEC0	31:16	OC6IE	IC6IE	IC6EIE	T6IE	OC5IE	IC5IE	IC5EIE	T5IE	INT4IE	OC4IE	IC4IE	IC4EIE	T4IE	INT3IE	OC3IE	IC3IE	0000
		15:0	IC3EIE	T3IE	INT2IE	OC2IE	IC2IE	IC2EIE	T2IE	INT1IE	OC1IE	IC1IE	IC1EIE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
00D0	IEC1	31:16	ADCD4IE	ADCD3IE	ADCD2IE	ADCD1IE	ADCD0IE	ADCFLTIE	ADCDF6IE	ADCDF5IE	ADCDF4IE	ADCDF3IE	ADCDF2IE	ADCDF1IE	ADCDC6IE	ADCDC5IE	ADCDC4IE	ADCDC3IE	0000
		15:0	ADCDC2IE	ADCDC1IE	ADCFIFOIE	ADCIE	OC9IE	IC9IE	IC9EIE	T9IE	OC8IE	IC8IE	IC8EIE	T8IE	OC7IE	IC7IE	IC7EIE	T7IE	0000
00E0	IEC2(5)	31:16	ADCD36IE	ADCD35IE	ADCD34IE	ADCD33IE	ADCD32IE	ADCD31IE	ADCD30IE	ADCD29IE	ADCD28IE	ADCD27IE	ADCD26IE	ADCD25IE	ADCD24IE	ADCD23IE	ADCD22IE	ADCD21IE	0000
		15:0	ADCD20IE	ADCD19IE	ADCD18IE	ADCD17IE	ADCD16IE	ADCD15IE	ADCD14IE	ADCD13IE	ADCD12IE	ADCD11IE	ADCD10IE	ADCD9IE	ADCD8IE	ADCD7IE	ADCD6IE	ADCD5IE	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

REGISTER 11-5: USBIE0CSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 0) (CONTINUED)

bit 21 **SENDSTALL:** Send Stall Control bit (*Device mode*)
1 = Terminate the current transaction and transmit a STALL handshake. This bit is automatically cleared.
0 = Do not send STALL handshake.

REQPKT: IN transaction Request Control bit (*Host mode*)
1 = Request an IN transaction. This bit is cleared when the RXPKTRDY bit is set.
0 = Do not request an IN transaction

bit 20 **SETUPEND:** Early Control Transaction End Status bit (*Device mode*)
1 = A control transaction ended before the DATAEND bit has been set. An interrupt will be generated and the FIFO flushed at this time.
0 = Normal operation

This bit is cleared by writing a '1' to the SVCSETEND bit in this register.

ERROR: No Response Error Status bit (*Host mode*)
1 = Three attempts have been made to perform a transaction with no response from the peripheral. An interrupt is generated.
0 = Clear this flag. Software must write a '0' to this bit to clear it.

bit 19 **DATAEND:** End of Data Control bit (*Device mode*)
The software sets this bit when:

- Setting TXPKTRDY for the last data packet
- Clearing RXPKTRDY after unloading the last data packet
- Setting TXPKTRDY for a zero length data packet

Hardware clears this bit.

SETUPPKT: Send a SETUP token Control bit (*Host mode*)
1 = When set at the same time as the TXPKTRDY bit is set, the module sends a SETUP token instead of an OUT token for the transaction
0 = Normal OUT token operation

Setting this bit also clears the Data Toggle.

bit 18 **SENTSTALL:** STALL sent status bit (*Device mode*)
1 = STALL handshake has been transmitted
0 = Software clear of bit

RXSTALL: STALL handshake received Status bit (*Host mode*)
1 = STALL handshake was received
0 = Software clear of bit

bit 17 **TXPKTRDY:** TX Packet Ready Control bit
1 = Data packet has been loaded into the FIFO. It is cleared automatically.
0 = No data packet is ready for transmit

bit 16 **RXPKTRDY:** RX Packet Ready Status bit
1 = Data packet has been received. Interrupt is generated (when enabled) when this bit is set.
0 = No data packet has been received

This bit is cleared by setting the SVCRPR bit.

bit 15-0 **Unimplemented:** Read as '0'

REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER (CONTINUED)

bit 0 **SESSION:** Active Session Control/Status bit

'A' device:

1 = Start a session

0 = End a session

'B' device:

1 = (Read) Session has started or is in progress, (Write) Initiate the Session Request Protocol

0 = When USB module is in Suspend mode, clearing this bit will cause a software disconnect

Clearing this bit when the USB module is not suspended will result in undefined behavior.

TABLE 12-6: PORTC REGISTER MAP FOR 100-PIN, 124-PIN, AND 144-PIN DEVICES ONLY

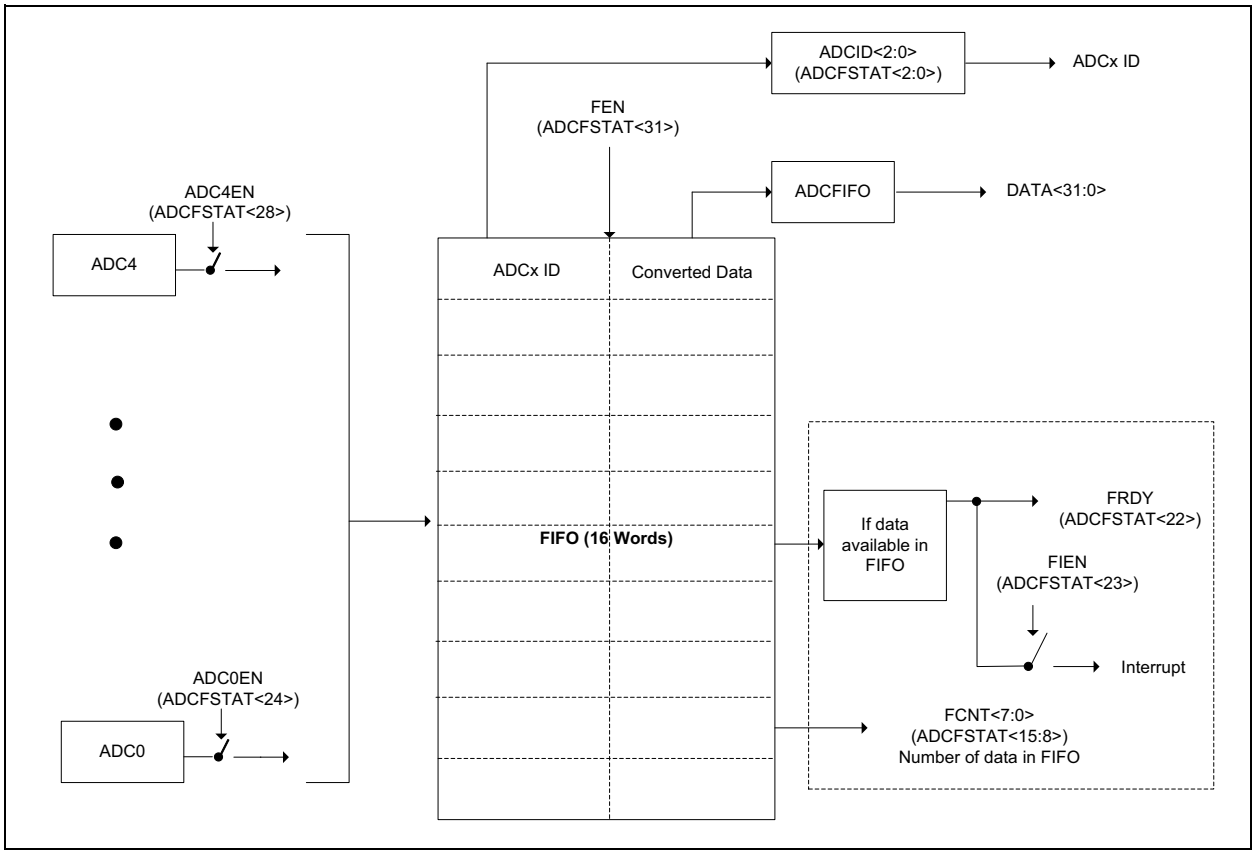
Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	ANSELC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	ANSC4	ANSC3	ANSC2	ANSC1	—	001E
0210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	TRISC4	TRISC3	TRISC2	TRISC1	—	F01E
0220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	RC4	RC3	RC2	RC1	—	xxxx
0230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	LATC4	LATC3	LATC2	LATC1	—	xxxx
0240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	ODCC4	ODCC3	ODCC2	ODCC1	—	0000
0250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUC15	CNPUC14	CNPUC13	CNPUC12	—	—	—	—	—	—	—	CNPUC4	CNPUC3	CNPUC2	CNPUC1	—	0000
0260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDC15	CNPDC14	CNPDC13	CNPDC12	—	—	—	—	—	—	—	CNPDC4	CNPDC3	CNPDC2	CNPDC1	—	0000
0270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0280	CNENC	31:16	—	—		—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNENC15	CNENC14	CNENC13	CNENC12								CNENC4	CNENC3	CNENC2	CNENC1	—	0000
0290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATC15	CNSTATC14	CNSTATC13	CNSTATC12	—	—	—	—	—	—	—	CNSTATC4	CNSTATC3	CNSTATC2	CNSTATC1	—	0000
02A0	CNNEC	31:16	—	—		—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEC15	CNNEC14	CNNEC13	CNNEC12	—	—	—	—	—	—	—	CNNEC4	CNNEC3	CNNEC2	CNNEC1	—	0000
02B0	CNFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFC15	CNFC14	CNFC13	CNFC12	—	—	—	—	—	—	—	CNFC4	CNFC3	CNFC2	CNFC1	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

NOTES:

FIGURE 28-3: FIFO BLOCK DIAGRAM



REGISTER 28-31: ADCEISTAT2: ADC EARLY INTERRUPT STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	EIRDY44(2)	EIRDY43(2)	EIRDY42(2)	EIRDY41(2)	EIRDY40(2)
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	EIRDY39(2)	EIRDY38(2)	EIRDY37(2)	EIRDY36(2)	EIRDY35(2)	EIRDY34(1)	EIRDY33(1)	EIRDY32(1)

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 31-0 **EIRDY44:EIRDY32:** Early Interrupt for Corresponding Analog Input Ready bits

1 = This bit is set when the early interrupt event occurs for the specified analog input. An interrupt will be generated if early interrupts are enabled in the ADCEIEN2 register. For the Class 1 analog inputs, this bit will set as per the configuration of the ADCEIS<2:0> bits in the ADCxTIME register. For the shared ADC module, this bit will be set as per the configuration of the ADCEIS<2:0> bits in the ADCCON2 register.

0 = Interrupts are disabled

Note 1: This bit is not available on 64-pin devices.

2: This bit is not available on 64-pin and 100-pin devices.

REGISTER 29-1: CiCON: CAN MODULE CONTROL REGISTER (CONTINUED)

bit 13 **SIDLE:** CAN Stop in Idle bit
1 = CAN Stops operation when system enters Idle mode
0 = CAN continues operation when system enters Idle mode

bit 12 **Unimplemented:** Read as '0'

bit 11 **CANBUSY:** CAN Module is Busy bit
1 = The CAN module is active
0 = The CAN module is completely disabled

bit 10-5 **Unimplemented:** Read as '0'

bit 4-0 **DNCNT<4:0>:** Device Net Filter Bit Number bits
10011-11111 = Invalid Selection (compare up to 18-bits of data with EID)
10010 = Compare up to data byte 2 bit 6 with EID17 (CiRXFn<17>)
•
•
•
00001 = Compare up to data byte 0 bit 7 with EID0 (CiRXFn<0>)
00000 = Do not compare data bytes

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

REGISTER 29-13: CiFLTCON3: CAN FILTER CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN15	MSEL15<1:0>		FSEL15<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN14	MSEL14<1:0>		FSEL14<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN13	MSEL13<1:0>		FSEL13<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN12	MSEL12<1:0>		FSEL12<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN15:** Filter 15 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL15<1:0>:** Filter 15 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL15<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN14:** Filter 14 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL14<1:0>:** Filter 14 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL14<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 29-15: CiFLTCON5: CAN FILTER CONTROL REGISTER 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN23	MSEL23<1:0>		FSEL23<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN22	MSEL22<1:0>		FSEL22<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN21	MSEL21<1:0>		FSEL21<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN20	MSEL20<1:0>		FSEL20<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN23:** Filter 23 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL23<1:0>:** Filter 23 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL23<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN22:** Filter 22 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL22<1:0>:** Filter 22 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL22<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER (CONTINUED)

bit 7 **CRCERREN:** CRC Error Collection Enable bit
1 = The received packet CRC must be invalid for the packet to be accepted
0 = Disable CRC Error Collection filtering
This bit allows the user to collect all packets that have an invalid CRC.

bit 6 **CRCOKEN:** CRC OK Enable bit
1 = The received packet CRC must be valid for the packet to be accepted
0 = Disable CRC filtering
This bit allows the user to reject all packets that have an invalid CRC.

bit 5 **RUNTERREN:** Runt Error Collection Enable bit
1 = The received packet must be a runt packet for the packet to be accepted
0 = Disable Runt Error Collection filtering

This bit allows the user to collect all packets that are runt packets. For this filter, a runt packet is defined as any packet with a size of less than 64 bytes (when CRCOKEN = 0) or any packet with a size of less than 64 bytes that has a valid CRC (when CRCOKEN = 1).

bit 4 **RUNTEN:** Runt Enable bit
1 = The received packet must not be a runt packet for the packet to be accepted
0 = Disable Runt filtering

This bit allows the user to reject all runt packets. For this filter, a runt packet is defined as any packet with a size of less than 64 bytes.

bit 3 **UCEN:** Unicast Enable bit
1 = Enable Unicast Filtering
0 = Disable Unicast Filtering

This bit allows the user to accept all unicast packets whose Destination Address matches the Station Address.

bit 2 **NOTMEEN:** Not Me Unicast Enable bit
1 = Enable Not Me Unicast Filtering
0 = Disable Not Me Unicast Filtering

This bit allows the user to accept all unicast packets whose Destination Address does not match the Station Address.

bit 1 **MCEN:** Multicast Enable bit
1 = Enable Multicast Filtering
0 = Disable Multicast Filtering

This bit allows the user to accept all Multicast Address packets.

bit 0 **BCEN:** Broadcast Enable bit
1 = Enable Broadcast Filtering
0 = Disable Broadcast Filtering

This bit allows the user to accept all Broadcast Address packets.

Note 1: XOR = True when either one or the other conditions are true, but not both.
2: This Hash Table Filter match is active regardless of the value of the HTEN bit.
3: This Magic Packet Filter match is active regardless of the value of the MPEN bit.

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

TABLE 37-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial		
Param. No.	**Typical(2)**	**Maximum(5)**	**Units**	**Conditions**	
Power-Down Current (I_{PD}) (Note 1)					
DC40k	0.7	7	mA	-40°C	Base Power-Down Current
DC40l	1.5	7	mA	+25°C	
DC40n	7	20	mA	+85°C	
Module Differential Current					
DC41e	15	50	µA	3.6V	Watchdog Timer Current: ΔI_{WDT} **(Note 3)**
DC42e	25	50	µA	3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} **(Note 3)**
DC43d	3	3.8	mA	3.6V	ADC: ΔI_{ADC} **(Notes 3, 4)**
DC44	15	50	µA	3.6V	Deadman Timer Current: ΔI_{DMT} **(Note 3)**

Note 1: The test conditions for I_{PD} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBMD = 1), V_{USB3V3} is connected to V_{SS}
- CPU is in Sleep mode
- L1 Cache and Prefetch modules are disabled
- No peripheral modules are operating, (ON bit = 0), and the associated PMD bit is set. All clocks are disabled ON bit (PBxDIV<15>) = 0 (x ≠ 1,7)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DD}
- RTCC and JTAG are disabled
- Voltage regulator is in Stand-by mode (VREGS = 0)

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Voltage regulator is operational (VREGS = 1).

5: Data in the "Maximum" column is at 3.3V, +85ºC at specified operating frequency, unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 37-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS

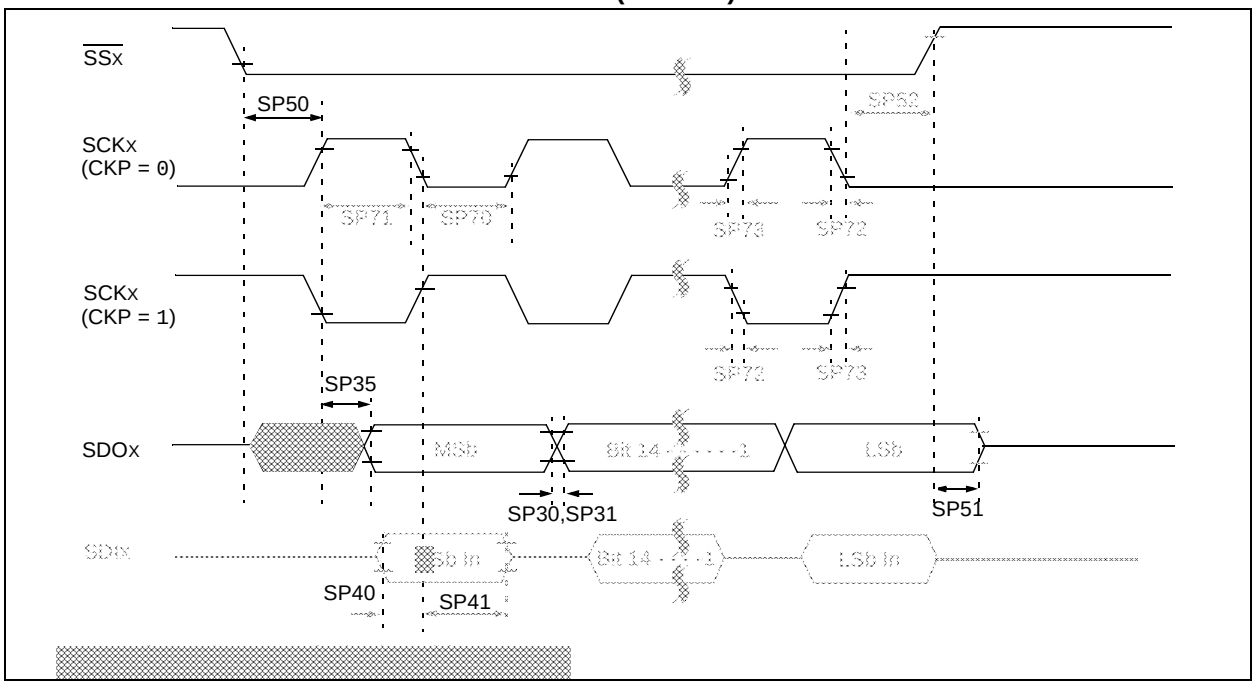


TABLE 37-32: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time **(Note 3)**	Tsck/2	—	—	ns	—
SP71	TscH	SCKx Input High Time **(Note 3)**	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See parameter DO32
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	VDD > 2.7V
			—	—	10	ns	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	88	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 3)**	2.5	—	12	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	10	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 20 ns.

4: Assumes 30 pF load on all SPIx pins.

39.0 252 MHz ELECTRICAL CHARACTERISTICS

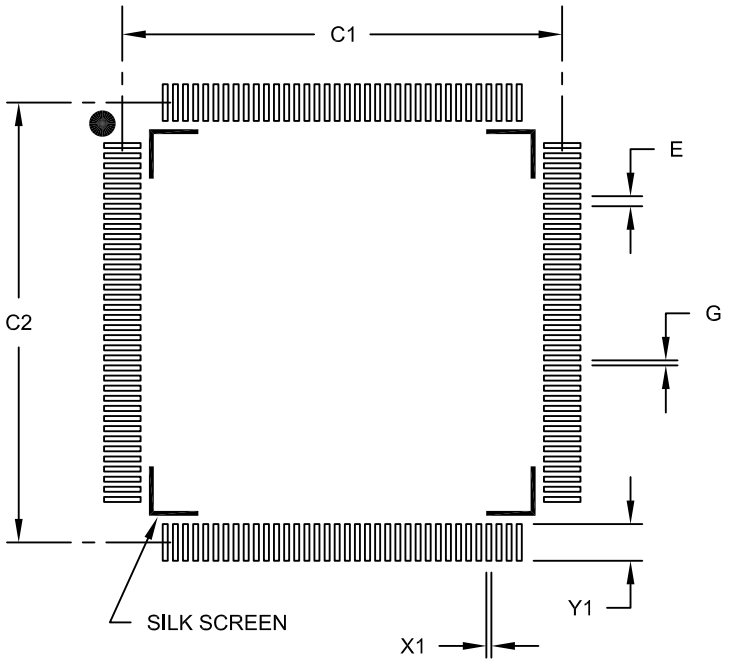
This section provides an overview of the PIC32MZ EF electrical characteristics for devices running at 252 MHz. Additional information will be provided in future revisions of this document as it becomes available.

The specifications for 252 MHz are identical to those shown in **37.0 "Electrical Characteristics"** including absolute maximum ratings, with the exception of the parameters listed in this chapter.

Parameters in this chapter begin with the letter "M", which denotes 252 MHz operation. For example, parameter DC27a in **37.0 "Electrical Characteristics"**, is the up to 200 MHz operation equivalent for MDC27a.

144-Lead Plastic Thin Quad Flat Pack (PH) - 16x16 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		17.40	
Contact Pad Spacing	C2		17.40	
Contact Pad Width (X144)	X1			0.20
Contact Pad Length (X144)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2155B

NOTES:

TABLE A-3: ADC DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Scan Trigger Source	
On PIC32MX devices, there are four sources that can trigger a scan conversion in the ADC module: Auto, Timer3, INT0, and clearing the SAMP bit. SSRC<2:0> (AD1CON1<7:5>) 111 = Auto convert 110 = Reserved 101 = Reserved 100 = Reserved 011 = Reserved 010 = Timer3 period match 001 = Active transition on INT0 pin 000 = Clearing SAMP bit	On PIC32MZ EF devices, the list of sources for triggering a scan conversion has been expanded to include the comparators, Output Compare, and two additional Timers. In addition, trigger sources can be simulated by setting the RQCNVRT (ADCCON3<8>) bit. STRGSRC<4:0> (ADCCON1<20:16>) 11111 = Reserved • • • 01101 = Reserved 01100 = Comparator 2 COUT 01011 = Comparator 1 COUT 01010 = OCMP5 01001 = OCMP3 01000 = OCMP1 00111 = TMR5 match 00110 = TMR3 match 00101 = TMR1 match 00100 = INT0 00011 = Reserved 00010 = Global level software trigger (GLSWTRG) 00001 = Global software trigger (GSWTRG) 00000 = No trigger
Output Format	
On PIC32MX devices, the output format was decided for all ADC channels based on the setting of the FORM<2:0> bits. FORM<2:0> (AD1CON1<10:8>) 011 = Signed Fractional 16-bit 010 = Fractional 16-bit 001 = Signed Integer 16-bit 000 = Integer 16-bit 111 = Signed Fractional 32-bit 110 = Fractional 32-bit 101 = Signed Integer 32-bit 100 = Integer 32-bit	On PIC32MZ EF devices, the FRACT bit determines whether fractional or integer format is used. Then, each input can have its own setting for input (differential or single-ended) and sign (signed or unsigned) using the DIFFx and SIGNx bits in the ADCIMODx registers. FRACT (ADCCON1<23>) 1 = Fractional 0 = Integer DIFFx (ADCIMODy) 1 = Channel x is using Differential mode 0 = Channel x is using Single-ended mode SIGNx (ADCMODy) 1 = Channel x is using Signed Data mode 0 = Channel x is using Unsigned Data mode
Interrupts	
On PIC32MX devices, an interrupt is triggered from the ADC module when a certain number of conversions have taken place, irrespective of which channel was converted. SMPI<3:0> (AD1CON2<5:2>) 1111 = Interrupt for each 16th sample/convert sequence 1110 = Interrupt for each 15th sample/convert sequence • • • 0001 = Interrupt for each 2nd sample/convert sequence 0000 = Interrupt for each sample/convert sequence	On PIC32MZ EF devices, the ADC module can trigger an interrupt for each channel when it is converted. Use the Interrupt Controller bits, IEC1<31:27>, IEC2<31:0>, and IEC3<7:0>, to enable/disable them. In addition, the ADC support one global interrupt to indicate conversion on any number of channels. AGIENxx (ADCGIRQENx<y>) 1 = Data ready event will generate a Global ADC interrupt 0 = No global interrupt In addition, interrupts can be generated for filter and comparator events.