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#### Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024eff100-i-pf">https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024eff100-i-pf</a>

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**TABLE 4: PIN NAMES FOR 124-PIN DEVICES (CONTINUED)**

124-PIN VTLA (BOTTOM VIEW)			
		A17	A34
		B13	B29
		B1	B41
		B56	A51
		A1	
		A68	
		Polarity Indicator	
Package Pin #	Full Pin Name	Package Pin #	Full Pin Name
B1	EBIA5/AN34/PMA5/RA5	B29	Vss
B2	EBID6/AN16/PMD6/RE6	B30	D+
B3	EBIA6/AN22/RPC1/PMA6/RC1	B31	RPF2/SDA3/RF2
B4	AN36/ETXD1/RJ9	B32	ERXD0/RH8
B5	EBIWE/AN20/RPC3/PMWR/RC3	B33	ECOL/RH10
B6	AN14/C1IND/RPG6/SCK2/RG6	B34	EBIRDY1/SDA2/RA3
B7	EBIA3/AN12/C2IND/RPG8/SCL4/PMA3/RG8	B35	VDD
B8	VDD	B36	EBIA9/RPF4/SDA5/PMA9/RF4
B9	EBIA2/AN11/C2INC/RPG9/PMA2/RG9	B37	RPA14/SCL1/RA14
B10	AN25/RPE8/RE8	B38	EBIA15/RPD9/PMCS2/PMA15/RD9
B11	AN45/C1INA/RPB5/RB5	B39	EMDC/RPD11/RD11
B12	AN37/ERXCLK/EREFCLK/RJ11	B40	ERXDV/ECRSRV/RH13
B13	Vss	B41	SOSCI/RPC13/RC13
B14	PGEC2/AN46/RPB6/RB6	B42	EBID14/RPD2/PMD14/RD2
B15	VREF-/CVREF-/AN27/RA9	B43	EBID12/RPD12/PMD12/RD12
B16	AVDD	B44	ETXERR/RJ0
B17	AN38/ETXD2/RH0	B45	EBIRDY3/RJ2
B18	EBIA10/AN48/RPB8/PMA10/RB8	B46	SQICS1/RPD5/RD5
B19	EBIA13/CVREFOUT/AN5/RPB10/PMA13/RB10	B47	ETXCLK/RPD7/RD7
B20	Vss	B48	Vss
B21	TCK/EBIA19/AN29/RA1	B49	EBID10/RPF1/PMD10/RF1
B22	TDO/EBIA17/AN31/RPF12/RF12	B50	EBID8/RPG0/PMD8/RG0
B23	AN8/RB13	B51	TRD3/SQID3/RA7
B24	EBIA0/AN10/RPB15/OCFB/PMA0/RB15	B52	EBID0/PMD0/RE0
B25	VDD	B53	VDD
B26	AN41/ERXD1/RH5	B54	TRD2/SQID2/RG14
B27	AN32/AETXD0/RPD14/RD14	B55	TRD0/SQID0/RG13
B28	OSC1/CLKI/RC12	B56	EBID3/RPE3/PMD3/RE3

- Note** 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 “Peripheral Pin Select (PPS)”** for restrictions.
- 2: Every I/O port pin (RAX-RJx) can be used as a change notification pin (CNAX-CNJx). See **Section 12.0 “I/O Ports”** for more information.
- 3: Shaded pins are 5V tolerant.
- 4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

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# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**TABLE 1-14: USB PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/LQFP			
VBUS	33	51	A35	73	I	Analog	USB bus power monitor
VUSB3V3	34	52	A36	74	P	—	USB internal transceiver supply. If the USB module is <i>not</i> used, this pin must be connected to Vss. When connected, the shared pin functions on USBID will <i>not</i> be available.
D+	37	55	B30	77	I/O	Analog	USB D+
D-	36	54	A37	76	I/O	Analog	USB D-
USBID	38	56	A38	78	I	ST	USB OTG ID detect

**Legend:** CMOS = CMOS-compatible input or output  
ST = Schmitt Trigger input with CMOS levels  
TTL = Transistor-transistor Logic input buffer

Analog = Analog input  
O = Output  
PPS = Peripheral Pin Select

P = Power  
I = Input

**TABLE 1-15: CAN1 AND CAN2 PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/LQFP			
C1TX	PPS	PPS	PPS	PPS	O	—	CAN1 Bus Transmit Pin
C1RX	PPS	PPS	PPS	PPS	I	ST	CAN1 Bus Receive Pin
C2TX	PPS	PPS	PPS	PPS	O	—	CAN2 Bus Transmit Pin
C2RX	PPS	PPS	PPS	PPS	I	ST	CAN2 Bus Receive Pin

**Legend:** CMOS = CMOS-compatible input or output  
ST = Schmitt Trigger input with CMOS levels  
TTL = Transistor-transistor Logic input buffer

Analog = Analog input  
O = Output  
PPS = Peripheral Pin Select

P = Power  
I = Input

## 3.1 Architecture Overview

The MIPS32 M-Class Microprocessor core in PIC32MZ EF family devices contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution unit
- General Purpose Register (GPR)
- Multiply/Divide Unit (MDU)
- System control coprocessor (CP0)
- Floating Point Unit (FPU)
- Memory Management Unit (MMU)
- Instruction/Data cache controllers
- Power Management
- Instructions and data caches
- microMIPS support
- Enhanced JTAG (EJTAG) controller

### 3.1.1 EXECUTION UNIT

The processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. Seven additional register file shadow sets (containing thirty-two registers) are added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Trap condition comparator
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results

- Leading Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing arithmetic and bitwise logical operations
- Shifter and store aligner
- DSP ALU and logic block for performing DSP instructions, such as arithmetic/shift/compare operations

### 3.1.2 MULTIPLY/DIVIDE UNIT (MDU)

The processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations, and DSP ASE multiply instructions. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x32 booth recoded multiplier, four pairs of result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x32) represents the *rs* operand. The second number ('32' of 32x32) represents the *rt* operand.

The MDU supports execution of one multiply or multiply-accumulate operation every clock cycle.

Divide operations are implemented with a simple 1-bit-per-clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation has completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the processor core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

**TABLE 3-1: MIPS32® M-CLASS MICROPROCESSOR CORE HIGH-PERFORMANCE INTEGER MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES**

Opcode	Operand Size (mul <i>rt</i> ) (div <i>rs</i> )	Latency	Repeat Rate
MULT/MULTU, MADD/MADDU, MSUB/MSUBU (HI/LO destination)	16 bits	5	1
	32 bits	5	1
MUL (GPR destination)	16 bits	5	1
	32 bits	5	1
DIV/DIVU	8 bits	12/14	12/14
	16 bits	20/22	20/22
	24 bits	28/30	28/30
	32 bits	36/38	36/38

## 7.0 CPU EXCEPTIONS AND INTERRUPT CONTROLLER

**Note:** This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. “Interrupt Controller”** (DS60001108) and **Section 50. “CPU for Devices with MIPS32® microAptiv™ and M-Class Cores”** (DS60001192) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com/PIC32](http://www.microchip.com/PIC32)).

PIC32MZ EF devices generate interrupt requests in response to interrupt events from peripheral modules. The Interrupt Controller module exists outside of the CPU and prioritizes the interrupt events before presenting them to the CPU.

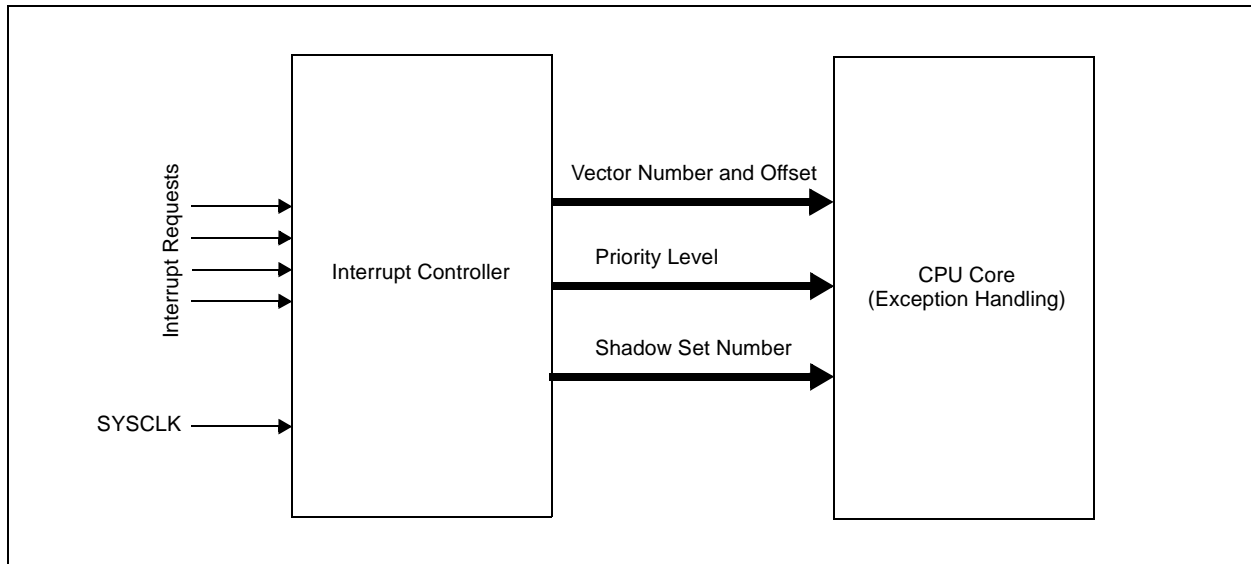
The CPU handles interrupt events as part of the exception handling mechanism, which is described in **Section 7.1 “CPU Exceptions”**.

The Interrupt Controller module includes the following features:

- Up to 213 interrupt sources and vectors with dedicated programmable offsets, eliminating the need for redirection
- Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable subpriority levels within each priority
- Seven shadow register sets that can be used for any priority level, eliminating software context switch and reducing interrupt latency
- Software can generate any interrupt

Figure 7-1 shows the block diagram for the Interrupt Controller and CPU exceptions.

**FIGURE 7-1: CPU EXCEPTIONS AND INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM**



## REGISTER 11-11: USBIENCSR3: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 3 (ENDPOINT 1-7) (CONTINUED)

bit 15-8 **RXINTERV<7:0>**: Endpoint RX Polling Interval/NAK Limit bits

For Interrupt and Isochronous transfers, this field defines the polling interval for the endpoint. For Bulk endpoints, this field sets the number of frames/microframes after which the endpoint should time out on receiving a stream of NAK responses.

The following table describes the valid values and meaning for this field:

Transfer Type	Speed	Valid Values (m)	Interpretation
Interrupt	Low/Full	0x01 to 0xFF	Polling interval is 'm' frames.
	High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames.
Isochronous	Full or High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames/microframes.
Bulk	Full or High	0x02 to 0x10	NAK limit is $2^{(m-1)}$ frames/microframes. A value of '0' or '1' disables the NAK time-out function.

bit 7-6 **SPEED<1:0>**: RX Endpoint Operating Speed Control bits

11 = Low-Speed  
10 = Full-Speed  
01 = Hi-Speed  
00 = Reserved

bit 5-4 **PROTOCOL<1:0>**: RX Endpoint Protocol Control bits

11 = Interrupt  
10 = Bulk  
01 = Isochronous  
00 = Control

bit 3-0 **TEP<3:0>**: RX Target Endpoint Number bits

This value is the endpoint number contained in the TX endpoint descriptor returned to the USB module during device enumeration.

## 12.1 Parallel I/O (PIO) Ports

All port pins have up to 14 registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

### 12.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx, and TRISx registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V) on any desired 5V-tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

Refer to the pin name tables (Table 2 through Table 5) for the available pins and their functionality.

### 12.1.2 CONFIGURING ANALOG AND DIGITAL PORT PINS

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSEL and TRIS bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

If the TRIS bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or Comparator module.

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

### 12.1.3 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be an NOP.

### 12.1.4 INPUT CHANGE NOTIFICATION

The input change notification function of the I/O ports allows the PIC32MZ EF devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-of-states even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a change-of-state.

Seven control registers are associated with the CN functionality of each I/O port. The CNENx/CNNEx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins. CNENx enables a mismatch CN interrupt condition when the EDGEDETECT bit (CNCONx<11>) is not set. When the EDGEDETECT bit is set, CNNEx controls the negative edge while CNENx controls the positive.

The CNSTATx/CNFX registers indicate the status of change notice based on the setting of the EDGEDETECT bit. If the EDGEDETECT bit is set to '0', the CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit. If the EDGEDETECT bit is set to '1', the CNFX register indicates whether a change has occurred and through the CNNEx/CNNEx registers the edge type of the change that occurred is also indicated.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

**Note:** Pull-ups and pull-downs on change notification pins should always be disabled when the port pin is configured as a digital output.

An additional control register (CNCONx) is shown in Register 12-3.



**TABLE 12-10: PORTD REGISTER MAP FOR 64-PIN DEVICES ONLY**

Virtual Address (BF86_#)	Register Name <sup>(1)</sup>	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	TRISD11	TRISD10	TRISD9	—	—	—	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	0E3F
0320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	RD11	RD10	RD9	—	—	—	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
0330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LATD11	LATD10	LATD9	—	—	—	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
0340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ODCD11	ODCD10	ODCD9	—	—	—	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
0350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNPUD11	CNPUD10	CNPUD9	—	—	—	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
0360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNPDD11	CNPDD10	CNPDD9	—	—	—	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
0370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNEND11	CNEND10	CNEND9	—	—	—	CNEND5	CNEND4	CNEND3	CNEND2	CNEND1	CNEND0	0000
0390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CN STATD11	CN STATD10	CN STATD9	—	—	—	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	CN STATD0	0000
03A0	CNNED	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNNED11	CNNED10	CNNED9	—	—	—	CNNED5	CNNED4	CNNED3	CNNED2	CNNED1	CNNED0	0000
03B0	CNFD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNFD11	CNFD10	CNFD9	—	—	—	CNFD5	CNFD4	CNFD3	CNFD2	CNFD1	CNFD0	0000

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

## 13.2 Timer1 Control Register

**TABLE 13-1: TIMER1 REGISTER MAP**

Virtual Address (BF84_#)	Register Name <sup>(1)</sup>	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	TWDIS	TWIP	—	—	—	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—	0000
0010	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR1<15:0>																0000
0020	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR1<15:0>																FFFF

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9)**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON <sup>(1)</sup>	—	SIDL <sup>(2)</sup>	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
	TGATE <sup>(1)</sup>	TCKPS<2:0> <sup>(1)</sup>			T32 <sup>(3)</sup>	—	TCS <sup>(1)</sup>	—

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit<sup>(1)</sup>

1 = Module is enabled

0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit<sup>(2)</sup>

1 = Discontinue operation when device enters Idle mode

0 = Continue operation even in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit<sup>(1)</sup>

When TCS = 1:

This bit is ignored and is read as '0'.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits<sup>(1)</sup>

111 = 1:256 prescale value

110 = 1:64 prescale value

101 = 1:32 prescale value

100 = 1:16 prescale value

011 = 1:8 prescale value

010 = 1:4 prescale value

001 = 1:2 prescale value

000 = 1:1 prescale value

bit 3 **T32:** 32-Bit Timer Mode Select bit<sup>(3)</sup>

1 = Odd numbered and even numbered timers form a 32-bit timer

0 = Odd numbered and even numbered timers form separate 16-bit timers

**Note 1:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, Timer5, Timer7, and Timer9). All timer functions are set through the even numbered timers.

**2:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

**3:** This bit is available only on even numbered timers (Timer2, Timer4, Timer6, and Timer8).

## REGISTER 20-1: SQI1XCON1: SQI XIP CONTROL REGISTER 1 (CONTINUED)

bit 5-4 **TYPEMODE<1:0>**: SQI Type Mode Enable bits

The boot controller will send the mode in Single Lane, Dual Lane, or Quad Lane.

11 = Reserved

10 = Quad Lane mode is enabled

01 = Dual Lane mode is enabled

00 = Single Lane mode is enabled

bit 3-2 **TYPEADDR<1:0>**: SQI Type Address Enable bits

The boot controller will send the address in Single Lane, Dual Lane, or Quad Lane.

11 = Reserved

10 = Quad Lane mode address is enabled

01 = Dual Lane mode address is enabled

00 = Single Lane mode address is enabled

bit 1-0 **TYPECMD<1:0>**: SQI Type Command Enable bits

The boot controller will send the command in Single Lane, Dual Lane, or Quad Lane.

11 = Reserved

10 = Quad Lane mode command is enabled

01 = Dual Lane mode command is enabled

00 = Single Lane mode command is enabled

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 21-1: I2CxCON: I<sup>2</sup>C CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
15:8	R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	SCKREL	STRICT	A10M	DISSLW	SMEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN

**Legend:**

R = Readable bit

-n = Value at POR

HC = Cleared in Hardware

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22 **PCIE:** Stop Condition Interrupt Enable bit (I<sup>2</sup>C Slave mode only)

1 = Enable interrupt on detection of Stop condition

0 = Stop detection interrupts are disabled

bit 21 **SCIE:** Start Condition Interrupt Enable bit (I<sup>2</sup>C Slave mode only)

1 = Enable interrupt on detection of Start or Restart conditions

0 = Start detection interrupts are disabled

bit 20 **BOEN:** Buffer Overwrite Enable bit (I<sup>2</sup>C Slave mode only)

1 = I2CxRCV is updated and  $\overline{ACK}$  is generated for a received address/data byte, ignoring the state of the I2COV bit (I2CxSTAT<6>) only if the RBF bit (I2CxSTAT<2>) = 0

0 = I2CxRCV is only updated when the I2COV bit (I2CxSTAT<6>) is clear

bit 19 **SDAHT:** SDA Hold Time Selection bit

1 = Minimum of 300 ns hold time on SDA after the falling edge of SCL

0 = Minimum of 100 ns hold time on SDA after the falling edge of SCL

bit 18 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I<sup>2</sup>C Slave mode only)

1 = Enable slave bus collision interrupts

0 = Slave bus collision interrupts are disabled

bit 18 **AHEN:** Address Hold Enable bit (Slave mode only)

1 = Following the 8th falling edge of SCL for a matching received address byte; SCKREL bit will be cleared and the SCL will be held low.

0 = Address holding is disabled

bit 16 **DHEN:** Data Hold Enable bit (I<sup>2</sup>C Slave mode only)

1 = Following the 8th falling edge of SCL for a received data byte; slave hardware clears the SCKREL bit and SCL is held low

0 = Data holding is disabled

bit 15 **ON:** I<sup>2</sup>C Enable bit

1 = Enables the I<sup>2</sup>C module and configures the SDA and SCL pins as serial port pins

0 = Disables the I<sup>2</sup>C module; all I<sup>2</sup>C pins are controlled by PORT functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 28-15: ADCCMPx: ADC DIGITAL COMPARATOR 'x' LIMIT VALUE REGISTER  
(‘x’ = 1 THROUGH 6)**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPHI<15:8> <sup>(1,2,3)</sup>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPHI<7:0> <sup>(1,2,3)</sup>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPLO<15:8> <sup>(1,2,3)</sup>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPLO<7:0> <sup>(1,2,3)</sup>							

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 31-16 **DCMPHI<15:0>**: Digital Comparator 'x' High Limit Value bits<sup>(1,2,3)</sup>

These bits store the high limit value, which is used by digital comparator for comparisons with ADC converted data.

bit 15-0 **DCMPLO<15:0>**: Digital Comparator 'x' Low Limit Value bits<sup>(1,2,3)</sup>

These bits store the low limit value, which is used by digital comparator for comparisons with ADC converted data.

- Note 1:** Changing these bits while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.
- 2:** The format of the limit values should match the format of the ADC converted value in terms of sign and fractional settings.
- 3:** For Digital Comparator 0 used in CVD mode, the DCM PHI<15:0> and DCMPLO<15:0> bits must always be specified in signed format, as the CVD output data is differential and is always signed.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 30-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUFCNT<7:0> <sup>(1)</sup>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ETHBUSY <sup>(5)</sup>	TxBUSY <sup>(2,6)</sup>	RxBUSY <sup>(3,6)</sup>	—	—	—	—	—

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **BUFCNT<7:0>:** Packet Buffer Count bits<sup>(1)</sup>

Number of packet buffers received in memory. Once a packet has been successfully received, this register is incremented by hardware based on the number of descriptors used by the packet. Software decrements the counter (by writing to the BUFCDEC bit (ETHCON1<0>)) for each descriptor used) after a packet has been read out of the buffer. The register does not roll over (0xFF to 0x00) when hardware tries to increment the register and the register is already at 0xFF. Conversely, the register does not roll under (0x00 to 0xFF) when software tries to decrement the register and the register is already at 0x0000. When software attempts to decrement the counter at the same time that the hardware attempts to increment the counter, the counter value will remain unchanged.

When this register value reaches 0xFF, the RX logic will halt (only if automatic Flow Control is enabled) awaiting software to write the BUFCDEC bit in order to decrement the register below 0xFF.

If automatic Flow Control is disabled, the RxDMA will continue processing and the BUFCNT will saturate at a value of 0xFF.

When this register is non-zero, the PKTPEND status bit will be set and an interrupt may be generated, depending on the value of the ETHIEN bit <PKTPENDIE> register.

When the ETHRXST register is written, the BUFCNT counter is automatically cleared to 0x00.

**Note:** BUFCNT will not be cleared when ON is set to '0'. This enables software to continue to utilize and decrement this count.

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **ETHBUSY:** Ethernet Module busy bit<sup>(5)</sup>

1 = Ethernet logic has been turned on (ON (ETHCON1<15>) = 1) or is completing a transaction

0 = Ethernet logic is idle

This bit indicates that the module has been turned on or is completing a transaction after being turned off.

**Note 1:** This bit is only used for RX operations.

**2:** This bit is only affected by TX operations.

**3:** This bit is only affected by RX operations.

**4:** This bit is affected by TX and RX operations.

**5:** This bit will be *set* when the ON bit (ETHCON1<15>) = 1.

**6:** This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 30-25: EMAC1IPGT: ETHERNET CONTROLLER MAC BACK-TO-BACK INTERPACKET GAP REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
	—	B2BIPKTGP<6:0>						

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-7 **Unimplemented:** Read as '0'

bit 6-0 **B2BIPKTGP<6:0>:** Back-to-Back Interpacket Gap bits

This is a programmable field representing the nibble time offset of the minimum possible period between the end of any transmitted packet, to the beginning of the next. In Full-Duplex mode, the register value should be the desired period in nibble times minus 3. In Half-Duplex mode, the register value should be the desired period in nibble times minus 6. In Full-Duplex the recommended setting is 0x15 (21d), which represents the minimum IPG of 0.96  $\mu$ s (in 100 Mbps) or 9.6  $\mu$ s (in 10 Mbps). In Half-Duplex mode, the recommended setting is 0x12 (18d), which also represents the minimum IPG of 0.96  $\mu$ s (in 100 Mbps) or 9.6  $\mu$ s (in 10 Mbps).

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.



### 33.3.1 CONTROLLING CONFIGURATION CHANGES

Because peripherals can be disabled during run time, some restrictions on disabling peripherals are needed to prevent accidental configuration changes. PIC32MZ EF devices include two features to prevent alterations to enabled or disabled peripherals:

- Control register lock sequence
- Configuration bit select lock

#### 33.3.1.1 Control Register Lock

Under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK Configuration bit (CFGCON<12>). Setting PMDLOCK prevents writes to the control registers; clearing PMDLOCK allows writes.

To set or clear PMDLOCK, an unlock sequence must be executed. Refer to **Section 42. “Oscillators with Enhanced PLL”** (DS60001250) in the *“PIC32 Family Reference Manual”* for details.

#### 33.3.1.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the PMDx registers. The PMDL1WAY Configuration bit (DEVCFG3<28>) blocks the PMDLOCK bit from being cleared after it has been set once. If PMDLOCK remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable PMD functionality is to perform a device Reset.

### REGISTER 34-5: DEVCFG2/ADEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 3     **Reserved:** Write as '1'

bit 2-0   **FPLLIDIV<2:0>:** PLL Input Divider bits

111 = Divide by 8

110 = Divide by 7

101 = Divide by 6

100 = Divide by 5

011 = Divide by 4

010 = Divide by 3

001 = Divide by 2

000 = Divide by 1

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 34-11: DEVID: DEVICE AND REVISION ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	VER<3:0> <sup>(1)</sup>				DEVID<27:24> <sup>(1)</sup>			
23:16	R	R	R	R	R	R	R	R
	DEVID<23:16> <sup>(1)</sup>							
15:8	R	R	R	R	R	R	R	R
	DEVID<15:8> <sup>(1)</sup>							
7:0	R	R	R	R	R	R	R	R
	DEVID<7:0> <sup>(1)</sup>							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **VER<3:0>**: Revision Identifier bits<sup>(1)</sup>

bit 27-0 **DEVID<27:0>**: Device ID<sup>(1)</sup>

**Note 1:** Refer to “*PIC32 Embedded Connectivity with Floating Point Unit (EF) Family Silicon Errata and Data Sheet Clarification*” (DS80000663) for a list of Revision and Device ID values.

## REGISTER 34-12: DEVS<sub>Nx</sub>: DEVICE SERIAL NUMBER REGISTER 'x' ('x' = 0, 1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	SN<31:24>							
23:16	R	R	R	R	R	R	R	R
	SN<23:16>							
15:8	R	R	R	R	R	R	R	R
	SN<15:8>							
7:0	R	R	R	R	R	R	R	R
	SN<7:0>							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **SN<31:0>**: Device Unique Serial Number bits

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**TABLE 37-20: INTERNAL FRC ACCURACY**

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature    -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Characteristics	Min.	Typ.	Max.	Units	Conditions
Internal FRC Accuracy @ 8.00 MHz <sup>(1)</sup>						
F20	FRC	-5	—	+5	%	0°C ≤ TA ≤ +85°C
		-8	—	+8	%	-40°C ≤ TA ≤ +85°C
		-10	—	+10	%	-40°C ≤ TA ≤ +125°C

**Note 1:** Frequency calibrated at +25°C and 3.3V. The TUN bits (OSCTUN<5:0>) can be used to compensate for temperature drift.

**TABLE 37-21: INTERNAL LPRC ACCURACY**

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature    -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Characteristics	Min.	Typ.	Max.	Units	Conditions
Internal LPRC @ 32.768 kHz <sup>(1)</sup>						
F21	LPRC	-8	—	+8	%	0°C ≤ TA ≤ +85°C
		-25	—	+25	%	-40°C ≤ TA ≤ +125°C

**Note 1:** Change of LPRC frequency as VDD changes.

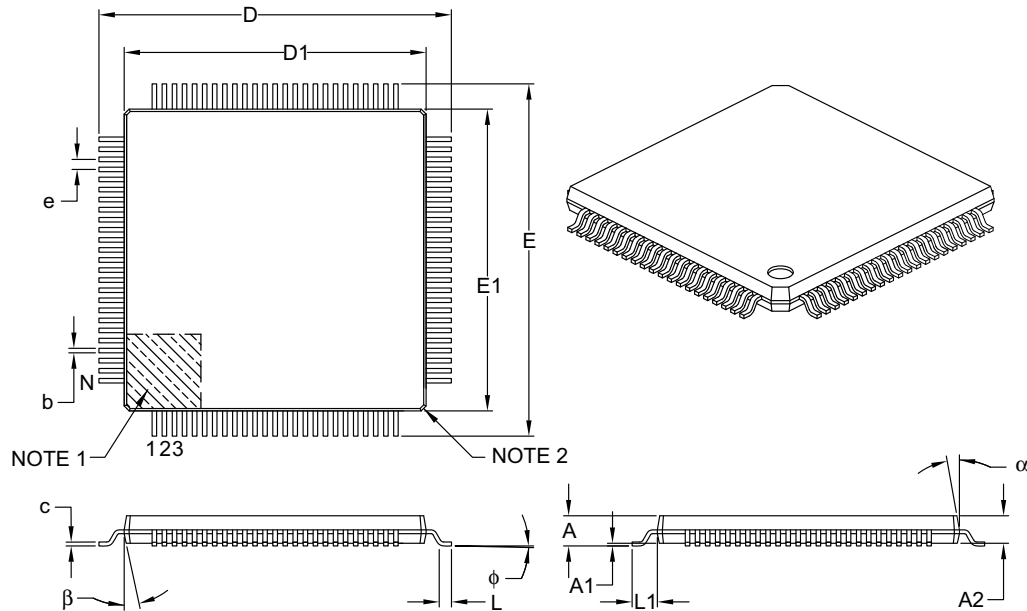
**TABLE 37-22: INTERNAL BACKUP FRC (BFRC) ACCURACY**

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature    -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Characteristics	Min.	Typ.	Max.	Units	Conditions
Internal BFRC Accuracy @ 8 MHz						
F22	BFRC	—	±30	—	%	—

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## 100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Leads	N		100		
Lead Pitch	e		0.40 BSC		
Overall Height	A		–	–	1.20
Molded Package Thickness	A2		0.95	1.00	1.05
Standoff	A1		0.05	–	0.15
Foot Length	L		0.45	0.60	0.75
Footprint	L1		1.00 REF		
Foot Angle	φ		0°	3.5°	7°
Overall Width	E		14.00 BSC		
Overall Length	D		14.00 BSC		
Molded Package Width	E1		12.00 BSC		
Molded Package Length	D1		12.00 BSC		
Lead Thickness	c		0.09	–	0.20
Lead Width	b		0.13	0.18	0.23
Mold Draft Angle Top	α		11°	12°	13°
Mold Draft Angle Bottom	β		11°	12°	13°

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B