Microchip Technology - PIC32MZ1024EFF144T-I/PL Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024eff144t-i-pl

NOTES:

1.0 DEVICE OVERVIEW

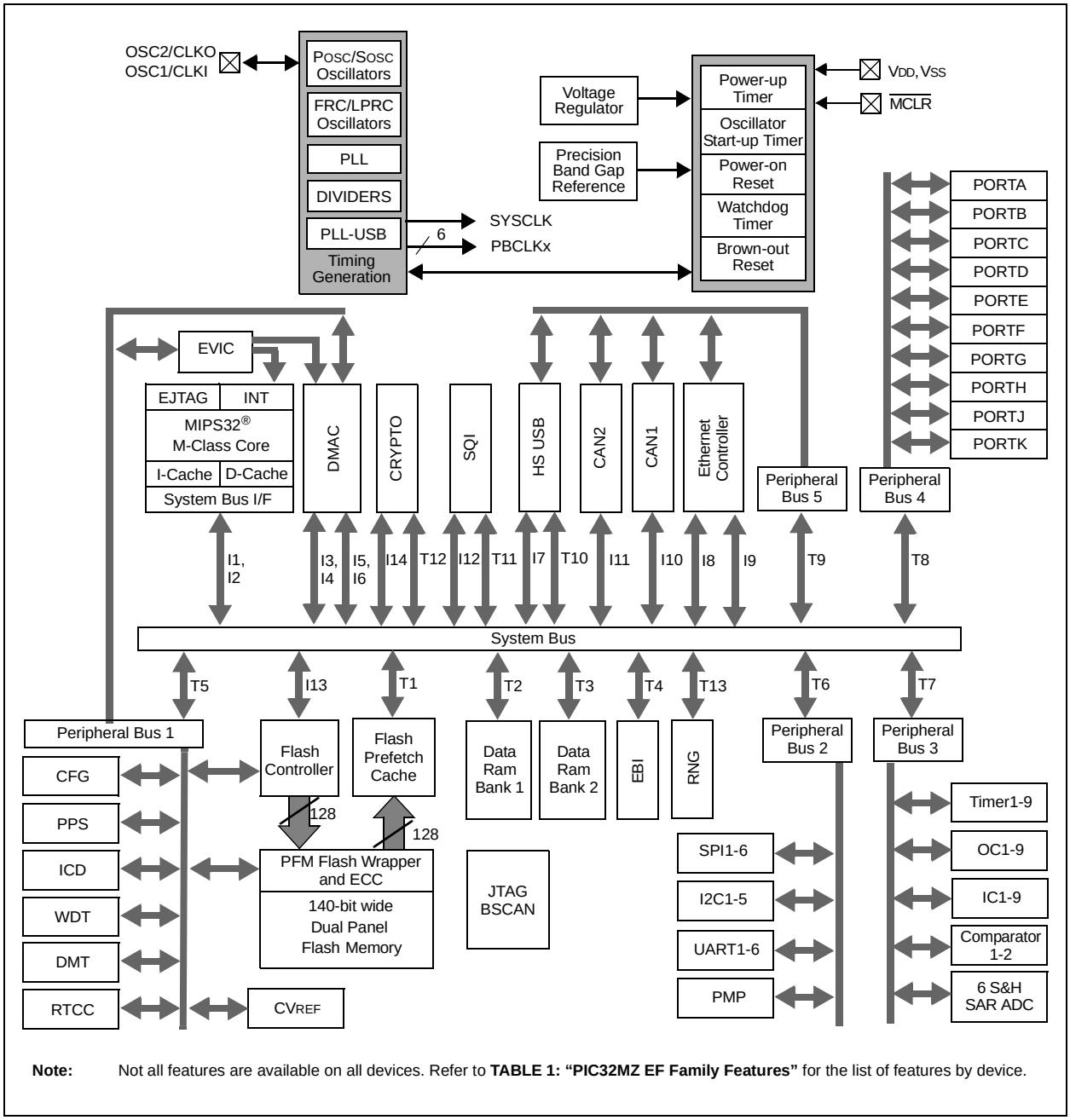
Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This data sheet contains device-specific information for PIC32MZ EF devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MZ EF family of devices.

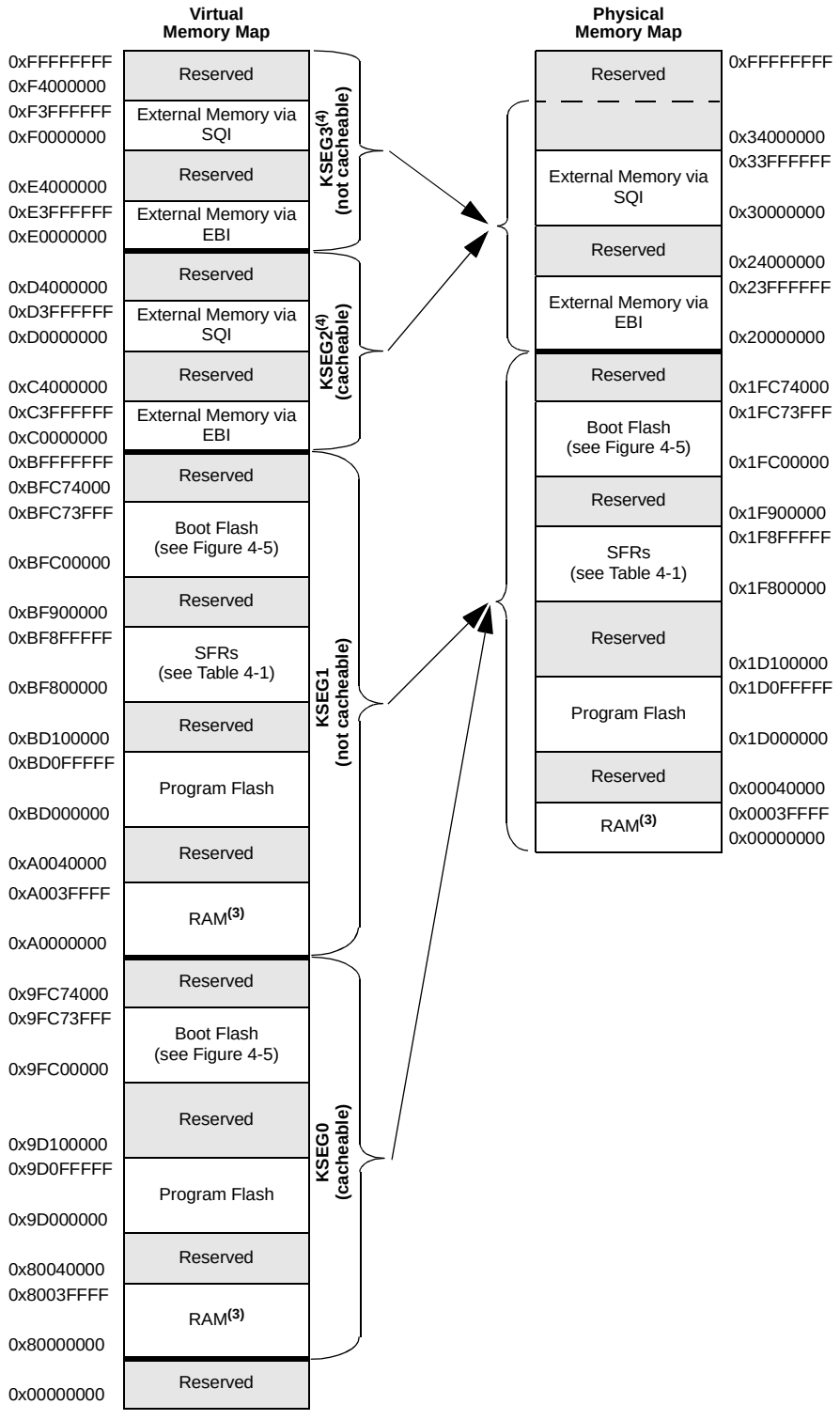
Table 1-21 through Table 1-22 list the pinout I/O descriptions for the pins shown in the device pin tables (see Table 2 through Table 5).

FIGURE 1-1: PIC32MZ EF FAMILY BLOCK DIAGRAM



Note: Not all features are available on all devices. Refer to **TABLE 1: "PIC32MZ EF Family Features"** for the list of features by device.

FIGURE 4-2: MEMORY MAP FOR DEVICES WITH 1024 KB OF PROGRAM MEMORY AND 256 KB OF RAM(1,2)



Note 1: Memory areas are not shown to scale.
2: The Cache, MMU, and TLB are initialized by compiler start-up code.
3: RAM memory is divided into two equal banks: RAM Bank 1 and RAM Bank 2 on a half boundary.
4: The MMU must be enabled and the TLB must be set up to access this segment.

TABLE 4-6: SYSTEM BUS TARGETS AND ASSOCIATED PROTECTION REGISTERS

Target Number	Target Description[5]	SBTxREGy Register							SBTxRDy Register		SBTxWRy Register	
		Name	Region Base (BASE<21:0>) (see Note 2)	Physical Start Address	Region Size (SIZE<4:0>) (see Note 3)	Region Size	Priority (PRI)	Priority Level	Name	Read Permission (GROUP3, GROUP2, GROUP1, GROUP0)	Name	Write Permission (GROUP3, GROUP2, GROUP1, GROUP0)
0	System Bus	SBT0REG0	R	0x1F8F0000	R	64 KB	—	0	SBT0RD0	R/W[1]	SBT0WR0	R/W[1]
		SBT0REG1	R	0x1F8F8000	R	32 KB	—	3	SBT0RD1	R/W[1]	SBT0WR1	R/W[1]
1	**Flash Memory[6]:** Program Flash Boot Flash Prefetch Module	SBT1REG0	R	0x1D000000	R[4]	R[4]	—	0	SBT1RD0	R/W[1]	SBT1WR0	0, 0, 0, 0
		SBT1REG2	R	0x1F8E0000	R	4 KB	1	2	SBT1RD2	R/W[1]	SBT1WR2	R/W[1]
		SBT1REG3	R/W	R/W	R/W	R/W	1	2	SBT1RD3	R/W[1]	SBT1WR3	0, 0, 0, 0
		SBT1REG4	R/W	R/W	R/W	R/W	1	2	SBT1RD4	R/W[1]	SBT1WR4	0, 0, 0, 0
		SBT1REG5	R/W	R/W	R/W	R/W	1	2	SBT1RD5	R/W[1]	SBT1WR5	0, 0, 0, 0
		SBT1REG6	R/W	R/W	R/W	R/W	1	2	SBT1RD6	R/W[1]	SBT1WR6	0, 0, 0, 0
		SBT1REG7	R/W	R/W	R/W	R/W	0	1	SBT1RD7	R/W[1]	SBT1WR7	0, 0, 0, 0
		SBT1REG8	R/W	R/W	R/W	R/W	0	1	SBT1RD8	R/W[1]	SBT1WR8	0, 0, 0, 0
2	RAM Bank 1 Memory	SBT2REG0	R	0x00000000	R[4]	R[4]	—	0	SBT2RD0	R/W[1]	SBT2WR0	R/W[1]
		SBT2REG1	R/W	R/W	R/W	R/W	—	3	SBT2RD1	R/W[1]	SBT2WR1	R/W[1]
		SBT2REG2	R/W	R/W	R/W	R/W	0	1	SBT2RD2	R/W[1]	SBT2WR2	R/W[1]
3	RAM Bank 2 Memory	SBT3REG0	R[4]	R[4]	R[4]	R[4]	—	0	SBT3RD0	R/W[1]	SBT3WR0	R/W[1]
		SBT3REG1	R/W	R/W	R/W	R/W	—	3	SBT3RD1	R/W[1]	SBT3WR1	R/W[1]
		SBT3REG2	R/W	R/W	R/W	R/W	0	1	SBT3RD2	R/W[1]	SBT3WR2	R/W[1]
4	External Memory via EBI and EBI Module[6]	SBT4REG0	R	0x20000000	R	64 MB	—	0	SBT4RD0	R/W[1]	SBT4WR0	R/W[1]
		SBT4REG2	R	0x1F8E1000	R	4 KB	0	1	SBT4RD2	R/W[1]	SBT4WR2	R/W[1]
5	**Peripheral Set 1:** System Control Flash Control DMT/WDT RTCC CVR PPS Input PPS Output Interrupts DMA	SBT5REG0	R	0x1F800000	R	128 KB	—	0	SBT5RD0	R/W[1]	SBT5WR0	R/W[1]
		SBT5REG1	R/W	R/W	R/W	R/W	—	3	SBT5RD1	R/W[1]	SBT5WR1	R/W[1]
		SBT5REG2	R/W	R/W	R/W	R/W	0	1	SBT5RD2	R/W[1]	SBT5WR2	R/W[1]

Legend: R = Read; R/W = Read/Write; 'x' in a register name = 0-13; 'y' in a register name = 0-8.

Note 1: Reset values for these bits are '0', '1', '1', '1', respectively.

2: The BASE<21:0> bits must be set to the corresponding Physical Address and right shifted by 10 bits. For Read-only bits, this value is set by hardware on Reset.

3: The SIZE<4:0> bits must be set to the corresponding Region Size, based on the following formula: Region Size = $2^{(SIZE-1)}$ x 1024 bytes. For read-only bits, this value is set by hardware on Reset.

4: Refer to the Device Memory Maps (Figure 4-1 through Figure 4-4) for specific device memory sizes and start addresses.

5: See Table 4-1for information on specific target memory size and start addresses.

6: The SBTxREG1 SFRs are reserved, and therefore, are not listed in this table for this target.

7.0 CPU EXCEPTIONS AND INTERRUPT CONTROLLER

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupt Controller"** (DS60001108) and **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MZ EF devices generate interrupt requests in response to interrupt events from peripheral modules. The Interrupt Controller module exists outside of the CPU and prioritizes the interrupt events before presenting them to the CPU.

The CPU handles interrupt events as part of the exception handling mechanism, which is described in **Section 7.1 "CPU Exceptions"**.

The Interrupt Controller module includes the following features:

- Up to 213 interrupt sources and vectors with dedicated programmable offsets, eliminating the need for redirection
- Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable subpriority levels within each priority
- Seven shadow register sets that can be used for any priority level, eliminating software context switch and reducing interrupt latency
- Software can generate any interrupt

Figure 7-1 shows the block diagram for the Interrupt Controller and CPU exceptions.

FIGURE 7-1: CPU EXCEPTIONS AND INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM

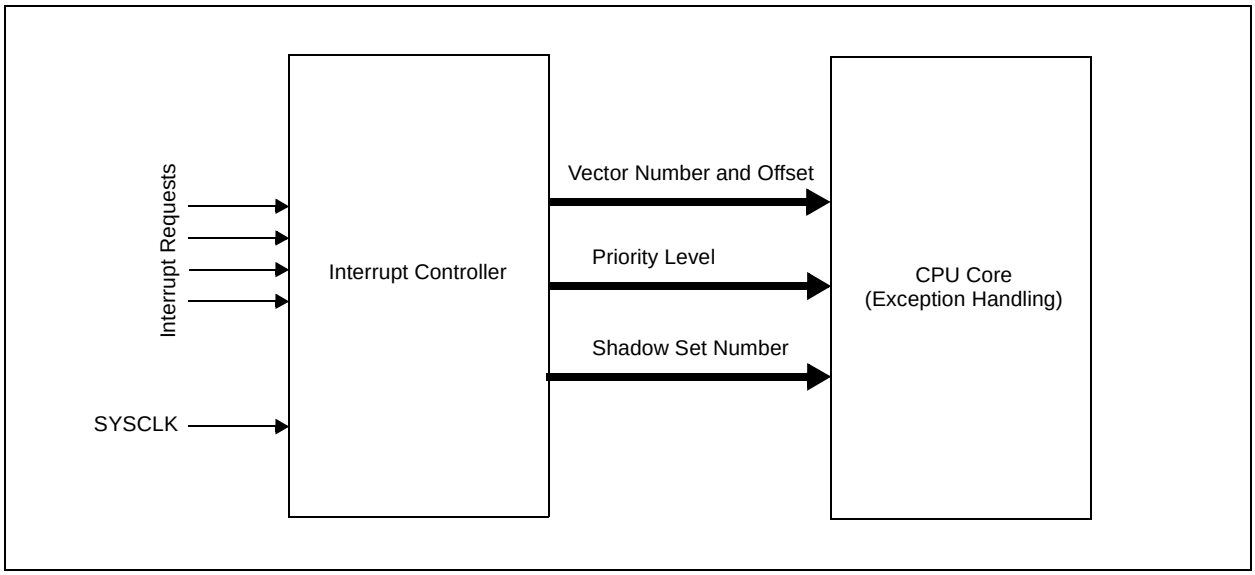


TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
02E0	IPC26	31:16	—	—	—	CRPTIP<2:0>(7)			CRPTIS<1:0>(7)		—	—	—	SBIP<2:0>			SBIS<1:0>		0000
		15:0	—	—	—	CFDCIP<2:0>			CFDCIS<1:0>		—	—	—	CPCIP<2:0>			CPCIS<1:0>		0000
02F0	IPC27	31:16	—	—	—	SPI1TXIP<2:0>			SPI1TXIS<1:0>		—	—	—	SPI1RXIP<2:0>			SPI1RXIS<1:0>		0000
		15:0	—	—	—	SPI1EIP<2:0>			SPI1EIS<1:0>		—	—	—	—	—	—	—	—	0000
0300	IPC28	31:16	—	—	—	I2C1BIP<2:0>			I2C1BIS<1:0>		—	—	—	U1TXIP<2:0>			U1TXIS<1:0>		0000
		15:0	—	—	—	U1RXIP<2:0>			U1RXIS<1:0>		—	—	—	U1EIP<2:0>			U1EIS<1:0>		0000
0310	IPC29	31:16	—	—	—	CNBIP<2:0>			CNBIS<1:0>		—	—	—	CNAIP<2:0>(2)			CNAIS<1:0>(2)		0000
		15:0	—	—	—	I2C1MIP<2:0>			I2C1MIS<1:0>		—	—	—	I2C1SIP<2:0>			I2C1SIS<1:0>		0000
0320	IPC30	31:16	—	—	—	CNFIP<2:0>			CNFIS<1:0>		—	—	—	CNEIP<2:0>			CNEIS<1:0>		0000
		15:0	—	—	—	CNDIP<2:0>			CNDIS<1:0>		—	—	—	CNCIP<2:0>			CNCIS<1:0>		0000
0330	IPC31	31:16	—	—	—	CNKIP<2:0>(2,4,8)			CNKIS<1:0>(2,4,8)		—	—	—	CNJIP<2:0>(2,4)			CNJIS<1:0>(2,4)		0000
		15:0	—	—	—	CNHIP<2:0>(2,4)			CNHIS<1:0>(2,4)		—	—	—	CNGIP<2:0>			CNGIS<1:0>		0000
0340	IPC32	31:16	—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		0000
		15:0	—	—	—	PMPEIP<2:0>			PMPEIS<1:0>		—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000
0350	IPC33	31:16	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
		15:0	—	—	—	USBDMAIP<2:0>			USBDMAIS<1:0>		—	—	—	USBIP<2:0>			USBIS<1:0>		0000
0360	IPC34	31:16	—	—	—	DMA5IP<2:0>			DMA5IS<1:0>		—	—	—	DMA4IP<2:0>			DMA4IS<1:0>		0000
		15:0	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
0370	IPC35	31:16	—	—	—	SPI2RXIP<2:0>			SPI2RXIS<1:0>		—	—	—	SPI2EIP<2:0>			SPI2EIS<1:0>		0000
		15:0	—	—	—	DMA7IP<2:0>			DMA7IS<1:0>		—	—	—	DMA6IP<2:0>			DMA6IS<1:0>		0000
0380	IPC36	31:16	—	—	—	U2TXIP<2:0>			U2TXIS<1:0>		—	—	—	U2RXIP<2:0>			U2RXIS<1:0>		0000
		15:0	—	—	—	U2EIP<2:0>			U2EIS<1:0>		—	—	—	SPI2TXIP<2:0>			SPI2TXIS<1:0>		0000
0390	IPC37	31:16	—	—	—	CAN1IP<2:0>(3)			CAN1IS<1:0>(3)		—	—	—	I2C2MIP<2:0>(2)			I2C2MIS<1:0>(2)		0000
		15:0	—	—	—	I2C2SIP<2:0>(2)			I2C2SIS<1:0>(2)		—	—	—	I2C2BIP<2:0>(2)			I2C2BIS<1:0>(2)		0000
03A0	IPC38	31:16	—	—	—	SPI3RXIP<2:0>			SPI3RXIS<1:0>		—	—	—	SPI3EIP<2:0>			SPI3EIS<1:0>		0000
		15:0	—	—	—	ETHIP<2:0>			ETHIS<1:0>		—	—	—	CAN2IP<2:0>(3)			CAN2IS<1:0>(3)		0000
03B0	IPC39	31:16	—	—	—	U3TXIP<2:0>			U3TXIS<1:0>		—	—	—	U3RXIP<2:0>			U3RXIS<1:0>		0000
		15:0	—	—	—	U3EIP<2:0>			U3EIS<1:0>		—	—	—	SPI3TXIP<2:0>			SPI3TXIS<1:0>		0000
03C0	IPC40	31:16	—	—	—	SPI4EIP<2:0>			SPI4EIS<1:0>		—	—	—	I2C3MIP<2:0>			I2C3MIS<1:0>		0000
		15:0	—	—	—	I2C3SIP<2:0>			I2C3SIS<1:0>		—	—	—	I2C3BIP<2:0>			I2C3BIS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER (CONTINUED)

bit 15-12 **PRI3SS<3:0>:** Interrupt with Priority Level 3 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 3 uses Shadow Set 0)
0111 = Interrupt with a priority level of 3 uses Shadow Set 7
0110 = Interrupt with a priority level of 3 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 3 uses Shadow Set 1
0000 = Interrupt with a priority level of 3 uses Shadow Set 0

bit 11-8 **PRI2SS<3:0>:** Interrupt with Priority Level 2 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 2 uses Shadow Set 0)
0111 = Interrupt with a priority level of 2 uses Shadow Set 7
0110 = Interrupt with a priority level of 2 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 2 uses Shadow Set 1
0000 = Interrupt with a priority level of 2 uses Shadow Set 0

bit 7-4 **PRI1SS<3:0>:** Interrupt with Priority Level 1 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 1 uses Shadow Set 0)
0111 = Interrupt with a priority level of 1 uses Shadow Set 7
0110 = Interrupt with a priority level of 1 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 1 uses Shadow Set 1
0000 = Interrupt with a priority level of 1 uses Shadow Set 0

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **SS0:** Single Vector Shadow Register Set bit
1 = Single vector is presented with a shadow set
0 = Single vector is not presented with a shadow set

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

REGISTER 8-4: REFOxCON: REFERENCE OSCILLATOR CONTROL REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RODIV<14:8>						
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RODIV<7:0>							
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC
	ON(1)	—	SIDL	OE	RSLP(2)	—	DIVSWEN	ACTIVE(1)
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	ROSEL<3:0>(3)			

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-16 **RODIV<14:0>** Reference Clock Divider bits
The value selects the reference clock divider bits (see Figure 8-1 for details). A value of '0' selects no divider.

bit 15 **ON:** Output Enable bit(1)
1 = Reference Oscillator module is enabled
0 = Reference Oscillator module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Peripheral Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **OE:** Reference Clock Output Enable bit
1 = Reference clock is driven out on REFCLKOx pin
0 = Reference clock is not driven out on REFCLKOx pin

bit 11 **RSLP:** Reference Oscillator Module Run in Sleep bit(2)
1 = Reference Oscillator module output continues to run in Sleep
0 = Reference Oscillator module output is disabled in Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **DIVSWEN:** Divider Switch Enable bit
1 = Divider switch is in progress
0 = Divider switch is complete

bit 8 **ACTIVE:** Reference Clock Request Status bit(1)
1 = Reference clock request is active
0 = Reference clock request is not active

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits(3)
1111 = Reserved
•
•
•
1001 = BFRC
1000 = REFCLKIx
0111 = System PLL output
0110 = Reserved
0101 = SOSC
0100 = LPRC
0011 = FRC
0010 = POSC
0001 = PBCLK1
0000 = SYSCLK

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.
2: This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.
3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

TABLE 12-7: PORTC REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	—	—	—	—	—	F000
0220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUC15	CNPUC14	CNPUC13	CNPUC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
0260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDC15	CNPDC14	CNPDC13	CNPDC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
0270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0280	CNENC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNENC15	CNENC14	CNENC13	CNENC12													0000
0290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATC15	CNSTATC14	CNSTATC13	CNSTATC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
02A0	CNNEC	31:16	—	—		—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEC15	CNNEC14	CNNEC13	CNNEC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
02B0	CNFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFC15	CNFC14	CNFC13	CNFC12	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 17-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	—	—	—	FEDGE	C32
7:0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
	ICTMR(1)	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Bit Value at POR: (‘0’, ‘1’, x = unknown)	P = Programmable bit	r = Reserved bit

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Input Capture Module Enable bit
- 1 = Module is enabled
- 0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = Halt in CPU Idle mode
- 0 = Continue to operate in CPU Idle mode

bit 12-10 **Unimplemented:** Read as ‘0’

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
- 1 = Capture rising edge first
- 0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit
- 1 = 32-bit timer resource capture
- 0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is ‘1’)(1)
- 0 = Timery is the counter source for capture
- 1 = Timerx is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits
- 11 = Interrupt on every fourth capture event
- 10 = Interrupt on every third capture event
- 01 = Interrupt on every second capture event
- 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
- 1 = Input capture overflow is occurred
- 0 = No input capture overflow is occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
- 1 = Input capture buffer is not empty; at least one more capture value can be read
- 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
- 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
- 110 = Simple Capture Event mode – every edge, specified edge first and every edge thereafter
- 101 = Prescaled Capture Event mode – every sixteenth rising edge
- 100 = Prescaled Capture Event mode – every fourth rising edge
- 011 = Simple Capture Event mode – every rising edge
- 010 = Simple Capture Event mode – every falling edge
- 001 = Edge Detect mode – every edge (rising and falling)
- 000 = Input Capture module is disabled

Note 1: Refer to Table 17-1 for Timerx and Timery selections.

NOTES:

REGISTER 20-8: SQI1INTEN: SQI INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DMAEIE	PKTCOMPIE	BDDONEIE	CONTHRIE
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CONEMPTYIE	CONFULLIE	RXTHRIE	RXFULLIE	RXEMPTYIE	TXTHRIE	TXFULLIE	TXEMPTYIE

Legend:	HS = Hardware Set		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11 **DMAEIE:** DMA Bus Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 10 **PKTCOMPIE:** DMA Buffer Descriptor Packet Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 9 **BDDONEIE:** DMA Buffer Descriptor Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 8 **CONTHRIE:** Control Buffer Threshold Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 7 **CONEMPTYIE:** Control Buffer Empty Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **CONFULLIE:** Control Buffer Full Interrupt Enable bit
This bit enables an interrupt when the receive FIFO buffer is full.
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **RXTHRIE:** Receive Buffer Threshold Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 4 **RXFULLIE:** Receive Buffer Full Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **RXEMPTYIE:** Receive Buffer Empty Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 2 **TXTHRIE:** Transmit Threshold Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **TXFULLIE:** Transmit Buffer Full Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 0 **TXEMPTYIE:** Transmit Buffer Empty Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

REGISTER 23-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0, HC	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
	RDSTART	—	—	—	—	—	DUALBUF	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	CSF<1:0>(1)		ALP(1)	CS2P(1)	CS1P(1)	—	WRSP	RDSP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **RDSTART:** Start Read on PMP Bus bit
This bit is cleared by hardware at the end of the read cycle.
1 = Start a read cycle on the PMP bus
0 = No effect

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **DUALBUF:** Dual Read/Write Buffers enable bit
This bit is valid in Master mode only.
1 = PMP uses separate registers for reads and writes (PMRADDR, PMDATAIN, PMWADDR, PMDATAOUT)
0 = PMP uses legacy registers (PMADDR, PMDATA)

bit 16 **Unimplemented:** Read as '0'

bit 15 **ON:** Parallel Master Port Enable bit
1 = PMP is enabled
0 = PMP is disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
11 = Lower 8 bits of address are multiplexed on PMD<15:0> pins; upper 8 bits are not used
10 = All 16 bits of address are multiplexed on PMD<15:0> pins
01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<15:8>
00 = Address and data appear on separate pins

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
1 = PMP module uses TTL input buffers
0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
1 = PMWR/PMENB port is enabled
0 = PMWR/PMENB port is disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
1 = PMRD/PMWR port is enabled
0 = PMRD/PMWR port is disabled

Note 1: These bits have no effect when their corresponding pins are used as address lines.

REGISTER 23-6: PMAEN: PARALLEL PORT PIN ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTEN<15:14>		PTEN<13:8>					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 15-14 **PTEN<15:14>:** PMCS1 Strobe Enable bits
- 1 = PMA15 and PMA14 function as either PMA<15:14> or PMCS1 and PMCS2**(1)**
- 0 = PMA15 and PMA14 function as port I/O

bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits
- 1 = PMA<13:2> function as PMP address lines
- 0 = PMA<13:2> function as port I/O

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Strobe Enable bits
- 1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL**(2)**
- 0 = PMA1 and PMA0 pads function as port I/O

Note 1: The use of these pins as PMA15 and PMA14 or CS1 and CS2 is selected by the CSF<1:0> bits in the PMCON register.

2: The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by bits ADRMUX<1:0> in the PMCON register.

REGISTER 28-1: ADCCON1: ADC CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRBEN	TRBERR	TRBMST<2:0>			TRBSLV<2:0>		
23:16	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRACT	SELRES<1:0>		STRGSRC<4:0>				
15:8	R/W-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	U-0
	ON		SIDL	AICPMPEN	CVDEN	FSSCLKEN	FSPBCLKEN	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	—	IRQVS<2:0>			STRGLVL	—	—	—

Legend:	HC = Hardware Set	HS = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **TRBEN:** Turbo Channel Enable bit
1 = Enable the Turbo channel
0 = Disable the Turbo channel

bit 30 **TRBERR:** Turbo Channel Error Status bit
1 = An error occurred while setting the Turbo channel and Turbo channel function to be disabled regardless of the TRBEN bit being set to '1'.
0 = Turbo channel error did not occur

Note: The status of this bit is valid only after the TRBEN bit is set.

bit 29-27 **TRBMST<2:0>:** Turbo Master ADCx bits
111 = Reserved
110 = ADC4 is selected as the Turbo Master
•
•
•
000 = ADC0 is selected as the Turbo Master

bit 26-24 **TRBSLV<2:0>:** Turbo Slave ADCx bits
111 = Reserved
110 = ADC4 is selected as the Turbo Slave
•
•
•
000 = ADC0 is selected as the Turbo Slave

bit 23 **FRACT:** Fractional Data Output Format bit
1 = Fractional
0 = Integer

bit 22-21 **SELRES<1:0>:** Shared ADC (ADC7) Resolution bits
11 = 12 bits (default)
10 = 10 bits
01 = 8 bits
00 = 6 bits

Note: Changing the resolution of the ADC does not shift the result in the corresponding ADCDATAx register. The result will still occupy 12 bits, with the corresponding lower unused bits set to '0'. For example, a resolution of 6 bits will result in ADCDATAx<5:0> being set to '0', and ADCDATAx<11:6> holding the result.

REGISTER 28-6: ADCIMCON2: ADC INPUT MODE CONTROL REGISTER 2 (CONTINUED)

bit 6 **SIGN19:** AN19 Signed Data Mode bit(1)
1 = AN19 is using Signed Data mode
0 = AN19 is using Unsigned Data mode

bit 5 **DIFF18:** AN18 Mode bit
1 = AN18 is using Differential mode
0 = AN18 is using Single-ended mode

bit 4 **SIGN18:** AN18 Signed Data Mode bit
1 = AN18 is using Signed Data mode
0 = AN18 is using Unsigned Data mode

bit 3 **DIFF17:** AN17 Mode bit
1 = AN17 is using Differential mode
0 = AN17 is using Single-ended mode

bit 2 **SIGN17:** AN17 Signed Data Mode bit
1 = AN17 is using Signed Data mode
0 = AN17 is using Unsigned Data mode

bit 1 **DIFF16:** AN16 Mode bit
1 = AN16 is using Differential mode
0 = AN16 is using Single-ended mode

bit 0 **SIGN16:** AN16 Signed Data Mode bit
1 = AN16 is using Signed Data mode
0 = AN16 is using Unsigned Data mode

Note 1: This bit is not available on 64-pin devices.

NOTES:

39.0 252 MHz ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MZ EF electrical characteristics for devices running at 252 MHz. Additional information will be provided in future revisions of this document as it becomes available.

The specifications for 252 MHz are identical to those shown in **37.0 "Electrical Characteristics"** including absolute maximum ratings, with the exception of the parameters listed in this chapter.

Parameters in this chapter begin with the letter "M", which denotes 252 MHz operation. For example, parameter DC27a in **37.0 "Electrical Characteristics"**, is the up to 200 MHz operation equivalent for MDC27a.

NOTES:

Revision D (July 2016)

This revision includes the following major changes, which are referenced by their respective chapter in Table C-3.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE C-3: MAJOR SECTION UPDATES

Section Name	Update Description
32-bit MCUs (up to 2 MB Live-Update Flash and 512 KB SRAM) with FPU, Audio and Graphics Interfaces, HS USB, Ethernet, and Advanced Analog	Updated the Operating Conditions and Core MHz values. The XFBGA package was renamed to TFBGA.
20.0 "Serial Quad Interface (SQI)"	The CLKDIV<9:0> bits in the SQI1CLKCON register were updated (see Register 20-5). The THRES<4:0> bits in the SQI1THR register were updated (see Register 20-21).
37.0 "Electrical Characteristics"	The Program Flash Memory Wait States were updated (see Table 37-13). The minimum value for System Time Requirements parameter OS51 (when the USB module is enabled) was updated (see Table 37-18).
39.0 "252 MHz Electrical Characteristics"	This chapter was added.
Appendix A: "Migrating from PIC32MX5XX/6XX/7XX to PIC32MZ EF"	The new ADC module reference was updated (see **A.2 "Analog-to-Digital Converter (ADC)"**). ADC Calibration was added to **B.2 "Analog-to-Digital Converter (ADC)"**
Appendix B: "Migrating from PIC32MZ EC to PIC32MZ EF"	The Device Configuration and Control Differences (Table B-8) were updated to include the Boot Flash Sequence. **B.10 "Serial Quad Interface (SQI)"** was updated.
Product Identification System	The Speed category was added.