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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	Ethernet, I <sup>2</sup> C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	46
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efg064-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efg064-i-pt</a>

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**TABLE 3: PIN NAMES FOR 100-PIN DEVICES**

100-PIN TQFP (TOP VIEW)			
<b>PIC32MZ0512EF(E/F/K)100</b> <b>PIC32MZ1024EF(G/H/M)100</b> <b>PIC32MZ1024EF(E/F/K)100</b> <b>PIC32MZ2048EF(G/H/M)100</b>			
		100	1
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN23/AERXERR/RG15	36	Vss
2	EBIA5/AN34/PMA5/RA5	37	VDD
3	EBID5/AN17/RPE5/PMD5/RE5	38	TCK/EBIA19/AN29/RA1
4	EBID6/AN16/PMD6/RE6	39	TDI/EBIA18/AN30/RPF13/SCK5/RF13
5	EBID7/AN15/PMD7/RE7	40	TDO/EBIA17/AN31/RPF12/RF12
6	EBIA6/AN22/RPC1/PMA6/RC1	41	EBIA11/AN7/ERXD0/AECRS/PMA11/RB12
7	EBIA12/AN21/RPC2/PMA12/RC2	42	AN8/ERXD1/AECOL/RB13
8	EBIWE/AN20/RPC3/PMWR/RC3	43	EBIA1/AN9/ERXD2/AETXD3/RPB14/SCK3/PMA1/RB14
9	EBIOE/AN19/RPC4/PMRD/RC4	44	EBIA0/AN10/ERXD3/AETXD2/RPB15/OCFB/PMA0/RB15
10	AN14/C1IND/ECOL/RPG6/SCK2/RG6	45	Vss
11	EBIA4/AN13/C1INC/ECRS/RPG7/SDA4/PMA4/RG7	46	VDD
12	EBIA3/AN12/C2IND/ERXDV/ECRS/SDV/AERXDV/AECRS/SDV/RPG8/SCL4/PMA3/RG8	47	AN32/AETXD0/RPD14/RD14
13	Vss	48	AN33/AETXD1/RPD15/SCK6/RD15
14	VDD	49	OSC1/CLK1/RC12
15	MCLR	50	OSC2/CLK0/RC15
16	EBIA2/AN11/C2INC/ERXCLK/EREFCLK/AERXCLK/AEREFCLK/RPG9/PMA2/RG9	51	VBUS
17	TMS/EBIA16/AN24/RA0	52	VUSB3V3
18	AN25/AERXD0/RPE8/RE8	53	Vss
19	AN26/AERXD1/RPE9/RE9	54	D-
20	AN45/C1INA/RPB5/RB5	55	D+
21	AN4/C1INB/RB4	56	RPF3/USBID/RF3
22	AN3/C2INA/RPB3/RB3	57	EBIRDY3/RPF2/SDA3/RF2
23	AN2/C2INB/RPB2/RB2	58	EBIRDY2/RPF8/SCL3/RF8
24	PGEC1/AN1/RPB1/RB1	59	EBICS0/SCL2/RA2
25	PGED1/AN0/RPB0/RB0	60	EBIRDY1/SDA2/RA3
26	PGEC2/AN46/RPB6/RB6	61	EBIA14/PMCS1/PMA14/RA4
27	PGED2/AN47/RPB7/RB7	62	VDD
28	VREF-/CVREF-/AN27/AERXD2/RA9	63	Vss
29	VREF+/CVREF+/AN28/AERXD3/RA10	64	EBIA9/RPF4/SDA5/PMA9/RF4
30	AVDD	65	EBIA8/RPF5/SCL5/PMA8/RF5
31	AVSS	66	AETXCLK/RPA14/SCL1/RA14
32	EBIA10/AN48/RPB8/PMA10/RB8	67	AETXEN/RPA15/SDA1/RA15
33	EBIA7/AN49/RPB9/PMA7/RB9	68	EBIA15/RPD9/PMCS2/PMA15/RD9
34	EBIA13/CVREFOUT/AN5/RPB10/PMA13/RB10	69	RPD10/SCK4/RD10
35	AN6/ERXERR/AETXERR/RB11	70	EMDC/AEMDC/RPD11/RD11

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 “Peripheral Pin Select (PPS)”** for restrictions.
  - 2: Every I/O port pin (RAX-RGx) can be used as a change notification pin (CNAX-CNGx). See **Section 12.0 “I/O Ports”** for more information.
  - 3: Shaded pins are 5V tolerant.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 5: PIN NAMES FOR 144-PIN DEVICES

144-PIN LQFP AND TQFP (TOP VIEW)		144	
<b>PIC32MZ0512EF(E/F/K)144</b> <b>PIC32MZ1024EF(G/H/M)144</b> <b>PIC32MZ1024EF(E/F/K)144</b> <b>PIC32MZ2048EF(G/H/M)144</b>		1	
Pin Number	Full Pin Name	Pin Number	Full Pin Name
1	AN23/RG15	37	PGEC2/AN46/RPB6/RB6
2	EBIA5/AN34/PMA5/RA5	38	PGED2/AN47/RPB7/RB7
3	EBID5/AN17/RPE5/PMD5/RE5	39	VREF-/CVREF-/AN27/RA9
4	EBID6/AN16/PMD6/RE6	40	VREF+/CVREF+/AN28/RA10
5	EBID7/AN15/PMD7/RE7	41	AVDD
6	EBIA6/AN22/RPC1/PMA6/RC1	42	AVSS
7	AN35/ETXD0/RJ8	43	AN38/ETXD2/RH0
8	AN36/ETXD1/RJ9	44	AN39/ETXD3/RH1
9	EBIBS0/RJ12	45	EBIRP/RH2
10	EBIBS1/RJ10	46	RH3
11	EBIA12/AN21/RPC2/PMA12/RC2	47	EBIA10/AN48/RPB8/PMA10/RB8
12	EBIWE/AN20/RPC3/PMWR/RC3	48	EBIA7/AN49/RPB9/PMA7/RB9
13	EBIOE/AN19/RPC4/PMRD/RC4	49	CVREFOUT/AN5/RPB10/RB10
14	AN14/C1IND/RPG6/SCK2/RG6	50	AN6/RB11
15	AN13/C1INC/RPG7/SDA4/RG7	51	EBIA1/PMA1/RK1
16	AN12/C2IND/RPG8/SCL4/RG8	52	EBIA3/PMA3/RK2
17	Vss	53	EBIA17/RK3
18	VDD	54	Vss
19	EBIA16/RK0	55	VDD
20	MCLR	56	TCK/AN29/RA1
21	EBIA2/AN11/C2INC/RPG9/PMA2/RG9	57	TDI/AN30/RPF13/SCK5/RF13
22	TMS/AN24/RA0	58	TDO/AN31/RPF12/RF12
23	AN25/RPE8/RE8	59	AN7/RB12
24	AN26/RPE9/RE9	60	AN8/RB13
25	AN45/C1INA/RPB5/RB5	61	AN9/RPB14/SCK3/RB14
26	AN4/C1INB/RB4	62	AN10/RPB15/OCFB/RB15
27	AN37/ERXCLK/EREFCLK/RJ11	63	Vss
28	EBIA13/PMA13/RJ13	64	VDD
29	EBIA11/PMA11/RJ14	65	AN40/ERXERR/RH4
30	EBIA0/PMA0/RJ15	66	AN41/ERXD1/RH5
31	AN3/C2INA/RPB3/RB3	67	AN42/ERXD2/RH6
32	Vss	68	EBIA4/PMA4/RH7
33	VDD	69	AN32/RPD14/RD14
34	AN2/C2INB/RPB2/RB2	70	AN33/RPD15/SCK6/RD15
35	PGEC1/AN1/RPB1/RB1	71	OSC1/CLKI/RC12
36	PGED1/AN0/RPB0/RB0	72	OSC2/CLKO/RC15

- Note** 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 “Peripheral Pin Select (PPS)”** for restrictions.
- 2: Every I/O port pin (RAX-RKx) can be used as a change notification pin (CNAx-CNKx). See **Section 12.0 “I/O Ports”** for more information.
- 3: Shaded pins are 5V tolerant.

## 3.1.4 FLOATING POINT UNIT (FPU)

The Floating Point Unit (FPU), Coprocessor (CP1), implements the MIPS Instruction Set Architecture for floating point computation. The implementation supports the ANSI/IEEE Standard 754 (IEEE for Binary Floating Point Arithmetic) for 32-bit and 64-bit floating point data formats. The FPU can be programmed to have thirty-two 32-bit or 64-bit floating point registers used for floating point operations.

The performance is optimized for 32-bit formats. Most instructions have one FPU cycle throughput and four FPU cycle latency. The FPU implements the multiply-add (MADD) and multiply-sub (MSUB) instructions with intermediate rounding after the multiply function. The result is guaranteed to be the same as executing a MUL and an ADD instruction separately, but the instruction latency, instruction fetch, dispatch bandwidth, and the total number of register accesses are improved.

IEEE denormalized input operands and results are supported by hardware for some instructions. IEEE denormalized results are not supported by hardware in general, but a fast flush-to-zero mode is provided to optimize performance. The fast flush-to-zero mode is enabled through the FCCR register, and use of this mode is recommended for best performance when denormalized results are generated.

The FPU has a separate pipeline for floating point instruction execution. This pipeline operates in parallel with the integer core pipeline and does not stall when the integer pipeline stalls. This allows long-running FPU operations, such as divide or square root, to be partially masked by system stalls and/or other integer unit instructions. Arithmetic instructions are always dispatched and completed in order, but loads and stores can complete out of order. The exception model is “precise” at all times.

Table 3-4 contains the floating point instruction latencies and repeat rates for the processor core. In this table, 'Latency' refers to the number of FPU cycles necessary for the first instruction to produce the result needed by the second instruction. The “Repeat Rate” refers to the maximum rate at which an instruction can be executed per FPU cycle.

**TABLE 3-4: FPU INSTRUCTION LATENCIES AND REPEAT RATES**

Op code	Latency (FPU Cycles)	Repeat Rate (FPU Cycles)
ABS.[S,D], NEG.[S,D], ADD.[S,D], SUB.[S,D], C.cond.[S,D], MUL.S	4	1
MADD.S, MSUB.S, NMADD.S, NMSUB.S, CABS.cond.[S,D]	4	1
CVT.D.S, CVT.PS.PW, CVT.[S,D].[W,L]	4	1
CVT.S.D, CVT.[W,L].[S,D], CEIL.[W,L].[S,D], FLOOR.[W,L].[S,D], ROUND.[W,L].[S,D], TRUNC.[W,L].[S,D]	4	1
MOV.[S,D], MOVF.[S,D], MOVN.[S,D], MOVT.[S,D], MOVZ.[S,D]	4	1
MUL.D	5	2
MADD.D, MSUB.D, NMADD.D, NMSUB.D	5	2
RECIP.S	13	10
RECIP.D	26	21
RSQRT.S	17	14
RSQRT.D	36	31
DIV.S, SQRT.S	17	14
DIV.D, SQRT.D	32	29
MTC1, DMTC1, LWC1, LDC1, LDXC1, LUXC1, LWXC1	4	1
MFC1, DMFC1, SWC1, SDC1, SDXC1, SUXC1, SWXC1	1	1

**Legend:** S = Single (32-bit) D = Double (64-bit)  
W = Word (32-bit) L = Long word (64-bit)

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 6-4: PWRCON: POWER CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	VREGS

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **VREGS:** Voltage Regulator Stand-by Enable bit

1 = Voltage regulator will remain active during Sleep

0 = Voltage regulator will go to Stand-by mode during Sleep

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name <sup>(1)</sup>	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0584	OFF017	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
0588	OFF018	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
058C	OFF019	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
0590	OFF020	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
0594	OFF021	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
0598	OFF022	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
059C	OFF023	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05A0	OFF024	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05A4	OFF025	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05A8	OFF026	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05AC	OFF027	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05B0	OFF028	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05B4	OFF029	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05B8	OFF030	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
05BC	OFF031	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.
- 2: This bit or register is not available on 64-pin devices.
- 3: This bit or register is not available on devices without a CAN module.
- 4: This bit or register is not available on 100-pin devices.
- 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
- 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
- 7: This bit or register is not available on devices without a Crypto module.
- 8: This bit or register is not available on 124-pin devices.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 11-20: USBDMINT: USB DMA INTERRUPT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS
	DMA8IF	DMA7IF	DMA6IF	DMA5IF	DMA4IF	DMA3IF	DMA2IF	DMA1IF

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **DMAxIF:** DMA Channel 'x' Interrupt bit

1 = The DMA channel has an interrupt event

0 = No interrupt event

All bits are cleared on a read of the register.

**TABLE 12-3: OUTPUT PIN SELECTION (CONTINUED)**

RPN Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPD1	RPD1R	RPD1R<3:0>	0000 = No Connect 0001 = U1RTS 0010 = U2TX 0011 = U5RTS 0100 = U6TX 0101 = Reserved 0110 = SS2 0111 = Reserved 1000 = SDO4 1001 = Reserved 1010 = SDO6 <sup>(1)</sup> 1011 = OC2 1100 = OC1 1101 = OC9 1110 = Reserved 1111 = C2TX <sup>(3)</sup>
RPG9	RPG9R	RPG9R<3:0>	
RPB14	RPB14R	RPB14R<3:0>	
RPD0	RPD0R	RPD0R<3:0>	
RPB6	RPB6R	RPB6R<3:0>	
RPD5	RPD5R	RPD5R<3:0>	
RPB2	RPB2R	RPB2R<3:0>	
RPF3	RPF3R	RPF3R<3:0>	
RPF13 <sup>(1)</sup>	RPF13R <sup>(1)</sup>	RPF13R<3:0> <sup>(1)</sup>	
RPC2 <sup>(1)</sup>	RPC2R <sup>(1)</sup>	RPC2R<3:0> <sup>(1)</sup>	
RPE8 <sup>(1)</sup>	RPE8R <sup>(1)</sup>	RPE8R<3:0> <sup>(1)</sup>	
RPF2 <sup>(1)</sup>	RPF2R <sup>(1)</sup>	RPF2R<3:0> <sup>(1)</sup>	

**Note 1:** This selection is not available on 64-pin devices.

**2:** This selection is not available on 64-pin or 100-pin devices.

**3:** This selection is not available on devices without a CAN module.



TABLE 20-1: SERIAL QUADRATURE INTERFACE (SQI) REGISTER MAP (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
2044	SQI1BD STAT	31:16	—	—	—	—	—	—	—	—	—	BDSTATE<3:0>					DMA START	DMAACTV	0000
		15:0	BDCON<15:0>																0000
2048	SQI1BD POLLCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	POLLCON<15:0>																0000
204C	SQI1BD TXDSTAT	31:16	—	—	—	TXSTATE<3:0>				—	—	—	—	TXBUFCNT<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	TXCURBUFLEN<7:0>								0000
2050	SQI1BD RXDSTAT	31:16	—	—	—	RXSTATE<3:0>				—	—	—	—	RXBUFCNT<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	RXCURBUFLEN<7:0>								0000
2054	SQI1THR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	THRES<4:0>					0000	
2058	SQI1INT SIGEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	DMAEISE	PKT DONEISE	BD DONEISE	CON THRISE	CON EMPTYISE	CON FULLISE	RX THRISE	RX FULLISE	RX EMPTYISE	TX THRISE	TX FULLISE	TX EMPTYISE	0000
205C	SQI1 TAPCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	CLKINDLY<5:0>						DATAOUTDLY<3:0>				CLKOUTDLY<3:0>				0000
2060	SQI1 MEMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	STATPOS	TYPESTAT<1:0>		STATBYTES<1:0>		0000
		15:0	STATDATA<15:0>																0000
2064	SQI1 XCON3	31:16	—	—	—	INIT1 SCHECK	INIT1COUNT<1:0>		INIT1TYPE<1:0>		INIT1CMD3<7:0>								0000
		15:0	INIT1CMD2<7:0>								INIT1CMD1<7:0>								0000
2068	SQI1 XCON4	31:16	—	—	—	INIT2 SCHECK	INIT2COUNT<1:0>		INIT2TYPE<1:0>		INIT2CMD3<7:0>								0000
		15:0	INIT2CMD2<7:0>								INIT2CMD1<7:0>								0000

## REGISTER 22-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 7-6    **URXISEL<1:0>**: Receive Interrupt Mode Selection bit  
11 = Reserved  
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full  
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full  
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)
- bit 5    **ADDEN**: Address Character Detect bit (bit 8 of received data = 1)  
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect  
0 = Address Detect mode is disabled
- bit 4    **RIDLE**: Receiver Idle bit (read-only)  
1 = Receiver is Idle  
0 = Data is being received
- bit 3    **PERR**: Parity Error Status bit (read-only)  
1 = Parity error has been detected for the current character  
0 = Parity error has not been detected
- bit 2    **FERR**: Framing Error Status bit (read-only)  
1 = Framing error has been detected for the current character  
0 = Framing error has not been detected
- bit 1    **OERR**: Receive Buffer Overrun Error Status bit.  
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to empty state.  
1 = Receive buffer has overflowed  
0 = Receive buffer has not overflowed
- bit 0    **URXDA**: Receive Buffer Data Available bit (read-only)  
1 = Receive buffer has data, at least one more character can be read  
0 = Receive buffer is empty

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 26-3: CEBDADDR: CRYPTO ENGINE BUFFER DESCRIPTOR REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **BDPADDR<31:0>**: Current Buffer Descriptor Process Address Status bits

These bits contain the current descriptor address that is being processed by the Buffer Descriptor Processor (BDP).

**REGISTER 26-4: CEBDPADDR: CRYPTO ENGINE BUFFER DESCRIPTOR PROCESSOR REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **BASEADDR<31:0>**: Buffer Descriptor Base Address bits

These bits contain the physical address of the first Buffer Descriptor in the Buffer Descriptor chain. When enabled, the Crypto DMA begins fetching Buffer Descriptors from this address.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 27-3: RNGPOLYx: RANDOM NUMBER GENERATOR POLYNOMIAL REGISTER 'x'**  
(**'x' = 1 OR 2**)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	POLY<31:24>							
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	POLY<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLY<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLY<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **POLY<31:0>**: PRNG LFSR Polynomial MSb/LSb bits (RNGPOLY1 = LSb, RNGPOLY2 = MSb)

**REGISTER 27-4: RNGNUMGENx: RANDOM NUMBER GENERATOR REGISTER 'x' ('x' = 1 OR 2)**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RNG<31:24>							
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RNG<23:16>							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RNG<15:8>							
7:0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RNG<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **RNG<31:0>**: Current PRNG MSb/LSb Value bits (RNGNUMGEN1 = LSb, RNGNUMGEN2 = MSb)

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 28-15: ADCCMPx: ADC DIGITAL COMPARATOR 'x' LIMIT VALUE REGISTER  
( 'x' = 1 THROUGH 6 )**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPHI<15:8> <sup>(1,2,3)</sup>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPHI<7:0> <sup>(1,2,3)</sup>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPLO<15:8> <sup>(1,2,3)</sup>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPLO<7:0> <sup>(1,2,3)</sup>							

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 31-16 **DCMPHI<15:0>**: Digital Comparator 'x' High Limit Value bits<sup>(1,2,3)</sup>

These bits store the high limit value, which is used by digital comparator for comparisons with ADC converted data.

bit 15-0 **DCMPLO<15:0>**: Digital Comparator 'x' Low Limit Value bits<sup>(1,2,3)</sup>

These bits store the low limit value, which is used by digital comparator for comparisons with ADC converted data.

- Note 1:** Changing these bits while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.
- 2:** The format of the limit values should match the format of the ADC converted value in terms of sign and fractional settings.
- 3:** For Digital Comparator 0 used in CVD mode, the DCM PHI<15:0> and DCMPLO<15:0> bits must always be specified in signed format, as the CVD output data is differential and is always signed.

## REGISTER 29-21: CiFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' ('n' = 0-31) (CONTINUED)

- bit 9     **TXHALFIF**: FIFO Transmit FIFO Half Empty Interrupt Flag bit<sup>(1)</sup>  
    TXEN = 1: (FIFO configured as a Transmit Buffer)  
    1 = FIFO is  $\leq$  half full  
    0 = FIFO is  $>$  half full  
    TXEN = 0: (FIFO configured as a Receive Buffer)  
    Unused, reads '0'
- bit 8     **TXEMPTYIF**: Transmit FIFO Empty Interrupt Flag bit<sup>(1)</sup>  
    TXEN = 1: (FIFO configured as a Transmit Buffer)  
    1 = FIFO is empty  
    0 = FIFO is not empty, at least 1 message queued to be transmitted  
    TXEN = 0: (FIFO configured as a Receive Buffer)  
    Unused, reads '0'
- bit 7-4   **Unimplemented**: Read as '0'
- bit 3     **RXOVFLIF**: Receive FIFO Overflow Interrupt Flag bit  
    TXEN = 1: (FIFO configured as a Transmit Buffer)  
    Unused, reads '0'  
    TXEN = 0: (FIFO configured as a Receive Buffer)  
    1 = Overflow event has occurred  
    0 = No overflow event occurred
- bit 2     **RXFULLIF**: Receive FIFO Full Interrupt Flag bit<sup>(1)</sup>  
    TXEN = 1: (FIFO configured as a Transmit Buffer)  
    Unused, reads '0'  
    TXEN = 0: (FIFO configured as a Receive Buffer)  
    1 = FIFO is full  
    0 = FIFO is not full
- bit 1     **RXHALFIF**: Receive FIFO Half Full Interrupt Flag bit<sup>(1)</sup>  
    TXEN = 1: (FIFO configured as a Transmit Buffer)  
    Unused, reads '0'  
    TXEN = 0: (FIFO configured as a Receive Buffer)  
    1 = FIFO is  $\geq$  half full  
    0 = FIFO is  $<$  half full
- bit 0     **RXEMPTYIF**: Receive Buffer Not Empty Interrupt Flag bit<sup>(1)</sup>  
    TXEN = 1: (FIFO configured as a Transmit Buffer)  
    Unused, reads '0'  
    TXEN = 0: (FIFO configured as a Receive Buffer)  
    1 = FIFO is not empty, has at least 1 message  
    0 = FIFO is empty

**Note 1:** This bit is read-only and reflects the status of the FIFO.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 30-23: EMAC1CFG1: ETHERNET CONTROLLER MAC CONFIGURATION 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-1	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	SOFT RESET	SIM RESET	—	—	RESET RMCS	RESET RFUN	RESET TMCS	RESET TFUN
7:0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1
	—	—	—	LOOPBACK	TX PAUSE	RX PAUSE	PASSALL	RX ENABLE

### Legend:

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit, read as '0'  
'0' = Bit is cleared  
x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SOFTRESET:** Soft Reset bit

Setting this bit will put the MACMII in reset. Its default value is '1'.

bit 14 **SIMRESET:** Simulation Reset bit

Setting this bit will cause a reset to the random number generator within the Transmit Function.

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **RESETRMCS:** Reset MCS/RX bit

Setting this bit will put the MAC Control Sub-layer/Receive domain logic in reset.

bit 10 **RESETRFUN:** Reset RX Function bit

Setting this bit will put the MAC Receive function logic in reset.

bit 9 **RESETTMCS:** Reset MCS/TX bit

Setting this bit will put the MAC Control Sub-layer/TX domain logic in reset.

bit 8 **RESETTFUN:** Reset TX Function bit

Setting this bit will put the MAC Transmit function logic in reset.

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **LOOPBACK:** MAC Loopback mode bit

1 = MAC Transmit interface is loop backed to the MAC Receive interface  
0 = MAC normal operation

bit 3 **TXPAUSE:** MAC TX Flow Control bit

1 = PAUSE Flow Control frames are allowed to be transmitted  
0 = PAUSE Flow Control frames are blocked

bit 2 **RXPAUSE:** MAC RX Flow Control bit

1 = The MAC acts upon received PAUSE Flow Control frames  
0 = Received PAUSE Flow Control frames are ignored

bit 1 **PASSALL:** MAC Pass all Receive Frames bit

1 = The MAC will accept all frames regardless of type (Normal vs. Control)  
0 = The received Control frames are ignored

bit 0 **RXENABLE:** MAC Receive Enable bit

1 = Enable the MAC receiving of frames  
0 = Disable the MAC receiving of frames

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

## 34.0 SPECIAL FEATURES

**Note:** This data sheet summarizes the features of the PIC32MZ EF family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 32. “Configuration”** (DS60001124) and **Section 33. “Programming and Diagnostics”** (DS60001129) in the *“PIC32 Family Reference Manual”*, which are available from the Microchip web site ([www.microchip.com/PIC32](http://www.microchip.com/PIC32)).

PIC32MZ EF devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

- Flexible device configuration
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming™ (ICSP™)
- Internal temperature sensor

### 34.1 Configuration Bits

PIC32MZ EF devices contain two Boot Flash memories (Boot Flash 1 and Boot Flash 2), each with an associated configuration space. These configuration spaces can be programmed to contain various device configurations. Configuration space that is aliased by the Lower Boot Alias memory region is used to provide values for the following Configuration registers. See 4.1.1 “**Boot Flash Sequence and Configuration Spaces**” for more information.

- DEVSIGN0/ADEVSIGN0: Device Signature Word 0 Register
- DEVCP0/ADEVCP0: Device Code-Protect 0 Register
- DEVCFG0/ADEVCFG0: Device Configuration Word 0
- DEVCFG1/ADEVCFG1: Device Configuration Word 1
- DEVCFG2/ADEVCFG2: Device Configuration Word 2
- DEVCFG3/ADEVCFG3: Device Configuration Word 3
- DEVADCx: Device ADC Calibration Word ‘x’ (‘x’ = 0-4, 7)

The following run-time programmable Configuration registers provide additional configuration control:

- CFGCON: Configuration Control Register
- CFGEA: External Bus Interface Address Pin Configuration Register
- CFGEIC: External Bus Interface Control Pin Configuration Register
- CFGPG: Permission Group Configuration Register

In addition, the DEVID register provides device and revision information, the DEVADC0-DEVADC4 and DEVADC7 registers provide ADC module calibration/configuration data, and the DEVSNO and DEVSN1 registers contain a unique serial number of the device.

**Note:** Do not use Word program operation (NVMOP<3:0> = 0001) when programming the device Words that are described in this section.



## REGISTER 34-4: DEVCFG1/ADEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

bit 20-16 **WDTPS<4:0>**: Watchdog Timer Postscale Select bits

10100 = 1:1048576  
10011 = 1:524288  
10010 = 1:262144  
10001 = 1:131072  
10000 = 1:65536  
01111 = 1:32768  
01110 = 1:16384  
01101 = 1:8192  
01100 = 1:4096  
01011 = 1:2048  
01010 = 1:1024  
01001 = 1:512  
01000 = 1:256  
00111 = 1:128  
00110 = 1:64  
00101 = 1:32  
00100 = 1:16  
00011 = 1:8  
00010 = 1:4  
00001 = 1:2  
00000 = 1:1

All other combinations not shown result in operation = 10100

bit 15-14 **FCKSM<1:0>**: Clock Switching and Monitoring Selection Configuration bits

11 = Clock switching is enabled and clock monitoring is enabled  
10 = Clock switching is disabled and clock monitoring is enabled  
01 = Clock switching is enabled and clock monitoring is disabled  
00 = Clock switching is disabled and clock monitoring is disabled

bit 13-11 **Reserved**: Write as '1'

bit 10 **OSCIOFNC**: CLKO Enable Configuration bit

1 = CLKO output disabled  
0 = CLKO output signal active on the OSC2 pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)

bit 9-8 **POSCMOD<1:0>**: Primary Oscillator Configuration bits

11 = Posc disabled  
10 = HS Oscillator mode selected  
01 = Reserved  
00 = EC mode selected

bit 7 **IESO**: Internal External Switchover bit

1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)  
0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)

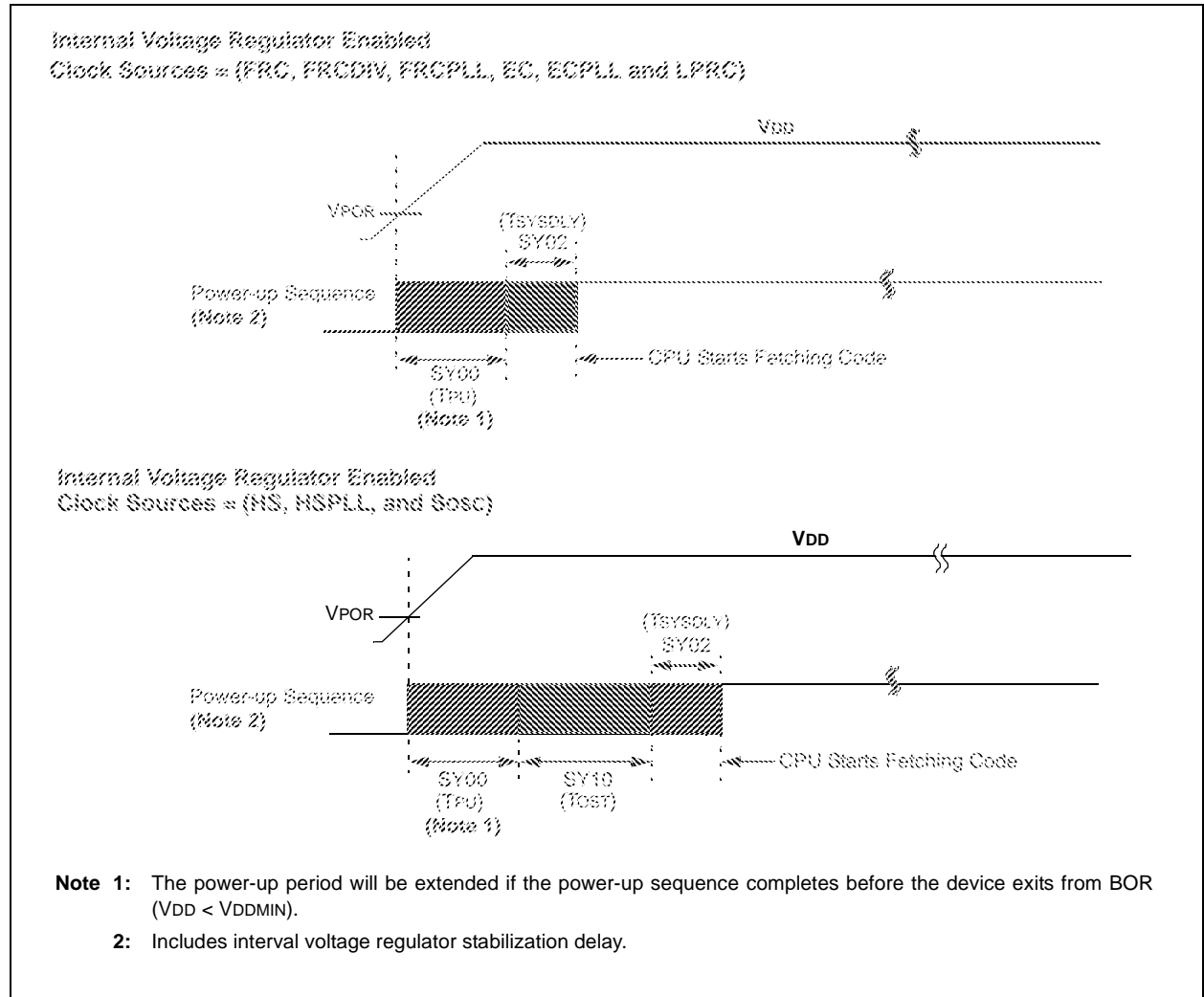
bit 6 **FSOSCEN**: Secondary Oscillator Enable bit

1 = Enable Sosc  
0 = Disable Sosc

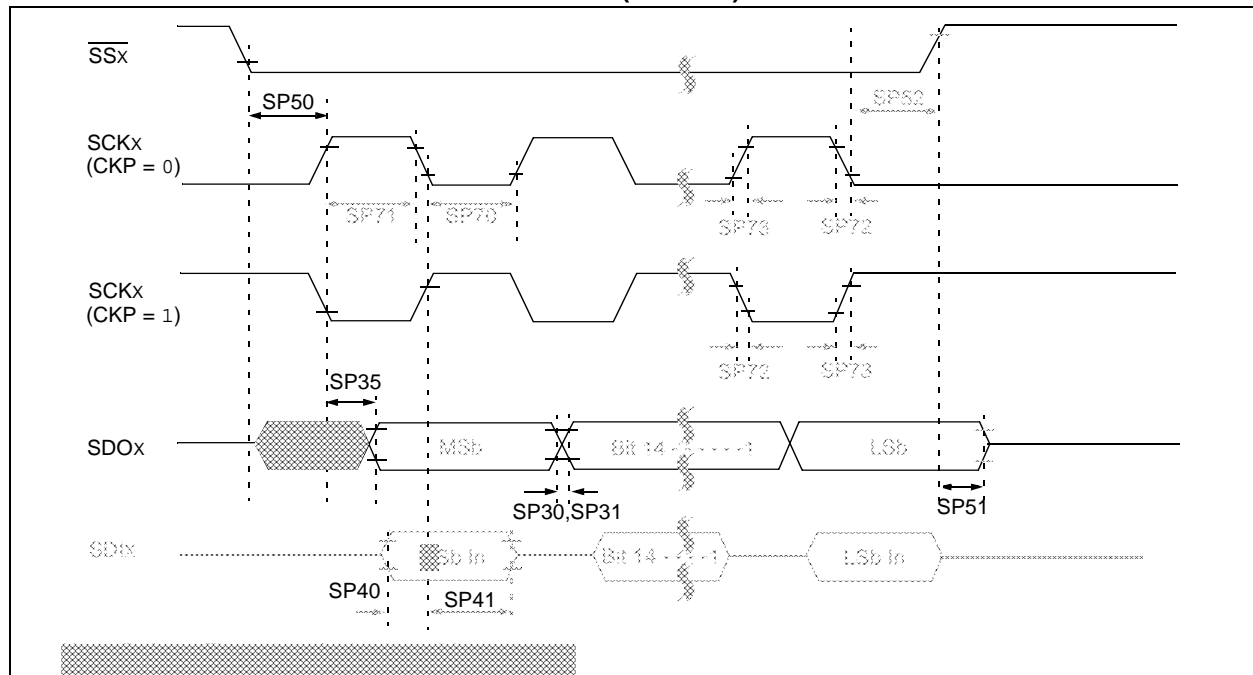
bit 5-3 **DMTINTV<2:0>**: Deadman Timer Count Window Interval bits

111 = Window/Interval value is 127/128 counter value  
110 = Window/Interval value is 63/64 counter value  
101 = Window/Interval value is 31/32 counter value  
100 = Window/Interval value is 15/16 counter value  
011 = Window/Interval value is 7/8 counter value  
010 = Window/Interval value is 3/4 counter value  
001 = Window/Interval value is 1/2 counter value  
000 = Window/Interval value is zero

**FIGURE 37-4: POWER-ON RESET TIMING CHARACTERISTICS**



**FIGURE 37-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS**



**TABLE 37-32: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS**

AC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP70	TscL	SCKx Input Low Time ( <b>Note 3</b> )	Tsck/2	—	—	ns	—
SP71	Tsch	SCKx Input High Time ( <b>Note 3</b> )	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See parameter DO32
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See parameter DO31
SP30	Tdof	SDOx Data Output Fall Time ( <b>Note 4</b> )	—	—	—	ns	See parameter DO32
SP31	Tdor	SDOx Data Output Rise Time ( <b>Note 4</b> )	—	—	—	ns	See parameter DO31
SP35	Tsch2boV, TscL2boV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	VDD > 2.7V
			—	—	10	ns	VDD < 2.7V
SP40	TdIV2sch, TdIV2scL	Setup Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP50	TssL2sch, TssL2scL	SSx ↓ to SCKx ↑ or SCKx Input	88	—	—	ns	—
SP51	TssH2boZ	SSx ↑ to SDOx Output High-Impedance ( <b>Note 3</b> )	2.5	—	12	ns	—
SP52	Tsch2ssh, TscL2ssh	SSx after SCKx Edge	10	—	—	ns	—

**Note 1:** These parameters are characterized, but not tested in manufacturing.

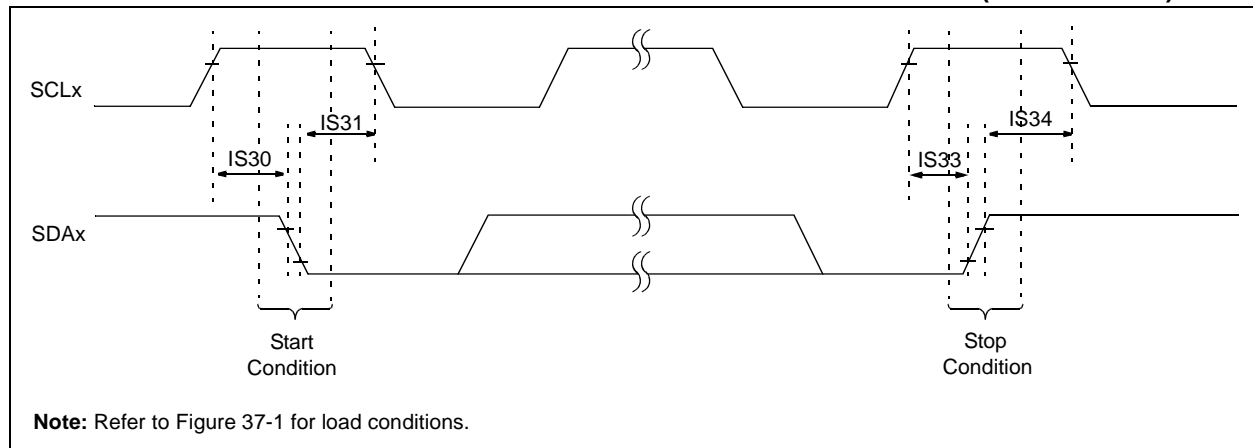
**2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 20 ns.

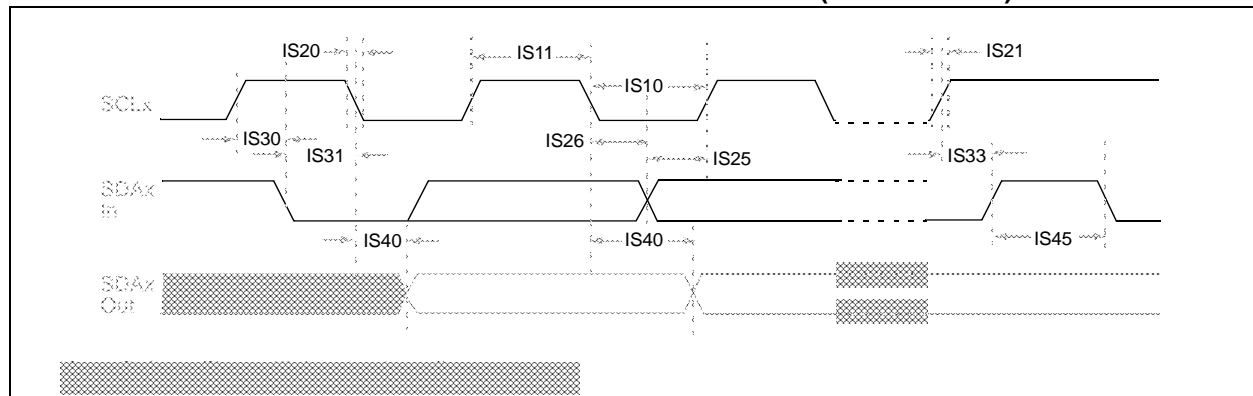
**4:** Assumes 30 pF load on all SPIx pins.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**FIGURE 37-18: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)**



**FIGURE 37-19: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**



**TABLE 37-36: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)**

AC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	1.3	—	μs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode (Note 1)	0.5	—	μs	—
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	0.6	—	μs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode (Note 1)	0.5	—	μs	—

**Note 1:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE C-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
<b>27.0 “Random Number Generator (RNG)”</b>	The TRNGMODE bit was added to the RNGCON register (see Register 27-2).
<b>28.0 “12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)”</b>	<p>The S&amp;H Block Diagram was updated (see Figure 28-2).</p> <p>The registers, ADCTRG4 through ADCTRG8, were removed.</p> <p>The bit value definitions for the ADCSEL&lt;1:0&gt; and CONCLKDIV&lt;5:0&gt; bits in the ADCCON3 register were updated (see Register 28-3).</p> <p>The bit names in the ADC Status registers (Register 28-12 and Register 28-13) were updated to match the names in the SFR summary table.</p> <p>The ADCTRGSNS register was updated (see Register 28-26).</p> <p>The POR values were changed in the ADC System Configuration registers (see Register 28-34 and Register 28-35).</p>
<b>34.0 “Special Features”</b>	The FDBGWP bit was removed from the DEVCFG0/ADEVCFG0 registers (see Register 34-3).
<b>37.0 “Electrical Characteristics”</b>	<p>V-Temp (<math>-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}</math>) information was removed from all tables.</p> <p>The operating conditions voltage range was updated in the Absolute Maximum Ratings and in all tables to: 2.1V to 3.6V.</p> <p>Notes on Maximum value operating conditions were added to the Operating, Idle, and Power-Down Current tables (see Table 37-6, Table 37-7, and Table 37-8, respectively).</p> <p>The conditions for System Timing Requirement parameters OS55a and OS55b were updated (see Table 37-18).</p> <p>The Internal FRC Accuracy specifications were updated (see Table 37-20).</p> <p>The Internal LPRC Accuracy specifications were updated (see Table 37-21).</p> <p>The ADC Module Specifications were updated (see Table 37-38).</p> <p>The Analog-to-Digital Conversion Timing Requirements were updated (see Table 37-39).</p>
<b>Appendix B: “Migrating from PIC32MZ EC to PIC32MZ EF”</b>	This appendix was added, which provides an overview of considerations for migrating from PIC32MZ EC devices to the PIC32MZ EF family of devices.
<b>Product Identification System</b>	V-Temp ( $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ ) information was removed.