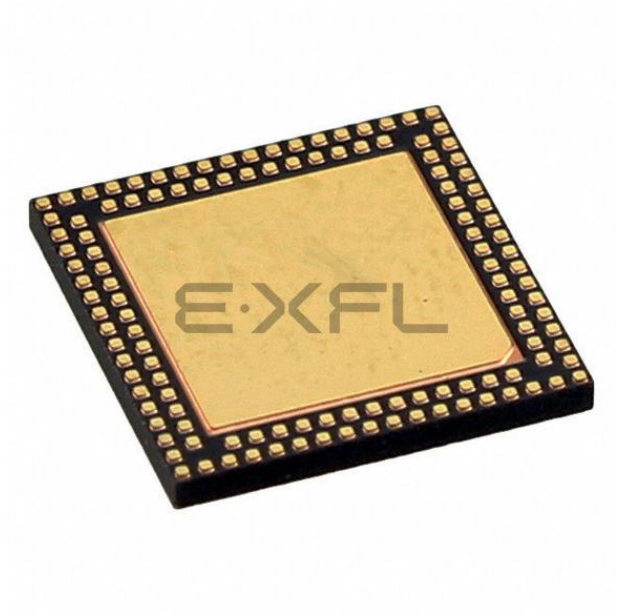

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	97
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efg124-e-tl

TABLE 3: PIN NAMES FOR 100-PIN DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)100
PIC32MZ1024EF(G/H/M)100
PIC32MZ1024EF(E/F/K)100
PIC32MZ2048EF(G/H/M)100

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN23/AERXERR/RG15	36	VSS
2	EBIA5/AN34/PMA5/RA5	37	VDD
3	EBID5/AN17/RPE5/PMD5/RE5	38	TCK/EBIA19/AN29/RA1
4	EBID6/AN16/PMD6/RE6	39	TDI/EBIA18/AN30/RPF13/SCK5/RF13
5	EBID7/AN15/PMD7/RE7	40	TDO/EBIA17/AN31/RPF12/RF12
6	EBIA6/AN22/RPC1/PMA6/RC1	41	EBIA11/AN7/ERXD0/AECRS/PMA11/RB12
7	EBIA12/AN21/RPC2/PMA12/RC2	42	AN8/ERXD1/AECOL/RB13
8	$\overline{\text{EBIWE}}$/AN20/RPC3/PMWR/RC3	43	EBIA1/AN9/ERXD2/AETXD3/RPB14/SCK3/PMA1/RB14
9	$\overline{\text{EBIOE}}$/AN19/RPC4/PMRD/RC4	44	EBIA0/AN10/ERXD3/AETXD2/RPB15/OCFB/PMA0/RB15
10	AN14/C1IND/ECOL/RPG6/SCK2/RG6	45	VSS
11	EBIA4/AN13/C1INC/ECRS/RPG7/SDA4/PMA4/RG7	46	VDD
12	EBIA3/AN12/C2IND/ERXDV/ECRSDV/AERXDV/ AECRSDV/RPG8/SCL4/PMA3/RG8	47	AN32/AETXD0/RPD14/RD14
13	VSS	48	AN33/AETXD1/RPD15/SCK6/RD15
14	VDD	49	OSC1/CLKI/RC12
15	$\overline{\text{MCLR}}$	50	OSC2/CLKO/RC15
16	EBIA2/AN11/C2INC/ERXCLK/EREFCLK/AERXCLK/ AEREFCLK/RPG9/PMA2/RG9	51	VBUS
17	TMS/EBIA16/AN24/RA0	52	VUSB3V3
18	AN25/AERXD0/RPE8/RE8	53	VSS
19	AN26/AERXD1/RPE9/RE9	54	D-
20	AN45/C1INA/RPB5/RB5	55	D+
21	AN4/C1INB/RB4	56	RPF3/USBID/RF3
22	AN3/C2INA/RPB3/RB3	57	EBIRDY3/RPF2/SDA3/RF2
23	AN2/C2INB/RPB2/RB2	58	EBIRDY2/RPF8/SCL3/RF8
24	PGEC1/AN1/RPB1/RB1	59	$\overline{\text{EBICS0}}$/SCL2/RA2
25	PGED1/AN0/RPB0/RB0	60	EBIRDY1/SDA2/RA3
26	PGEC2/AN46/RPB6/RB6	61	EBIA14/PMCS1/PMA14/RA4
27	PGED2/AN47/RPB7/RB7	62	VDD
28	VREF-/CVREF-/AN27/AERXD2/RA9	63	VSS
29	VREF+/CVREF+/AN28/AERXD3/RA10	64	EBIA9/RPF4/SDA5/PMA9/RF4
30	AVDD	65	EBIA8/RPF5/SCL5/PMA8/RF5
31	AVSS	66	AETXCLK/RPA14/SCL1/RA14
32	EBIA10/AN48/RPB8/PMA10/RB8	67	AETXEN/RPA15/SDA1/RA15
33	EBIA7/AN49/RPB9/PMA7/RB9	68	EBIA15/RPD9/PMCS2/PMA15/RD9
34	EBIA13/CVREFOUT/AN5/RPB10/PMA13/RB10	69	RPD10/SCK4/RD10
35	AN6/ERXERR/AETXERR/RB11	70	EMDC/AEMDC/RPD11/RD11

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTD							
RD0	46	71	A48	104	I/O	ST	PORTD is a bidirectional I/O port
RD1	49	76	A52	109	I/O	ST	
RD2	50	77	B42	110	I/O	ST	
RD3	51	78	A53	111	I/O	ST	
RD4	52	81	A56	118	I/O	ST	
RD5	53	82	B46	119	I/O	ST	
RD6	—	—	A57	120	I/O	ST	
RD7	—	—	B47	121	I/O	ST	
RD9	43	68	B38	97	I/O	ST	
RD10	44	69	A46	98	I/O	ST	
RD11	45	70	B39	99	I/O	ST	
RD12	—	79	B43	112	I/O	ST	
RD13	—	80	A54	113	I/O	ST	
RD14	—	47	B27	69	I/O	ST	
RD15	—	48	A32	70	I/O	ST	
PORTE							
RE0	58	91	B52	135	I/O	ST	PORTE is a bidirectional I/O port
RE1	61	94	A64	138	I/O	ST	
RE2	62	98	A66	142	I/O	ST	
RE3	63	99	B56	143	I/O	ST	
RE4	64	100	A67	144	I/O	ST	
RE5	1	3	A3	3	I/O	ST	
RE6	2	4	B2	4	I/O	ST	
RE7	3	5	A4	5	I/O	ST	
RE8	—	18	B10	23	I/O	ST	
RE9	—	19	A12	24	I/O	ST	
PORTF							
RF0	56	85	A59	124	I/O	ST	PORTF is a bidirectional I/O port
RF1	57	86	B49	125	I/O	ST	
RF2	—	57	B31	79	I/O	ST	
RF3	38	56	A38	78	I/O	ST	
RF4	41	64	B36	90	I/O	ST	
RF5	42	65	A44	91	I/O	ST	
RF8	—	58	A39	80	I/O	ST	
RF12	—	40	B22	58	I/O	ST	
RF13	—	39	A26	57	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION (CONTINUED)

Interrupt Source[1]	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Data 19[2]	_ADC_DATA19_VECTOR	78	OFF078<17:1>	IFS2<14>	IEC2<14>	IPC19<20:18>	IPC19<17:16>	Yes
ADC Data 20[2]	_ADC_DATA20_VECTOR	79	OFF079<17:1>	IFS2<15>	IEC2<15>	IPC19<28:26>	IPC19<25:24>	Yes
ADC Data 21[2]	_ADC_DATA21_VECTOR	80	OFF080<17:1>	IFS2<16>	IEC2<16>	IPC20<4:2>	IPC20<1:0>	Yes
ADC Data 22[2]	_ADC_DATA22_VECTOR	81	OFF081<17:1>	IFS2<17>	IEC2<17>	IPC20<12:10>	IPC20<9:8>	Yes
ADC Data 23[2]	_ADC_DATA23_VECTOR	82	OFF082<17:1>	IFS2<18>	IEC2<18>	IPC20<20:18>	IPC20<17:16>	Yes
ADC Data 24[2]	_ADC_DATA24_VECTOR	83	OFF083<17:1>	IFS2<19>	IEC2<19>	IPC20<28:26>	IPC20<25:24>	Yes
ADC Data 25[2]	_ADC_DATA25_VECTOR	84	OFF084<17:1>	IFS2<20>	IEC2<20>	IPC21<4:2>	IPC21<1:0>	Yes
ADC Data 26[2]	_ADC_DATA26_VECTOR	85	OFF085<17:1>	IFS2<21>	IEC2<21>	IPC21<12:10>	IPC21<9:8>	Yes
ADC Data 27[2]	_ADC_DATA27_VECTOR	86	OFF086<17:1>	IFS2<22>	IEC2<22>	IPC21<20:18>	IPC21<17:16>	Yes
ADC Data 28[2]	_ADC_DATA28_VECTOR	87	OFF087<17:1>	IFS2<23>	IEC2<23>	IPC21<28:26>	IPC21<25:24>	Yes
ADC Data 29[2]	_ADC_DATA29_VECTOR	88	OFF088<17:1>	IFS2<24>	IEC2<24>	IPC22<4:2>	IPC22<1:0>	Yes
ADC Data 30[2]	_ADC_DATA30_VECTOR	89	OFF089<17:1>	IFS2<25>	IEC2<25>	IPC22<12:10>	IPC22<9:8>	Yes
ADC Data 31[2]	_ADC_DATA31_VECTOR	90	OFF090<17:1>	IFS2<26>	IEC2<26>	IPC22<20:18>	IPC22<17:16>	Yes
ADC Data 32[2]	_ADC_DATA32_VECTOR	91	OFF091<17:1>	IFS2<27>	IEC2<27>	IPC22<28:26>	IPC22<25:24>	Yes
ADC Data 33[2]	_ADC_DATA33_VECTOR	92	OFF092<17:1>	IFS2<28>	IEC2<28>	IPC23<4:2>	IPC23<1:0>	Yes
ADC Data 34[2]	_ADC_DATA34_VECTOR	93	OFF093<17:1>	IFS2<29>	IEC2<29>	IPC23<12:10>	IPC23<9:8>	Yes
ADC Data 35[2,3]	_ADC_DATA35_VECTOR	94	OFF094<17:1>	IFS2<30>	IEC2<30>	IPC23<20:18>	IPC23<17:16>	Yes
ADC Data 36[2,3]	_ADC_DATA36_VECTOR	95	OFF095<17:1>	IFS2<31>	IEC2<31>	IPC23<28:26>	IPC23<25:24>	Yes
ADC Data 37[2,3]	_ADC_DATA37_VECTOR	96	OFF096<17:1>	IFS3<0>	IEC3<0>	IPC24<4:2>	IPC24<1:0>	Yes
ADC Data 38[2,3]	_ADC_DATA38_VECTOR	97	OFF097<17:1>	IFS3<1>	IEC3<1>	IPC24<12:10>	IPC24<9:8>	Yes
ADC Data 39[2,3]	_ADC_DATA39_VECTOR	98	OFF098<17:1>	IFS3<2>	IEC3<2>	IPC24<20:18>	IPC24<17:16>	Yes
ADC Data 40[2,3]	_ADC_DATA40_VECTOR	99	OFF099<17:1>	IFS3<3>	IEC3<3>	IPC24<28:26>	IPC24<25:24>	Yes
ADC Data 41[2,3]	_ADC_DATA41_VECTOR	100	OFF100<17:1>	IFS3<4>	IEC3<4>	IPC25<4:2>	IPC25<1:0>	Yes
ADC Data 42[2,3]	_ADC_DATA42_VECTOR	101	OFF101<17:1>	IFS3<5>	IEC3<5>	IPC25<12:10>	IPC25<9:8>	Yes
ADC Data 43	_ADC_DATA43_VECTOR	102	OFF102<17:1>	IFS3<6>	IEC3<6>	IPC25<20:18>	IPC25<17:16>	Yes
ADC Data 44	_ADC_DATA44_VECTOR	103	OFF103<17:1>	IFS3<7>	IEC3<7>	IPC25<28:26>	IPC25<25:24>	Yes
Core Performance Counter Interrupt	_CORE_PERF_COUNT_VECTOR	104	OFF104<17:1>	IFS3<8>	IEC3<8>	IPC26<4:2>	IPC26<1:0>	No
Core Fast Debug Channel Interrupt	_CORE_FAST_DEBUG_CHAN_VECTOR	105	OFF105<17:1>	IFS3<9>	IEC3<9>	IPC26<12:10>	IPC26<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MZ EF Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

4: This interrupt source is not available on 124-pin devices.

TABLE 8-2: OSCILLATOR CONFIGURATION REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets(2)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1360	PB7DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8800
1370	PB8DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
13C0	SLEWCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	SYSDIV<3:0>				0000
		15:0	—	—	—	—	—	SLWDIV<2:0>			—	—	—	—	—	UPEN	DNEN	BUSY	0204
13D0	CLKSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	LPRC RDY	SOSC RDY	—	POSC RDY	SPLL DIVRDY	FRCRDY	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

REGISTER 11-1: USBCSR0: USB CONTROL STATUS REGISTER 0 (CONTINUED)

bit 10 **RESUME:** Resume from Suspend control bit
1 = Generate Resume signaling when the device is in Suspend mode
0 = Stop Resume signaling

In *Device mode*, the software should clear this bit after 10 ms (a maximum of 15 ms) to end Resume signaling. In *Host mode*, the software should clear this bit after 20 ms.

bit 9 **SUSPMODE:** Suspend Mode status bit
1 = The USB module is in Suspend mode
0 = The USB module is in Normal operations

This bit is read-only in Device mode. In Host mode, it can be set by software, and is cleared by hardware.

bit 8 **SUSPEN:** Suspend Mode Enable bit
1 = Suspend mode is enabled
0 = Suspend mode is not enabled

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **FUNC<6:0>:** Device Function Address bits

These bits are only available in *Device mode*. This field is written with the address received through a SET_ADDRESS command, which will then be used for decoding the function address in subsequent token packets.

REGISTER 11-3: USBCSR2: USB CONTROL STATUS REGISTER 2 (CONTINUED)

bit 19 **SOFIF:** Start of Frame Interrupt bit
1 = A new frame has started
0 = No start of frame detected

bit 18 **RESETIF:** Reset/Babble Interrupt bit
1 = In *Host mode*, indicates babble is detected. In *Device mode*, indicates reset signaling is detected on the bus.
0 = No reset/babble detected

bit 17 **RESUMEIF:** Resume Interrupt bit
1 = Resume signaling is detected on the bus while USB module is in Suspend mode
0 = No Resume signaling detected

bit 16 **SUSPIF:** Suspend Interrupt bit
1 = Suspend signaling is detected on the bus *(Device mode)*
0 = No suspend signaling detected

bit 15-8 **Unimplemented:** Read as '0'

bit 7-1 **EP7RXIE:EP1RXIE:** Endpoint 'n' Receive Interrupt Enable bit
1 = Receive interrupt is enabled for this endpoint
0 = Receive interrupt is not enabled

bit 0 **Unimplemented:** Read as '0'

TABLE 12-16: PORTG REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	ANSELG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSG9	ANSG8	ANSG7	ANSG6	—	—	—	—	—	—	03C0
0610	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	—	—	03C0
0620	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RG9	RG8	RG7	RG6	—	—	—	—	—	—	xxxx
0630	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	—	—	xxxx
0640	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	—	—	0000
0650	CNPUG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	—	—	0000
0660	CNPDG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	—	—	0000
0670	CNCONG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0680	CNENG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNENG9	CNENG8	CNENG7	CNENG6	—	—	—	—	—	—	0000
0690	CNSTATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CN STATG9	CN STATG8	CN STATG7	CN STATG6	—	—	—	—	—	—	0000
06A0	CNNEG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNNEG9	CNNEG8	CNNEG7	CNNEG6	—	—	—	—	—	—	0000
06B0	CNFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNFG9	CNFG8	CNFG7	CNFG6	—	—	—	—	—	—	0000
06C0	SRCON0G	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	SR0G9	—	—	SR0G6	—	—	—	—	—	—	0000
06D0	SRCON1G	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	SR1G9	—	—	SR1G6	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

NOTES:

REGISTER 20-20: SQI1BDRXDSTAT: SQI BUFFER DESCRIPTOR DMA RECEIVE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-x	R-x	R-x	R-x	U-0
	—	—	—	RXSTATE<3:0>				—
23:16	U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
	—	—	—	RXBUFCNT<4:0>				
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RXCURBUFLEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-25 **RXSTATE<3:0>:** Current DMA Receive State Status bits
These bits provide information on the current DMA receive states.

bit 24-21 **Unimplemented:** Read as '0'

bit 20-16 **RXBUFCNT<4:0>:** DMA Buffer Byte Count Status bits
These bits provide information on the internal FIFO space.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **RXCURBUFLEN<7:0>:** Current DMA Receive Buffer Length Status bits
These bits provide the length of the current DMA receive buffer.

REGISTER 20-21: SQI1THR: SQI THRESHOLD CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	THRES<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-5 **Unimplemented:** Read as '0'

bit 4-0 **THRES<4:0>:** SQI Control Threshold Value bits
The SQI control threshold interrupt is asserted when the amount of space indicated by THRES<4:0> is available in the SQI control buffer.

REGISTER 20-26: SQI1XCON4: SQI XIP CONTROL REGISTER 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INIT2SCHECK	INIT2COUNT<1:0>		INIT2TYPE<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT2CMD3<7:0>(1)							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT2CMD2<7:0>(1)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT2CMD1<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **INIT2SCHECK:** Flash Initialization 2 Command Status Check bit
1 = Check the status after executing the INIT2 command
0 = Do not check the status

bit 27-26 **INIT2COUNT<1:0>:** Flash Initialization 2 Command Count bits
11 = INIT2CMD1, INIT2CMD2, and INIT2CMD3 are sent
10 = INIT2CMD1 and INIT2CMD2 are sent, but INIT2CMD3 is still pending
01 = INIT2CMD1 is sent, but INIT2CMD2 and INIT2CMD3 are still pending
00 = No commands are sent

bit 25-24 **INIT2TYPE<1:0>:** Flash Initialization 2 Command Type bits
11 = Reserved
10 = INIT2 commands are sent in Quad Lane mode
01 = INIT2 commands are sent in Dual Lane mode
00 = INIT2 commands are sent in Single Lane mode

bit 24-16 **INIT2CMD3<7:0>:** Flash Initialization Command 3 bits(1)
Third command of the Flash initialization.

bit 15-8 **INIT2CMD2<7:0>:** Flash Initialization Command 2 bits(1)
Second command of the Flash initialization.

bit 7-0 **INIT2CMD1<7:0>:** Flash Initialization Command 1 bits(1)
First command of the Flash initialization.

Note 1: INIT2CMD1 can be WEN and INIT2CMD2 can be SECTOR UNPROTECT.

Note: Some Flash devices require Write Enable and Sector Unprotect commands before read/write operations and this register is useful in working with those Flash types (XIP mode only)

Figure 26-10: Format of SA_CTRL (Continued)

bit 16-10 **ALGO<6:0>:** Type of Algorithm to Use
1xxxxxx = HMAC 1
x1xxxxx = SHA-256
xx1xxxx = SHA1
xxx1xxx = MD5
xxxx1xx = AES
xxxxx1x = TDES
xxxxxx1 = DES

bit 9 **ENC:** Type of Encryption Setting
1 = Encryption
0 = Decryption

bit 8-7 **KEYSIZE<1:0>:** Size of Keys in SA_AUTHKEYx or SA_ENCKEYx
11 = Reserved; do not use
10 = 256 bits
01 = 192 bits
00 = 128 bits(1)

bit 6-4 **MULTITASK<2:0>:** How to Combine Parallel Operations in the Crypto Engine
111 = Parallel pass (decrypt and authenticate incoming data in parallel)
101 = Pipe pass (encrypt the incoming data, and then perform authentication on the encrypted data)
011 = Reserved
010 = Reserved
001 = Reserved
000 = Encryption or authentication or decryption (no pass)

bit 3-0 **CRYPTOALGO<3:0>:** Mode of operation for the Crypto Algorithm
1111 = Reserved
1110 = AES_GCM (for AES processing)
1101 = RCTR (for AES processing)
1100 = RCBC_MAC (for AES processing)
1011 = ROFB (for AES processing)
1010 = RCFB (for AES processing)
1001 = RCBC (for AES processing)
1000 = RECB (for AES processing)
0111 = TOFB (for Triple-DES processing)
0110 = TCFB (for Triple-DES processing)
0101 = TCBC (for Triple-DES processing)
0100 = TECB (for Triple-DES processing)
0011 = OFB (for DES processing)
0010 = CFB (for DES processing)
0001 = CBC (for DES processing)
0000 = ECB (for DES processing)

Note 1: This setting does not alter the size of SA_AUTHKEYx or SA_ENCKEYx in the Security Association, only the number of bits of SA_AUTHKEYx and SA_ENCKEYx that are used.

REGISTER 27-1: RNGVER: RANDOM NUMBER GENERATOR VERSION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<15:8>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<7:0>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERSION<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	REVISION<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **ID<15:0>:** Block Identification bits

bit 15-8 **VERSION<7:0>:** Block Version bits

bit 7-0 **REVISION<7:0>:** Block Revision bits

REGISTER 28-28: ADCEIEN1: ADC EARLY INTERRUPT ENABLE REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN31(1)	EIEN30(1)	EIEN29(1)	EIEN28(1)	EIEN27(1)	EIEN26(1)	EIEN25(1)	EIEN24(1)
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN23(1)	EIEN22(1)	EIEN21(1)	EIEN20(1)	EIEN19(1)	EIEN18	EIEN17	EIEN16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN15	EIEN14	EIEN13	EIEN12	EIEN11	EIEN10	EIEN9	EIEN8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN7	EIEN6	EIEN5	EIEN4	EIEN3	EIEN2	EIEN1	EIEN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **EIEN31:EIEN0:** Early Interrupt Enable for Analog Input bits

1 = Early Interrupts are enabled for the selected analog input. The interrupt is generated after the early interrupt event occurs (indicated by the EIRDYx bit ('x' = 31-0) of the ADCEISTAT1 register)

0 = Interrupts are disabled

Note 1: This bit is not available on 64-pin devices.

REGISTER 28-29: ADCEIEN2: ADC EARLY INTERRUPT ENABLE REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	EIEN44(2)	EIEN43(2)	EIEN42(2)	EIEN41(2)	EIEN40(2)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN39(2)	EIEN38(2)	EIEN37(2)	EIEN36(2)	EIEN35(2)	EIEN34(1)	EIEN33(1)	EIEN32(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-0 **EIEN44:EIEN32:** Early Interrupt Enable for Analog Input bits

1 = Early Interrupts are enabled for the selected analog input. The interrupt is generated after the early interrupt event occurs (indicated by the EIRDYx bit ('x' = 44-32) of the ADCEISTAT2 register)

0 = Interrupts are disabled

Note 1: This bit is not available on 64-pin devices.

2: This bit is not available on 64-pin and 100-pin devices.

REGISTER 29-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER (CONTINUED)

bit 10-8 **PRSEG<2:0>:** Propagation Time Segment bits(4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 7-6 **SJW<1:0>:** Synchronization Jump Width bits(3)
11 = Length is 4 x TQ
10 = Length is 3 x TQ
01 = Length is 2 x TQ
00 = Length is 1 x TQ

bit 5-0 **BRP<5:0>:** Baud Rate Prescaler bits
111111 = TQ = (2 x 64)/TPBCLK5
111110 = TQ = (2 x 63)/TPBCLK5
•
•
•
000001 = TQ = (2 x 2)/TPBCLK5
000000 = TQ = (2 x 1)/TPBCLK5

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
2: 3 Time bit sampling is not allowed for BRP < 2.
3: SJW ≤ SEG2PH.
4: The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

REGISTER 30-1: ETHCON1: ETHERNET CONTROLLER CONTROL REGISTER 1 (CONTINUED)

bit 7 **AUTOFC:** Automatic Flow Control bit

1 = Automatic Flow Control enabled
0 = Automatic Flow Control disabled

Setting this bit will enable automatic Flow Control. If set, the full and empty watermarks are used to automatically enable and disable the Flow Control, respectively. When the number of received buffers BUFCNT (ETHSTAT<16:23>) rises to the full watermark, Flow Control is automatically enabled. When the BUFCNT falls to the empty watermark, Flow Control is automatically disabled.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **MANFC:** Manual Flow Control bit

1 = Manual Flow Control is enabled
0 = Manual Flow Control is disabled

Setting this bit will enable manual Flow Control. If set, the Flow Control logic will send a PAUSE frame using the PAUSE timer value in the PTV register. It will then resend a PAUSE frame every 128 * PTV<15:0>/2 TX clock cycles until the bit is cleared.

Note: For 10 Mbps operation, TX clock runs at 2.5 MHz. For 100 Mbps operation, TX clock runs at 25 MHz.

When this bit is cleared, the Flow Control logic will automatically send a PAUSE frame with a 0x0000 PAUSE timer value to disable Flow Control.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **BUFCDEC:** Descriptor Buffer Count Decrement bit

The BUFCDEC bit is a write-1 bit that reads as '0'. When written with a '1', the Descriptor Buffer Counter, BUFCNT, will decrement by one. If BUFCNT is incremented by the RX logic at the same time that this bit is written, the BUFCNT value will remain unchanged. Writing a '0' will have no effect.

This bit is only used for RX operations.

Note 1: It is not recommended to clear the RXEN bit and then make changes to any RX related field/register. The Ethernet Controller must be reinitialized (ON cleared to '0'), and then the RX changes applied.

REGISTER 30-2: ETHCON2: ETHERNET CONTROLLER CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RXBUFSZ<6:4>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	RXBUFSZ<3:0>				—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-4 **RXBUFSZ<6:0>:** RX Data Buffer Size for All RX Descriptors (in 16-byte increments) bits

1111111 = RX data Buffer size for descriptors is 2032 bytes
•
•
•
1100000 = RX data Buffer size for descriptors is 1536 bytes
•
•
•
0000011 = RX data Buffer size for descriptors is 48 bytes
0000010 = RX data Buffer size for descriptors is 32 bytes
0000001 = RX data Buffer size for descriptors is 16 bytes
0000000 = Reserved

bit 3-0 **Unimplemented:** Read as '0'

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

TABLE 37-18: SYSTEM TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
OS51	FSYS	System Frequency	DC	—	200	MHz	USB module disabled
			60	—	200	MHz	USB module enabled
OS55a	FPB	Peripheral Bus Frequency	DC	—	100	MHz	For PBCLKx, 'x' ≠ 4, 7
OS55b			DC	—	200	MHz	For PBCLK4, PBCLK7
OS56	FREF	Reference Clock Frequency	—	—	50	MHz	For REFCLKI1, 3, 4 and REFCLKO1, 3, 4 pins

TABLE 37-19: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
OS50	FIN	PLL Input Frequency Range	5	—	64	MHz	ECPLL, HSPLL, FRCPLL modes
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	100	µs	—
OS53	DCLK	CLKO Stability(2) (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period
OS54	FVCO	PLL VCO Frequency Range	350	—	700	MHz	—
OS54a	FPLL	PLL Output Frequency Range	10	—	200	MHz	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{PBCLK2}{CommunicationClock}}}$$

For example, if PBCLK2 = 100 MHz and SPI bit rate = 50 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{100}{50}}} = \frac{D_{CLK}}{1.41}$$

APPENDIX A: MIGRATING FROM PIC32MX5XX/6XX/7XX TO PIC32MZ EF

This appendix provides an overview of considerations for migrating from PIC32MX5XX/6XX/7XX devices to the PIC32MZ EF family of devices. The code developed for PIC32MX5XX/6XX/7XX devices can be ported to PIC32MZ EF devices after making the appropriate changes outlined in the following sections.

The PIC32MZ EF devices are based on a new architecture, and feature many improvements and new capabilities over PIC32MX5XX/6XX/7XX devices.

A.1 Oscillator and PLL Configuration

Because the maximum speed of the PIC32MZ EF family is greater, the configuration of the oscillator is different from prior PIC32MX5XX/6XX/7XX devices.

Table A-1 summarizes the differences (indicated by **Bold** type) between the family devices for the oscillator.

TABLE A-1: OSCILLATOR CONFIGURATION DIFFERENCES

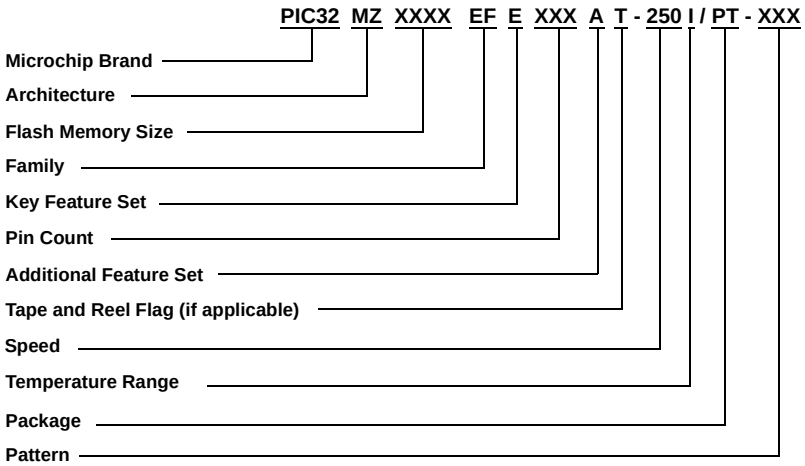
PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Primary Oscillator Configuration	
On PIC32MX devices, XT mode had to be selected if the input frequency was in the 3 MHz to 10 MHz range (4-10 for PLL), and HS mode had to be selected if the input frequency was in the 10 MHz to 20 MHz range.	On PIC32MZ EF devices, HS mode has a wider input frequency range (4 MHz to 12 MHz). The bit setting of '01' is Reserved.
POSCMOD<1:0> (DEVCFG1<9:8>) 11 = Primary Oscillator disabled 10 = HS Oscillator mode selected **01 = XT Oscillator mode selected** 00 = External Clock mode selected	POSCMOD<1:0> (DEVCFG1<9:8>) 11 = Primary Oscillator disabled 10 = HS Oscillator mode selected **01 = Reserved** 00 = External Clock mode selected
On PIC32MX devices, crystal mode could be selected with the HS or XT POSC setting, but an external oscillator could be fed into the OSC1/CLKI pin and the part would operate normally.	On PIC32MZ devices, this option is not available. External oscillator signals should only be fed into the OSC1/CLKI pin with the POSC set to EC mode.
Oscillator Selection	
On PIC32MX devices, clock selection choices are as follows:	On PIC32MZ EF devices, clock selection choices are as follows:
FNOSC<2:0> (DEVCFG1<2:0>) NOSC<2:0> (OSCCON<10:8>) 111 = FRCDIV **110 = FRCDIV16** 101 = LPRC 100 = SOSC **011 = POSC with PLL module** 010 = POSC (XT, HS, EC) **001 = FRCDIV+PLL** **000 = FRC**	FNOSC<2:0> (DEVCFG1<2:0>) NOSC<2:0> (OSCCON<10:8>) 111 = FRCDIV **110 = Reserved** 101 = LPRC 100 = SOSC **011 = Reserved** 010 = POSC (HS or EC) **001 = System PLL (SPLL)** **000 = FRCDIV**
COSC<2:0> (OSCCON<14:12>) 111 = FRC divided by FRCDIV **110 = FRC divided by 16** 101 = LPRC 100 = SOSC **011 = POSC + PLL module** 010 = POSC **001 = FRCPLL** **000 = FRC**	COSC<2:0> (OSCCON<14:12>) 111 = FRC divided by FRCDIV **110 = BFRC** 101 = LPRC 100 = SOSC **011 = Reserved** 010 = POSC **001 = System PLL** **000 = FRC divided by FRCDIV**

TABLE A-1: OSCILLATOR CONFIGURATION DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Secondary Oscillator Enable	
FSOSCEN (DEVCFG1<**5**>)	The location of the SOSCEN bit in the Flash Configuration Words has moved. FSOSCEN (DEVCFG1<**6**>)
PLL Configuration	
The FNOSC<2:0> and NOSC<2:0> bits select between POSC and FRC. **FNOSC<2:0> (DEVCFG1<2:0>)** **NOSC<2:0> (OSCCON<10:8>)**	Selection of which input clock (POSC or FRC) is now done through the FPLLICLK/PLLICLK bits. **FPLLICLK (DEVCFG2<7>)** **PLLICLK (SPLLCON<7>)**
On PIC32MX devices, the input frequency to the PLL had to be between 4 MHz and 5 MHz. FPLLIDIV selected how to divide the input frequency to give it the appropriate range. FPLLIDIV<2:0> (DEVCFG2<2:0>) **111 = 12x divider** **110 = 10x divider** 101 = 6x divider 100 = 5x divider 011 = 4x divider 010 = 3x divider 001 = 2x divider 000 = 1x divider	On PIC32MZ EF devices, the input range for the PLL is wider (5 MHz to 64 MHz). The input divider values have changed, and new FPLLRNG/PLLRNG bits have been added to indicate under what range the input frequency falls. FPLLIDIV<2:0> (DEVCFG2<2:0>) **PLLIDIV<2:0> (SPLLCON<2:0>)** **111 = Divide by 8** **110 = Divide by 7** 101 = Divide by 6 100 = Divide by 5 011 = Divide by 4 010 = Divide by 3 001 = Divide by 2 000 = Divide by 1 **FPLLRNG<2:0> (DEVCFG2<6:4>)** **PLLRNG<2:0> (SPLLCON<2:0>)** **111 = Reserved** **110 = Reserved** **101 = 34-64 MHz** **100 = 21-42 MHz** **011 = 13-26 MHz** **010 = 8-16 MHz** **001 = 5-10 MHz** **000 = Bypass**
On PIC32MX devices, the output frequency of PLL is between 60 MHz and 120 MHz. The PLL multiplier and divider bits configure the PLL for this range. FPLLMUL<**2**:0> (DEVCFG2<**6:4**>) PLLMULT<**2**:0> (OSCCON<18:16>) **111 = 24x multiplier** **110 = 21x multiplier** **101 = 20x multiplier** **100 = 19x multiplier** **011 = 18x multiplier** **010 = 17x multiplier** **001 = 16x multiplier** **000 = 15x multiplier** FPLLODIV<2:0> (DEVCFG2<18:16>) PLLODIV<2:0> (OSCCON<29:27>) **111 = 24x multiplier** **110 = 21x multiplier** **101 = 20x multiplier** **100 = 19x multiplier** **011 = 18x multiplier** **010 = 17x multiplier** **001 = 16x multiplier** **000 = 15x multiplier**	The PLL multiplier and divider on PIC32MZ EF devices have a wider range to accommodate the wider PLL specification range. FPLLMUL**T**<**6**:0> (DEVCFG2<**14:8**>) PLLMULT<**6**:0> (**SPLLCON<22:16>**) **1111111 = Multiply by 128** **1111110 = Multiply by 127** **1111101 = Multiply by 126** **1111100 = Multiply by 125** • • • **0000000 = Multiply by 1** FPLLODIV<2:0> (DEVCFG2<18:16>) PLLODIV<2:0> (**SPLLCON<26:24>**) **111 = PLL Divide by 32** **110 = PLL Divide by 32** **101 = PLL Divide by 32** **100 = PLL Divide by 16** **011 = PLL Divide by 8** **010 = PLL Divide by 4** **001 = PLL Divide by 2** **000 = PLL Divide by 2**

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Example:

PIC32MZ2048EFH144-I/PT:
Embedded Connectivity PIC32,
MIPS32® M-Class MPU core,
2048 KB program memory,
144-pin, with Floating Point Unit,
Industrial temperature, TQFP package.

Flash Memory Family

Architecture	MZ	= MIPS32® M-Class MPU Core
Flash Memory Size	0512	= 512 KB
	1024	= 1024 KB
	2048	= 2048 KB
Family	EF	= Embedded Connectivity Microcontroller Family with Floating Point Unit
Key Feature	E	= PIC32 EF Family Features (no CAN, no Crypto)
	F	= PIC32 EF Family Features (CAN, no Crypto)
	G	= PIC32 EF Family Features (no CAN, no Crypto)
	H	= PIC32 EF Family Features (CAN, no Crypto)
	K	= PIC32 EF Family Features (Crypto and CAN)
	M	= PIC32 EF Family Features (Crypto and CAN)
Pin Count	064	= 64-pin
	100	= 100-pin
	124	= 124-pin
	144	= 144-pin
Speed	Blank	= Up to 200 MHz
	250	= Up to 252 MHz
Temperature Range	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Extended)
Package	MR	= 64-Lead (9x9x0.9 mm) QFN (Plastic Quad Flatpack)
	PT	= 64-Lead (10x10x1 mm) TQFP (Thin Quad Flatpack)
	PT	= 100-Lead (12x12x1 mm) TQFP (Thin Quad Flatpack)
	PF	= 100-Lead (14x14x1 mm) TQFP (Thin Quad Flatpack)
	TL	= 124-Lead (9x9x0.9 mm) VTLA (Very Thin Leadless Array)
	PH	= 144-Lead (16x16x1 mm) TQFP (Thin Quad Flatpack)
	PL	= 144-Lead (20x20x1.40 mm) LQFP (Low Profile Quad Flatpack)
Pattern		Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise)
	ES	= Engineering Sample