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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	97
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efg124t-i-tl

2.9 Designing for High-Speed Peripherals

The PIC32MZ EF family devices have peripherals that operate at frequencies much higher than typical for an embedded environment. Table 2-1 lists the peripherals that produce high-speed signals on their external pins:

TABLE 2-1: PERIPHERALS THAT PRODUCE HS SIGNALS ON EXTERNAL PINS

Peripheral	High-Speed Signal Pins	Maximum Speed on Signal Pin
EBI	EBIAx, EBIDx	50 MHz
SQI1	SQICLK, SQICSt, SQIDx	50 MHz
HS USB	D+, D-	480 MHz

Due to these high-speed signals, it is important to consider several factors when designing a product that uses these peripherals, as well as the PCB on which these components will be placed. Adhering to these recommendations will help achieve the following goals:

- Minimize the effects of electromagnetic interference to the proper operation of the product
- Ensure signals arrive at their intended destination at the same time
- Minimize crosstalk
- Maintain signal integrity
- Reduce system noise
- Minimize ground bounce and power sag

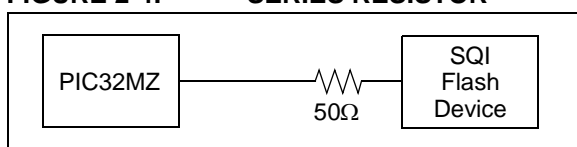
2.9.1 SYSTEM DESIGN

2.9.1.1 Impedance Matching

When selecting parts to place on high-speed buses, particularly the SQI bus, if the impedance of the peripheral device does not match the impedance of the pins on the PIC32MZ EF device to which it is connected, signal reflections could result, thereby degrading the quality of the signal.

If it is not possible to select a product that matches impedance, place a series resistor at the load to create the matching impedance. See Figure 2-4 for an example.

FIGURE 2-4: SERIES RESISTOR



2.9.1.2 PCB Layout Recommendations

The following list contains recommendations that will help ensure the PCB layout will promote the goals previously listed.

• Component Placement

- Place bypass capacitors as close to their component power and ground pins as possible, and place them on the same side of the PCB
- Devices on the same bus that have larger setup times should be placed closer to the PIC32MZ EF device

• Power and Ground

- Multi-layer PCBs will allow separate power and ground planes
- Each ground pin should be connected to the ground plane individually
- Place bypass capacitor vias as close to the pad as possible (preferably inside the pad)
- If power and ground planes are not used, maximize width for power and ground traces
- Use low-ESR, surface-mount bypass capacitors

• Clocks and Oscillators

- Place crystals as close as possible to the PIC32MZ EF device OSC/SOSC pins
- Do not route high-speed signals near the clock or oscillator
- Avoid via usage and branches in clock lines (SQICLK)
- Place termination resistors at the end of clock lines

• Traces

- Higher-priority signals should have the shortest traces
- Match trace lengths for parallel buses (EBIAx, EBIDx, SQIDx)
- Avoid long run lengths on parallel traces to reduce coupling
- Make the clock traces as straight as possible
- Use rounded turns rather than right-angle turns
- Have traces on different layers intersect on right angles to minimize crosstalk
- Maximize the distance between traces, preferably no less than three times the trace width
- Power traces should be as short and as wide as possible
- High-speed traces should be placed close to the ground plane

TABLE 4-17: SYSTEM BUS TARGET 9 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
A420	SBT9ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>				0000
A424	SBT9ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>			0000
A428	SBT9ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
A430	SBT9ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A438	SBT9ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A440	SBT9REG0	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
A450	SBT9RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A458	SBT9WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A460	SBT9REG1	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
A470	SBT9RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A478	SBT9WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
15B0	DCH7ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
15C0	DCH7INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
15D0	DCH7SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
15E0	DCH7DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
15F0	DCH7SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1600	DCH7DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1610	DCH7SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1620	DCH7DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1630	DCH7CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1640	DCH7CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1650	DCH7DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 11-3: USBCSR2: USB CONTROL STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 VBUSERRIE	R/W-0 SESSRQIE	R/W-0 DISCONIE	R/W-0 CONNIE	R/W-0 SOFIE	R/W-1 RESETIE	R/W-1 RESUMEIE	R/W-0 SUSPIE
23:16	R-0, HS VBUSERRIF	R-0, HS SESSRQIF	R-0, HS DISCONIF	R-0, HS CONNIF	R-0, HS SOFIF	R-0, HS RESETIF	R-0, HS RESUMEIF	R-0, HS SUSPIF
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	R/W-1 EP7RXIE	R/W-1 EP6RXIE	R/W-1 EP5RXIE	R/W-1 EP4RXIE	R/W-1 EP3RXIE	R/W-1 EP2RXIE	R/W-1 EP1RXIE	U-0 —

Legend:

R = Readable bit

-n = Value at POR

HS = Hardware Set

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

- bit 31 **VBUSERRIE:** VBUS Error Interrupt Enable bit
1 = VBUS error interrupt is enabled
0 = VBUS error interrupt is disabled
- bit 30 **SESSRQIE:** Session Request Interrupt Enable bit
1 = Session request interrupt is enabled
0 = Session request interrupt is disabled
- bit 29 **DISCONIE:** Device Disconnect Interrupt Enable bit
1 = Device disconnect interrupt is enabled
0 = Device disconnect interrupt is disabled
- bit 28 **CONNIE:** Device Connection Interrupt Enable bit
1 = Device connection interrupt is enabled
0 = Device connection interrupt is disabled
- bit 27 **SOFIE:** Start of Frame Interrupt Enable bit
1 = Start of Frame event interrupt is enabled
0 = Start of Frame event interrupt is disabled
- bit 26 **RESETIE:** Reset/Babble Interrupt Enable bit
1 = Interrupt when reset (*Device mode*) or Babble (*Host mode*) is enabled
0 = Reset/Babble interrupt is disabled
- bit 25 **RESUMEIE:** Resume Interrupt Enable bit
1 = Resume signaling interrupt is enabled
0 = Resume signaling interrupt is disabled
- bit 24 **SUSPIE:** Suspend Interrupt Enable bit
1 = Suspend signaling interrupt is enabled
0 = Suspend signaling interrupt is disabled
- bit 23 **VBUSERRIF:** VBUS Error Interrupt bit
1 = VBUS has dropped below the VBUS valid threshold during a session
0 = No interrupt
- bit 22 **SESSRQIF:** Session Request Interrupt bit
1 = Session request signaling has been detected
0 = No session request detected
- bit 21 **DISCONIF:** Device Disconnect Interrupt bit
1 = In *Host mode*, indicates when a device disconnect is detected. In *Device mode*, indicates when a session ends.
0 = No device disconnect detected
- bit 20 **CONNIF:** Device Connection Interrupt bit
1 = In *Host mode*, indicates when a device connection is detected
0 = No device connection detected

REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER (CONTINUED)

bit 19-16 **TXFIFOSZ<3:0>**: TX Endpoint FIFO packet size bits

The maximum packet size to allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)

1111 = Reserved

•
•
•

1010 = Reserved

1001 = 4096 bytes

1000 = 2048 bytes

0111 = 1024 bytes

0110 = 512 bytes

0101 = 256 bytes

0100 = 128 bytes

0011 = 64 bytes

0010 = 32 bytes

0001 = 16 bytes

0000 = 8 bytes

bit 15-10 **Unimplemented**: Read as '0'

bit 9 **TXEDMA**: TX Endpoint DMA Assertion Control bit

1 = DMA_REQ signal for all IN endpoints will be deasserted when MAXP-8 bytes have been written to an endpoint. This is Early mode.

0 = DMA_REQ signal for all IN endpoints will be deasserted when MAXP bytes have been written to an endpoint. This is Late mode.

bit 8 **RXEDMA**: RX Endpoint DMA Assertion Control bit

1 = DMA_REQ signal for all OUT endpoints will be deasserted when MAXP-8 bytes have been written to an endpoint. This is Early mode.

0 = DMA_REQ signal for all OUT endpoints will be deasserted when MAXP bytes have been written to an endpoint. This is Late mode.

bit 7 **BDEV**: USB Device Type bit

1 = USB is operating as a 'B' device

0 = USB is operating as an 'A' device

bit 6 **FSDEV**: Full-Speed/Hi-Speed device detection bit (*Host mode*)

1 = A Full-Speed or Hi-Speed device has been detected being connected to the port

0 = No Full-Speed or Hi-Speed device detected

bit 5 **LSDEV**: Low-Speed Device Detection bit (*Host mode*)

1 = A Low-Speed device has been detected being connected to the port

0 = No Low-Speed device detected

bit 4-3 **VBUS<1:0>**: VBUS Level Detection bits

11 = Above VBUS Valid

10 = Above AValid, below VBUS Valid

01 = Above Session End, below AValid

00 = Below Session End

bit 2 **HOSTMODE**: Host Mode bit

1 = USB module is acting as a Host

0 = USB module is not acting as a Host

bit 1 **HOSTREQ**: Host Request Control bit

'B' device only:

1 = USB module initiates the Host Negotiation when Suspend mode is entered. This bit is cleared when Host Negotiation is completed.

0 = Host Negotiation is not taking place

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 11-19: USBExRXA: USB ENDPOINT 'x' RECEIVE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXHUBPRT<6:0>							
23:16	R/W-0 MULTTRAN	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXHUBADD<6:0>							
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXFADDR<6:0>							

Legend:	HC = Hardware Cleared	HS = Hardware Set
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-24 **RXHUBPRT<6:0>:** RX Hub Port bits (*Host mode*)

When a Low-Speed or Full-Speed device is connected to this endpoint via a Hi-Speed USB 2.0 hub, this field records the port number of that USB 2.0 hub.

bit 23 **MULTTRAN:** RX Hub Multiple Translators bit (*Host mode*)

1 = The USB 2.0 hub has multiple transaction translators

0 = The USB 2.0 hub has a single transaction translator

bit 22-16 **RXHUBADD<6:0>:** RX Hub Address bits (*Host mode*)

When a Low-Speed or Full-Speed device is connected to this endpoint via a Hi-Speed USB 2.0 hub, these bits record the address of the USB 2.0 hub.

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **RXFADDR<6:0>:** RX Functional Address bits (*Host mode*)

Specifies the address for the target function that is to be accessed through the associated endpoint. It needs to be defined for each RX endpoint that is used.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 12-3: OUTPUT PIN SELECTION (CONTINUED)

RPN Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPD1	RPD1R	RPD1R<3:0>	0000 = No Connect 0001 = U1RTS 0010 = U2TX 0011 = U5RTS 0100 = U6TX 0101 = Reserved 0110 = SS2 0111 = Reserved 1000 = SDO4 1001 = Reserved 1010 = SDO6 ⁽¹⁾ 1011 = OC2 1100 = OC1 1101 = OC9 1110 = Reserved 1111 = C2TX ⁽³⁾
RPG9	RPG9R	RPG9R<3:0>	
RPB14	RPB14R	RPB14R<3:0>	
RPD0	RPD0R	RPD0R<3:0>	
RPB6	RPB6R	RPB6R<3:0>	
RPD5	RPD5R	RPD5R<3:0>	
RPB2	RPB2R	RPB2R<3:0>	
RPF3	RPF3R	RPF3R<3:0>	
RPF13 ⁽¹⁾	RPF13R ⁽¹⁾	RPF13R<3:0> ⁽¹⁾	
RPC2 ⁽¹⁾	RPC2R ⁽¹⁾	RPC2R<3:0> ⁽¹⁾	
RPE8 ⁽¹⁾	RPE8R ⁽¹⁾	RPE8R<3:0> ⁽¹⁾	
RPF2 ⁽¹⁾	RPF2R ⁽¹⁾	RPF2R<3:0> ⁽¹⁾	

Note 1: This selection is not available on 64-pin devices.

2: This selection is not available on 64-pin or 100-pin devices.

3: This selection is not available on devices without a CAN module.

TABLE 12-11: PORTE REGISTER MAP FOR 100-PIN, 124-PIN, AND 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0400	ANSELE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSE9	ANSE8	ANSE7	ANSE6	ANSE5	ANSE4	—	—	—	—	03F0
0410	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISE9	TRISE8	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	03FF
0420	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
0430	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATE9	LATE8	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
0440	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCE9	ODCE8	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000
0450	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUE9	CNPUE8	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPUE3	CNPUE2	CNPUE1	CNPUE0	0000
0460	CNPDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDE9	CNPDE8	CNPDE7	CNPDE6	CNPDE5	CNPDE4	CNPDE3	CNPDE2	CNPDE1	CNPDE0	0000
0470	CNCONOE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0480	CNENE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNENE9	CNENE8	CNENE7	CNENE6	CNENE5	CNENE4	CNENE3	CNENE2	CNENE1	CNENE0	0000
0490	CNSTATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CN STATE9	CN STATE8	CN STATE7	CN STATE6	CN STATE5	CN STATE4	CN STATE3	CN STATE2	CN STATE1	CN STATE0	0000
04A0	CNNEE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNNEE9	CNNEE8	CNNEE7	CNNEE6	CNNEE5	CNNEE4	CNNEE3	CNNEE2	CNNEE1	CNNEE0	0000
04B0	CNFE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNFE9	CNFE8	CNFE7	CNFE6	CNFE5	CNFE4	CNFE3	CNFE2	CNFE1	CNFE0	0000
04C0	SRCONOE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR0E3	SR0E2	SR0E1	SR0E0	0000
04D0	SRCON1E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR1E3	SR1E2	SR1E1	SR1E0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

14.2 Timer2-Timer9 Control Registers

TABLE 14-1: TIMER2 THROUGH TIMER9 REGISTER MAP

Virtual Address (BF84_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0210	TMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
0220	PR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>																FFFF
0400	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
0410	TMR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR3<15:0>																0000
0420	PR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR3<15:0>																FFFF
0600	T4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0610	TMR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR4<15:0>																0000
0620	PR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR4<15:0>																FFFF
0800	T5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
0810	TMR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR5<15:0>																0000
0820	PR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR5<15:0>																FFFF
0A00	T6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0A10	TMR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR6<15:0>																0000
0A20	PR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR6<15:0>																FFFF
0C00	T7CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 25-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN ^(1,2)	CHIME ⁽²⁾	PIV ⁽²⁾	ALRMSYNC	AMASK<3:0> ⁽²⁾			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARPT<7:0> ⁽²⁾							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ALRMEN:** Alarm Enable bit^(1,2)

1 = Alarm is enabled

0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit⁽²⁾

1 = Chime is enabled – ARPT<7:0> is allowed to rollover from 0x00 to 0xFF

0 = Chime is disabled – ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit⁽²⁾

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse.

When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 **ALRMSYNC:** Alarm Sync bit

1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read.

The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing.

0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is more than 32 real-time clocks away from a half-second rollover

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits⁽²⁾

0000 = Every half-second

0001 = Every second

0010 = Every 10 seconds

0011 = Every minute

0100 = Every 10 minutes

0101 = Every hour

0110 = Once a day

0111 = Once a week

1000 = Once a month

1001 = Once a year (except when configured for February 29, once every four years)

1010 = Reserved

1011 = Reserved

11xx = Reserved

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

Note: This register is reset only on a Power-on Reset (POR).

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 27-2: RNGCON: RANDOM NUMBER GENERATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	LOAD	TRNGMODE	CONT	PRNGEN	TRNGEN
7:0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
	PLEN<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12 **LOAD:** Device Select bit

This bit is self-clearing and is used to load the seed from the TRNG (i.e., the random value) as a seed to the PRNG.

bit 11 **TRNGMODE:** TRNG Mode Selection bit

1 = Use ring oscillators with bias corrector

0 = Use ring oscillators with XOR tree

Note: Enabling this bit will generate numbers with a more even distribution of randomness.

bit 10 **CONT:** PRNG Number Shift Enable bit

1 = The PRNG random number is shifted every cycle

0 = The PRNG random number is shifted when the previous value is removed

bit 9 **PRNGEN:** PRNG Operation Enable bit

1 = PRNG operation is enabled

0 = PRNG operation is not enabled

bit 8 **TRNGEN:** TRNG Operation Enable bit

1 = TRNG operation is enabled

0 = TRNG operation is not enabled

bit 7-0 **PLEN<7:0>:** PRNG Polynomial Length bits

These bits contain the length of the polynomial used for the PRNG.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 28-14: ADCCMPENx: ADC DIGITAL COMPARATOR 'x' ENABLE REGISTER
(‘x’ = 1 THROUGH 6)**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 CMPE31 ⁽¹⁾	R/W-0 CMPE30 ⁽¹⁾	R/W-0 CMPE29 ⁽¹⁾	R/W-0 CMPE28 ⁽¹⁾	R/W-0 CMPE27 ⁽¹⁾	R/W-0 CMPE26 ⁽¹⁾	R/W-0 CMPE25 ⁽¹⁾	R/W-0 CMPE24 ⁽¹⁾
23:16	R/W-0 CMPE23 ⁽¹⁾	R/W-0 CMPE22 ⁽¹⁾	R/W-0 CMPE21 ⁽¹⁾	R/W-0 CMPE20 ⁽¹⁾	R/W-0 CMPE19 ⁽¹⁾	R/W-0 CMPE18	R/W-0 CMPE17	R/W-0 CMPE16
15:8	R/W-0 CMPE15	R/W-0 CMPE14	R/W-0 CMPE13	R/W-0 CMPE12	R/W-0 CMPE11	R/W-0 CMPE10	R/W-0 CMPE9	R/W-0 CMPE8
7:0	R/W-0 CMPE7	R/W-0 CMPE6	R/W-0 CMPE5	R/W-0 CMPE4	R/W-0 CMPE3	R/W-0 CMPE2	R/W-0 CMPE1	R/W-0 CMPE0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **CMPE31:CMPE0**: ADC Digital Comparator 'x' Enable bits^(2,3)

These bits enable conversion results corresponding to the Analog Input to be processed by the Digital Comparator. CMPE0 enables AN0, CMPE1 enables AN1, and so on.

Note 1: This bit is not available on 64-pin devices.

2: CMPE_x = AN_x, where 'x' = 0-31 (Digital Comparator inputs are limited to AN0 through AN31).

3: Changing the bits in this register while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 30-28: EMAC1MAXF: ETHERNET CONTROLLER MAC MAXIMUM FRAME LENGTH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
	MACMAXF<15:8> ⁽¹⁾							
7:0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0
	MACMAXF<7:0> ⁽¹⁾							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MACMAXF<15:0>:** Maximum Frame Length bits⁽¹⁾

These bits reset to 0x05EE, which represents a maximum receive frame of 1518 octets. An untagged maximum size Ethernet frame is 1518 octets. A tagged frame adds four octets for a total of 1522 octets. If a shorter/longer maximum length restriction is desired, program this 16-bit field.

Note 1: If a proprietary header is allowed, this bit should be adjusted accordingly. For example, if 4-byte headers are prepended to frames, MACMAXF could be set to 1527 octets. This would allow the maximum VLAN tagged frame plus the 4-byte header.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 30-30: EMAC1TEST: ETHERNET CONTROLLER MAC TEST REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	TESTBP	TESTPAUSE ⁽¹⁾	SHRTQNTA ⁽¹⁾

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2 **TESTBP:** Test Backpressure bit

1 = The MAC will assert backpressure on the link. Backpressure causes preamble to be transmitted, raising carrier sense. A transmit packet from the system will be sent during backpressure.

0 = Normal operation

bit 1 **TESTPAUSE:** Test PAUSE bit⁽¹⁾

1 = The MAC Control sub-layer will inhibit transmissions, just as if a PAUSE Receive Control frame with a non-zero pause time parameter was received

0 = Normal operation

bit 0 **SHRTQNTA:** Shortcut PAUSE Quanta bit⁽¹⁾

1 = The MAC reduces the effective PAUSE Quanta from 64 byte-times to 1 byte-time

0 = Normal operation

Note 1: This bit is only used for testing purposes.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 30-37: EMAC1SA0: ETHERNET CONTROLLER MAC STATION ADDRESS 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR6<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR5<7:0>							

Legend:

R = Readable bit

W = Writable bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STNADDR6<7:0>:** Station Address Octet 6 bits

These bits hold the sixth transmitted octet of the station address.

bit 7-0 **STNADDR5<7:0>:** Station Address Octet 5 bits

These bits hold the fifth transmitted octet of the station address.

- Note 1:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.
- 2:** This register is loaded at reset from the factory preprogrammed station address.

37.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MZ EF electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MZ EF devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Specifications for Extended Temperature devices (-40°C to +125°C) that are different from the specifications in this section are provided in **38.0 “Extended Temperature Electrical Characteristics”**.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias	-40°C to +85°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to VSS (Note 3)	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 2.1V (Note 3)	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.1V (Note 3)	-0.3V to +3.6V
Voltage on D+ or D- pin with respect to VUSB3V3	-0.3V to (VUSB3V3 + 0.3V)
Voltage on VBUS with respect to VSS	-0.3V to +5.5V
Maximum current out of VSS pin(s)	200 mA
Maximum current into VDD pin(s) (Note 2)	200 mA
Maximum current sunk/sourced by any 4x I/O pin (Note 4)	15 mA
Maximum current sunk/sourced by any 8x I/O pin (Note 4)	25 mA
Maximum current sunk/sourced by any 12x I/O pin (Note 4)	33 mA
Maximum current sunk by all ports	150 mA
Maximum current sourced by all ports (Note 2)	150 mA

Note 1: Stresses above those listed under “**Absolute Maximum Ratings**” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 37-2).

3: See the pin name tables (Table 2 through Table 4) for the 5V tolerant pins.

4: Characterized, but not tested. Refer to parameters DO10, DO20, and DO20a for the 4x, 8x, and 12x I/O pin lists.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

37.1 DC Characteristics

TABLE 37-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts) (Note 1)	Temp. Range (in °C)	Max. Frequency	Comment
			PIC32MZ EF Devices	
DC5	2.1V-3.6V	-40°C to +85°C	200 MHz	—

Note 1: Overall functional device operation at $V_{BORMIN} < V_{DD} < V_{DDMIN}$ is guaranteed, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below V_{DDMIN} . Refer to parameter BO10 in Table 37-5 for BOR values.

TABLE 37-2: THERMAL OPERATING CONDITIONS

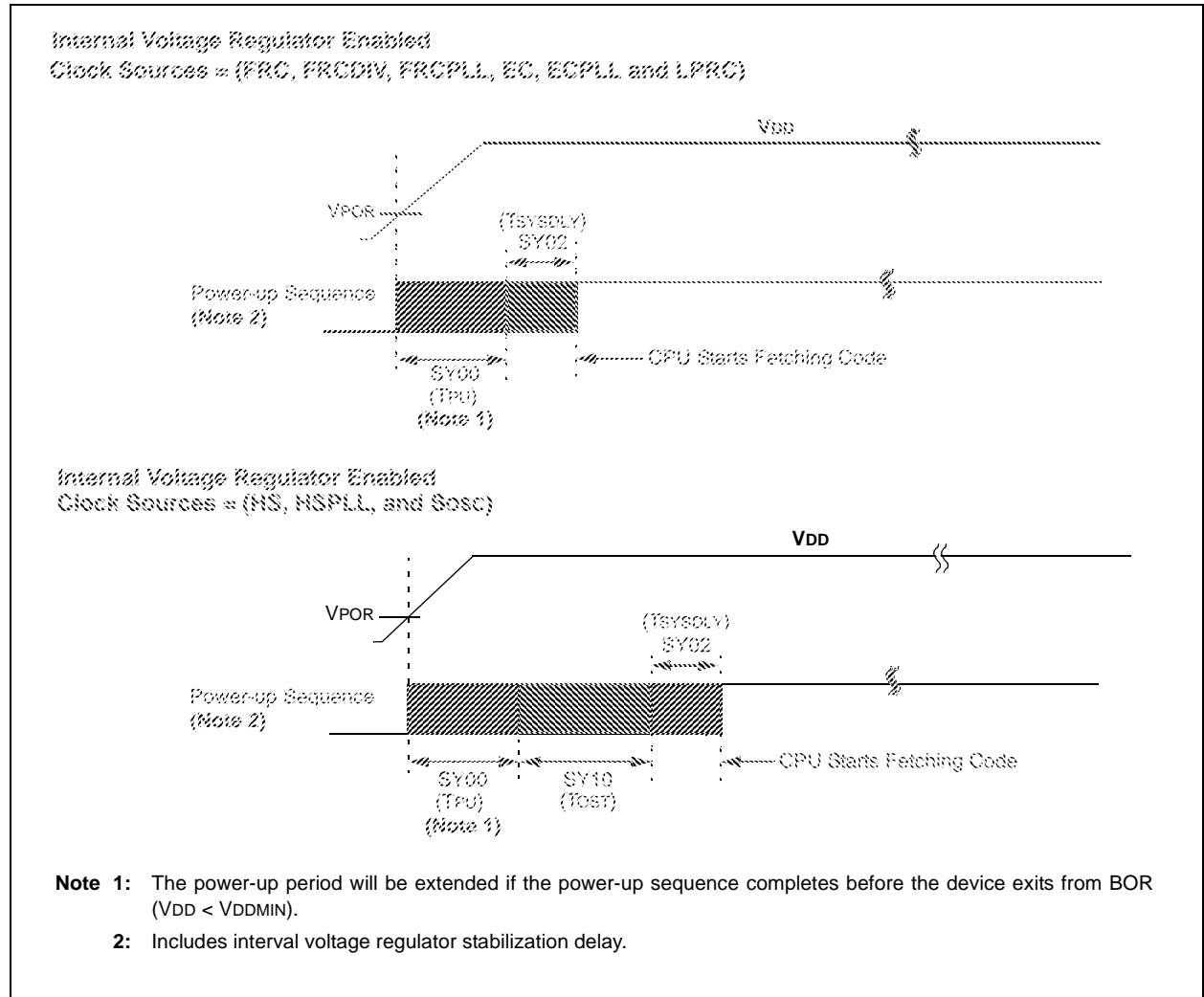
Rating	Symbol	Min.	Typical	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - S \cdot I_{OH})$ I/O Pin Power Dissipation: $P_{I/O} = S \cdot ((V_{DD} - V_{OH}) \times I_{OH}) + S \cdot (V_{OL} \times I_{OL})$	PD	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	PD _{MAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 37-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 64-pin QFN (9x9x0.9 mm)	θ_{JA}	28	—	°C/W	1
Package Thermal Resistance, 64-pin TQFP (10x10x1 mm)	θ_{JA}	49	—	°C/W	1
Package Thermal Resistance, 100-pin TQFP (12x12x1 mm)	θ_{JA}	43	—	°C/W	1
Package Thermal Resistance, 100-pin TQFP (14x14x1 mm)	θ_{JA}	40	—	°C/W	1
Package Thermal Resistance, 124-pin VTLA (9x9x0.9 mm)	θ_{JA}	30	—	°C/W	1
Package Thermal Resistance, 144-pin TQFP (16x16x1 mm)	θ_{JA}	42	—	°C/W	1
Package Thermal Resistance, 144-pin LQFP (20x20x1.4 mm)	θ_{JA}	39	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

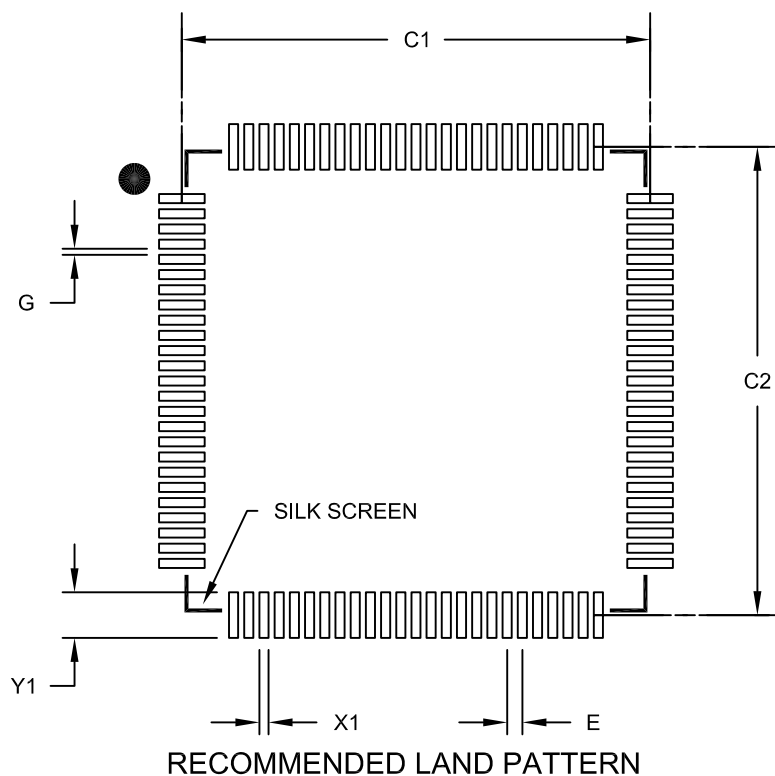
FIGURE 37-4: POWER-ON RESET TIMING CHARACTERISTICS



PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

100-Lead Plastic Thin Quad Flatpack (PF) - 14x14x1 mm Body 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		15.40	
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X100)	X1			0.30
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2110B

A.2 Analog-to-Digital Converter (ADC)

The PIC32MZ EF family of devices has a new 12-bit High-Speed Successive Approximation Register (SAR) ADC module that replaces the 10-bit ADC module in PIC32MX5XX/6XX/7XX devices; therefore, the use of **Bold** type to show differences is *not* used in the following table. Note that not all register differences are described in this section; however, the key feature differences are listed in Table A-3.

TABLE A-3: ADC DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Clock Selection and Operating Frequency (TAD)	
On PIC32MX devices, the ADC clock was derived from either the FRC or from the PBCLK.	On PIC32MZ EF devices, the three possible sources of the ADC clock are FRC, REFCLKO3, and SYSCLK.
ADRC (AD1CON3<15>) 1 = FRC clock 0 = Clock derived from Peripheral Bus Clock (PBCLK)	ADCSEL<1:0> (ADCCON3<31:30>) 11 = FRC 10 = REFCLKO3 01 = SYSCLK 00 = Reserved
On PIC32MX devices, if the ADC clock was derived from the PBCLK, that frequency was divided further down, with a maximum divisor of 512, and a minimum divisor of two.	On PIC32MZ EF devices, any ADC clock source can be divided down separately for each dedicated ADC and the shared ADC, with a maximum divisor of 254. The input clock can also be fed directly to the ADC.
ADCS<7:0> (AD1CON3<7:0>) 11111111 = 512 * TPB = TAD • • • 00000001 = 4 * TPB = TAD 00000000 = 2 * TPB = TAD	ADCDIV<6:0> (ADCTIME<22:16>) ADCDIV<6:0> (ADCCON2<6:0>) 11111111 = 254 * TQ = TAD • • • 00000111 = 6 * TQ = TAD 00000110 = 4 * TQ = TAD 00000011 = 2 * TQ = TAD 00000000 = TQ = TAD