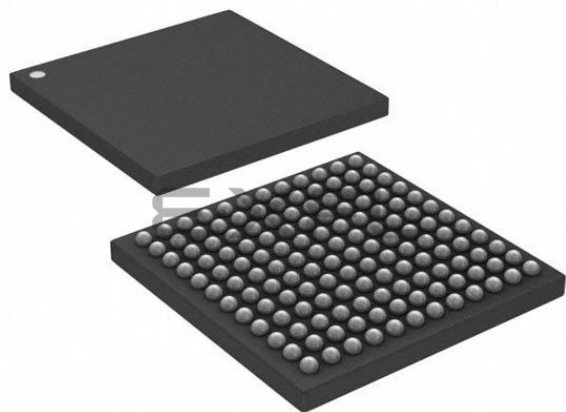




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Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TFBGA
Supplier Device Package	144-TFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efg144-i-jwx

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

NOTES:

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 1-10: I2C1 THROUGH I2C5 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Inter-Integrated Circuit 1							
SCL1	44	66	B37	95	I/O	ST	I2C1 Synchronous Serial Clock Input/Output
SDA1	43	67	A45	96	I/O	ST	I2C1 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 2							
SCL2	—	59	A41	85	I/O	ST	I2C2 Synchronous Serial Clock Input/Output
SDA2	—	60	B34	86	I/O	ST	I2C2 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 3							
SCL3	51	58	A39	80	I/O	ST	I2C3 Synchronous Serial Clock Input/Output
SDA3	50	57	B31	79	I/O	ST	I2C3 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 4							
SCL4	6	12	B7	16	I/O	ST	I2C4 Synchronous Serial Clock Input/Output
SDA4	5	11	A8	15	I/O	ST	I2C4 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 5							
SCL5	42	65	A44	91	I/O	ST	I2C5 Synchronous Serial Clock Input/Output
SDA5	41	64	B36	90	I/O	ST	I2C5 Synchronous Serial Data Input/Output

Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer

Analog = Analog input
O = Output
PPS = Peripheral Pin Select

P = Power
I = Input

TABLE 1-11: COMPARATOR 1, COMPARATOR 2 AND CVREF PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Comparator Voltage Reference							
CVREF+	16	29	A20	40	I	Analog	Comparator Voltage Reference (High) Input
CVREF-	15	28	B15	39	I	Analog	Comparator Voltage Reference (Low) Input
CVREFOUT	23	34	B19	49	O	Analog	Comparator Voltage Reference Output
Comparator 1							
C1INA	11	20	B11	25	I	Analog	Comparator 1 Positive Input
C1INB	12	21	A13	26	I	Analog	Comparator 1 Selectable Negative Input
C1INC	5	11	A8	15	I	Analog	
C1IND	4	10	B6	14	I	Analog	
C1OUT	PPS	PPS	PPS	PPS	O	—	Comparator 1 Output
Comparator 2							
C2INA	13	22	A14	31	I	Analog	Comparator 2 Positive Input
C2INB	14	23	A16	34	I	Analog	Comparator 2 Selectable Negative Input
C2INC	10	16	B9	21	I	Analog	
C2IND	6	12	B7	16	I	Analog	
C2OUT	PPS	PPS	PPS	PPS	O	—	Comparator 2 Output

Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer

Analog = Analog input
O = Output
PPS = Peripheral Pin Select

P = Power
I = Input

FIGURE 4-3: MEMORY MAP FOR DEVICES WITH 1024 KB OF PROGRAM MEMORY AND 512 KB OF RAM^(1,2)

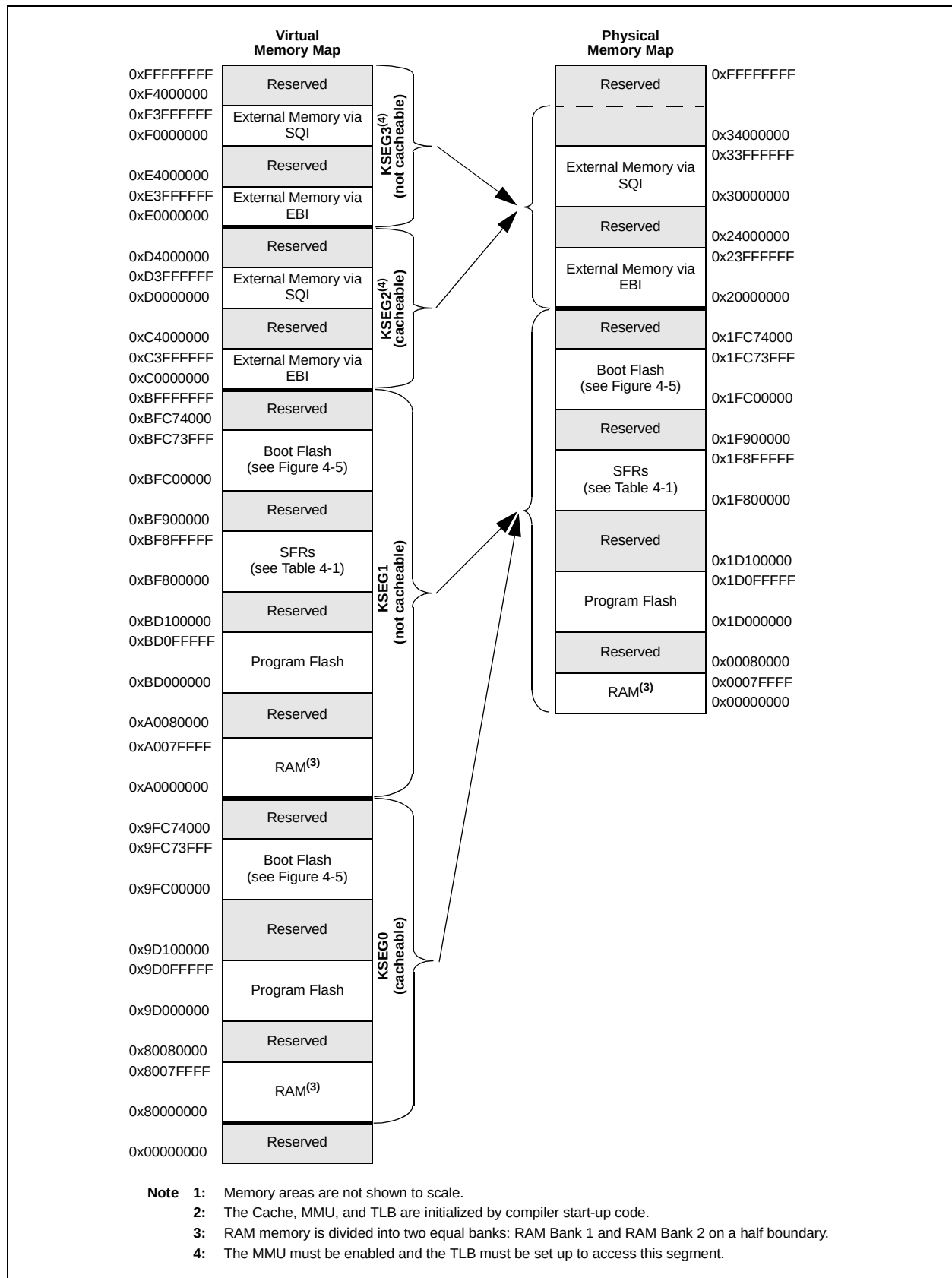


TABLE 4-11: SYSTEM BUS TARGET 3 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
8C20	SBT3ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>			0000	
8C24	SBT3ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000	
8C28	SBT3ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8C30	SBT3ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000	
8C38	SBT3ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000	
8C40	SBT3REG0	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>					PRI	—	SIZE<4:0>					—	—	—	xxxx	
8C50	SBT3RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C58	SBT3WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C60	SBT3REG1	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>					PRI	—	SIZE<4:0>					—	—	—	xxxx	
8C70	SBT3RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C78	SBT3WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C80	SBT3REG2	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>					PRI	—	SIZE<4:0>					—	—	—	xxxx	
8C90	SBT3RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C98	SBT3WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

TABLE 8-2: OSCILLATOR CONFIGURATION REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets ⁽²⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1360	PB7DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8800
1370	PB8DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
13C0	SLEWCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	SYSDIV<3:0>				0000
		15:0	—	—	—	—	—	SLWDIV<2:0>			—	—	—	—	—	UPEN	DNEN	BUSY	0204
13D0	CLKSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	LPRC RDY	SOSC RDY	—	POSC RDY	SPLL DIVRDY	FRCRDY	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.
- 2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

NOTES:

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0			
309C	USB E3RXA	31:16	—	RXHUBPRT<6:0>								MULTTRAN	RXHUBADD<6:0>								0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>								0000	
30A0	US BE4TXA	31:16	—	TXHUBPRT<6:0>								MULTTRAN	TXHUBADD<6:0>								0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>								0000	
30A4	USB E4RXA	31:16	—	RXHUBPRT<6:0>								MULTTRAN	RXHUBADD<6:0>								0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>								0000	
30A8	USB E5TXA	31:16	—	TXHUBPRT<6:0>								MULTTRAN	TXHUBADD<6:0>								0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>								0000	
30AC	USB E5RXA	31:16	—	RXHUBPRT<6:0>								MULTTRAN	RXHUBADD<6:0>								0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>								0000	
30B0	USB E6TXA	31:16	—	TXHUBPRT<6:0>								MULTTRAN	TXHUBADD<6:0>								0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>								0000	
30B4	USB E6RXA	31:16	—	RXHUBPRT<6:0>								MULTTRAN	RXHUBADD<6:0>								0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>								0000	
30B8	USB E7TXA	31:16	—	TXHUBPRT<6:0>								MULTTRAN	TXHUBADD<6:0>								0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>								0000	
30BC	USB E7RXA	31:16	—	RXHUBPRT<6:0>								MULTTRAN	RXHUBADD<6:0>								0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>								0000	
3100	USB E0CSR0	31:16	Indexed by the same bits in USBIE0CSR0																0000		
		15:0																	0000		
3108	USB E0CSR2	31:16	Indexed by the same bits in USBIE0CSR2																0000		
		15:0																	0000		
310C	USB E0CSR3	31:16	Indexed by the same bits in USBIE0CSR3																0000		
		15:0																	0000		
3110	USB E1CSR0	31:16	Indexed by the same bits in USBIE1CSR0																0000		
		15:0																	0000		
3114	USB E1CSR1	31:16	Indexed by the same bits in USBIE1CSR1																0000		
		15:0																	0000		
3118	USB E1CSR2	31:16	Indexed by the same bits in USBIE1CSR2																0000		
		15:0																	0000		
311C	USB E1CSR3	31:16	Indexed by the same bits in USBIE1CSR3																0000		
		15:0																	0000		
3120	USB E2CSR0	31:16	Indexed by the same bits in USBIE2CSR0																0000		
		15:0																	0000		
3124	USB E2CSR1	31:16	Indexed by the same bits in USBIE2CSR1																0000		
		15:0																	0000		

Note	1: Device mode. 2: Host mode. 3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0). 4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).
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PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 11-1: USBCSR0: USB CONTROL STATUS REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	R-0, HS EP7TXIF	R-0, HS EP6TXIF	R-0, HS EP5TXIF	R-0, HS EP4TXIF	R-0, HS EP3TXIF	R-0, HS EP2TXIF	R-0, HS EP1TXIF	R-0, HS EP0IF
15:8	R/W-0 ISOUPD —	R/W-0 SOFTCONN —	R/W-1 HSEN	R-0, HS HSMODE	R-0 RESET	R/W-0 RESUME	R-0, HC SUSPMODE	R/W-0 SUSPEN
7:0	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		FUNC<6:0>						
		—	—	—	—	—	—	—

Legend:	HS = Hardware Set	HC = Hardware Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-17 **EP7TXIF:EP1TXIF:** Endpoint 'n' TX Interrupt Flag bit

- 1 = Endpoint has a transmit interrupt to be serviced
- 0 = No interrupt event

bit 16 **EP0IF:** Endpoint 0 Interrupt bit

- 1 = Endpoint 0 has an interrupt to be serviced
- 0 = No interrupt event

All EPxTX and EP0 bits are cleared when the byte is read. Therefore, these bits must be read independently from the remaining bits in this register to avoid accidental clearing.

bit 15 **ISOUPD:** ISO Update bit (*Device mode only; unimplemented in Host mode*)

- 1 = USB module will wait for a SOF token from the time TXPKTRDY is set before sending the packet
- 0 = No change in behavior

This bit only affects endpoints performing isochronous transfers when in *Device mode*. This bit is unimplemented in *Host mode*.

bit 14 **SOFTCONN:** Soft Connect/Disconnect Feature Selection bit

- 1 = The USB D+/D- lines are enabled and active
- 0 = The USB D+/D- lines are disabled and are tri-stated

This bit is only available in *Device mode*.

bit 13 **HSEN:** Hi-Speed Enable bit

- 1 = The USB module will negotiate for Hi-Speed mode when the device is reset by the hub
- 0 = Module only operates in Full-Speed mode

bit 12 **HSMODE:** Hi-Speed Mode Status bit

- 1 = Hi-Speed mode successfully negotiated during USB reset
- 0 = Module is not in Hi-Speed mode

In *Device mode*, this bit becomes valid when a USB reset completes. In *Host mode*, it becomes valid when the RESET bit is cleared.

bit 11 **RESET:** Module Reset Status bit

- 1 = Reset signaling is present on the bus
- 0 = Normal module operation

In *Device mode*, this bit is read-only. In *Host mode*, this bit is read/write.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 11-8: USBIENCSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AUTOSET	ISO —	MODE	DMAREQEN	FRCDATTG	DMAREQMD	— DATAWEN	— DATATGGL
23:16	R/W-0, HS	R/W-0, HC	R/W-0, HS	R/W-0	R/W-0	R/W-0, HS	R/W-0	R/W-0, HC
	INCOMPTX NAKTMOUT	CLRDT	SENTSTALL RXSTALL	SENDSTALL SETUPPKT	FLUSH	UNDERRUN ERROR	FIFONE	TXPKTRDY
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MULT<4:0>					TXMAXP<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXMAXP<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31 **AUTOSET:** Auto Set Control bit
1 = TXPKTRDY will be automatically set when data of the maximum packet size (value in TXMAXP) is loaded into the TX FIFO. If a packet of less than the maximum packet size is loaded, then TXPKTRDY will have to be set manually.
0 = TXPKTRDY must be set manually for all packet sizes
- bit 30 **ISO:** Isochronous TX Endpoint Enable bit (Device mode)
1 = Enables the endpoint for Isochronous transfers
0 = Disables the endpoint for Isochronous transfers and enables it for Bulk or Interrupt transfers.
This bit only has an effect in Device mode. In Host mode, it always returns zero.
- bit 29 **MODE:** Endpoint Direction Control bit
1 = Endpoint is TX
0 = Endpoint is RX
This bit only has any effect where the same endpoint FIFO is used for both TX and RX transactions.
- bit 28 **DMAREQEN:** Endpoint DMA Request Enable bit
1 = DMA requests are enabled for this endpoint
0 = DMA requests are disabled for this endpoint
- bit 27 **FRCDATTG:** Force Endpoint Data Toggle Control bit
1 = Forces the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received.
0 = No forced behavior
- bit 26 **DMAREQMD:** Endpoint DMA Request Mode Control bit
1 = DMA Request Mode 1
0 = DMA Request Mode 0
This bit must not be cleared either before or in the same cycle as the above DMAREQEN bit is cleared.
- bit 25 **DATAWEN:** Data Toggle Write Enable bit (Host mode)
1 = Enable the current state of the TX Endpoint data toggle (DATATGGL) to be written
0 = Disables writing the DATATGGL bit
- bit 24 **DATATGGL:** Data Toggle Control bit (Host mode)
When read, this bit indicates the current state of the TX Endpoint data toggle. If DATAWEN = 1, this bit may be written with the required setting of the data toggle. If DATAWEN = 0, any value written to this bit is ignored.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 11-12: USBFIFOx: USB FIFO DATA REGISTER 'x' ('x' = 0-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **DATA<31:0>**: USB Transmit/Receive FIFO Data bits

Writes to this register loads data into the TxFIFO for the corresponding endpoint. Reading from this register unloads data from the RxFIFO for the corresponding endpoint.

Transfers may be 8-bit, 16-bit or 32-bit as required, and any combination of access is allowed provided the data accessed is contiguous. However, all transfers associated with one packet must be of the same width so that data is consistently byte-, word- or double-word aligned. The last transfer may contain fewer bytes than the previous transfers in order to complete an odd-byte or odd-word transfer.

TABLE 12-23: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1620	RPE8R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE8R<3:0>				0000
1624	RPE9R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE9R<3:0>				0000
1640	RPF0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF0R<3:0>				0000
1644	RPF1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF1R<3:0>				0000
1648	RPF2R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF2R<3:0>				0000
164C	RPF3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF3R<3:0>				0000
1650	RPF4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF4R<3:0>				0000
1654	RPF5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF5R<3:0>				0000
1660	RPF8R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF8R<3:0>				0000
1670	RPF12R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF12R<3:0>				0000
1674	RPF13R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF13R<3:0>				0000
1680	RPG0R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG0R<3:0>				0000
1684	RPG1R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG1R<3:0>				0000
1698	RPG6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG6R<3:0>				0000
169C	RPG7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG7R<3:0>				0000
16A0	RPG8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG8R<3:0>				0000
16A4	RPG9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG9R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: This register is not available on 64-pin devices.
 2: This register is not available on 64-pin and 100-pin devices.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 15-7: DMTPSINTV: POST STATUS CONFIGURE DMT INTERVAL STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-y	R-y	R-y
	PSINTV<7:0>							

Legend:

R = Readable bit

W = Writable bit

y = Value set from Configuration bits on POR

-n = Value at POR

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **PSINTV<31:0>:** DMT Window Interval Configuration Status bits

This is always the value of the DMTINTV<2:0> bits in the DEVCFG1 Configuration register.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 19-1: SPIxCON: SPI CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 FRMEN	R/W-0 FRMSYNC	R/W-0 FRMPOL	R/W-0 MSEN	R/W-0 FRMSYPW	FRMCNT<2:0>		
23:16	R/W-0 MCLKSEL ⁽¹⁾	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0 SPIFE	R/W-0 ENHBUF ⁽¹⁾
15:8	R/W-0 ON	U-0 —	R/W-0 SIDL	R/W-0 DISSDO ⁽⁴⁾	R/W-0 MODE32	R/W-0 MODE16	R/W-0 SMP	R/W-0 CKE ⁽²⁾
7:0	R/W-0 SSEN	R/W-0 CKP ⁽³⁾	R/W-0 MSTEN	R/W-0 DISSDI ⁽⁴⁾	R/W-0 STXISEL<1:0>	SRXISEL<1:0>		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31 **FRMEN:** Framed SPI Support bit
1 = Framed SPI support is enabled ($\overline{SSx}$ pin used as FSYNC input/output)
0 = Framed SPI support is disabled
- bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on $\overline{SSx}$ pin bit (Framed SPI mode only)
1 = Frame sync pulse input (Slave mode)
0 = Frame sync pulse output (Master mode)
- bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)
1 = Frame pulse is active-high
0 = Frame pulse is active-low
- bit 28 **MSEN:** Master Mode Slave Select Enable bit
1 = Slave select SPI support is enabled. The $\overline{SS}$ pin is automatically driven during transmission in Master mode. Polarity is determined by the FRMPOL bit.
0 = Slave select SPI support is disabled.
- bit 27 **FRMSYPW:** Frame Sync Pulse Width bit
1 = Frame sync pulse is one character wide
0 = Frame sync pulse is one clock wide
- bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits. Controls the number of data characters transmitted per pulse. This bit is only valid in Framed mode.
111 = Reserved
110 = Reserved
101 = Generate a frame sync pulse on every 32 data characters
100 = Generate a frame sync pulse on every 16 data characters
011 = Generate a frame sync pulse on every 8 data characters
010 = Generate a frame sync pulse on every 4 data characters
001 = Generate a frame sync pulse on every 2 data characters
000 = Generate a frame sync pulse on every data character
- bit 23 **MCLKSEL:** Master Clock Enable bit⁽¹⁾
1 = REFCLKO1 is used by the Baud Rate Generator
0 = PBCLK2 is used by the Baud Rate Generator
- bit 22-18 **Unimplemented:** Read as '0'

- Note 1:** This bit can only be written when the ON bit = 0. Refer to **Section 37.0 “Electrical Characteristics”** for maximum clock frequency requirements.
- 2:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
- 3:** When AUDEN = 1, the SPI/I²S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.
- 4:** This bit present for legacy compatibility and is superseded by PPS functionality on these devices (see **Section 12.4 “Peripheral Pin Select (PPS)”** for more information).

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 20-8: SQI1INTEN: SQI INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DMAEIE	PKTCOMPIE	BDDONEIE	CONTHRIE
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CONEMPTYIE	CONFULLIE	RXTHRIE	RXFULLIE	RXEMPTYIE	TXTHRIE	TXFULLIE	TXEMPTYIE

Legend:	HS = Hardware Set
R = Readable bit	W = Writable bit
-n = Value at POR	U = Unimplemented bit, read as '0'
	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11 **DMAEIE:** DMA Bus Error Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 10 **PKTCOMPIE:** DMA Buffer Descriptor Packet Complete Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 9 **BDDONEIE:** DMA Buffer Descriptor Done Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 8 **CONTHRIE:** Control Buffer Threshold Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 7 **CONEMPTYIE:** Control Buffer Empty Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 6 **CONFULLIE:** Control Buffer Full Interrupt Enable bit

This bit enables an interrupt when the receive FIFO buffer is full.

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 5 **RXTHRIE:** Receive Buffer Threshold Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 4 **RXFULLIE:** Receive Buffer Full Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 3 **RXEMPTYIE:** Receive Buffer Empty Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 2 **TXTHRIE:** Transmit Threshold Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 1 **TXFULLIE:** Transmit Buffer Full Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 0 **TXEMPTYIE:** Transmit Buffer Empty Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 23-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	R/W-0, HC RDSTART	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0 DUALBUF	U-0 —
15:8	R/W-0 ON	U-0 —	R/W-0 SIDL	R/W-0 ADRMUX<1:0>	R/W-0 ADRMUX<1:0>	R/W-0 PMP TTL	R/W-0 PTWREN	R/W-0 PTRDEN
7:0	R/W-0 CSF<1:0> ⁽¹⁾	R/W-0 ALP ⁽¹⁾	R/W-0 CS2P ⁽¹⁾	R/W-0 CS1P ⁽¹⁾	R/W-0 CS1P ⁽¹⁾	U-0 —	R/W-0 WRSP	R/W-0 RDSP

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **RDSTART:** Start Read on PMP Bus bit

This bit is cleared by hardware at the end of the read cycle.

1 = Start a read cycle on the PMP bus

0 = No effect

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **DUALBUF:** Dual Read/Write Buffers enable bit

This bit is valid in Master mode only.

1 = PMP uses separate registers for reads and writes (PMRADDR, PMDATAIN, PMWADDR, PMDATAOUT)

0 = PMP uses legacy registers (PMADDR, PMDATA)

bit 16 **Unimplemented:** Read as '0'

bit 15 **ON:** Parallel Master Port Enable bit

1 = PMP is enabled

0 = PMP is disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits

11 = Lower 8 bits of address are multiplexed on PMD<15:0> pins; upper 8 bits are not used

10 = All 16 bits of address are multiplexed on PMD<15:0> pins

01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<15:8>

00 = Address and data appear on separate pins

bit 10 **PMP TTL:** PMP Module TTL Input Buffer Select bit

1 = PMP module uses TTL input buffers

0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit

1 = PMWR/PMENB port is enabled

0 = PMWR/PMENB port is disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit

1 = PMRD/PMWR port is enabled

0 = PMRD/PMWR port is disabled

Note 1: These bits have no effect when their corresponding pins are used as address lines.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 29-15: CiFLTCON5: CAN FILTER CONTROL REGISTER 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN23	MSEL23<1:0>		FSEL23<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN22	MSEL22<1:0>		FSEL22<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN21	MSEL21<1:0>		FSEL21<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN20	MSEL20<1:0>		FSEL20<4:0>				

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31 **FLTEN23:** Filter 23 Enable bit
1 = Filter is enabled
0 = Filter is disabled
- bit 30-29 **MSEL23<1:0>:** Filter 23 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected
- bit 28-24 **FSEL23<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0
- bit 23 **FLTEN22:** Filter 22 Enable bit
1 = Filter is enabled
0 = Filter is disabled
- bit 22-21 **MSEL22<1:0>:** Filter 22 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected
- bit 20-16 **FSEL22<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 30-19: ETHMCOLFRM: ETHERNET CONTROLLER MULTIPLE COLLISION FRAMES STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MCOLFRMCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MCOLFRMCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MCOLFRMCNT<15:0>:** Multiple Collision Frame Count bits

Increment count for frames that were successfully transmitted after there was more than one collision.

Note 1: This register is only used for TX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

TABLE 33-2: PERIPHERAL MODULE DISABLE REGISTER SUMMARY

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0040	PMD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CVRMD	—	—	—	—	—	—	—	—	—	—	—	ADCMD	0000
0050	PMD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMP2MD	CMP1MD	0000
0060	PMD3	31:16	—	—	—	—	—	—	—	OC9MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
		15:0	—	—	—	—	—	—	—	IC9MD	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	0000
0070	PMD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	T9MD	T8MD	T7MD	T6MD	T5MD	T4MD	T3MD	T2MD	T1MD	0000
0080	PMD5	31:16	—	—	CAN2MD	CAN1MD	—	—	—	USBMD	—	—	—	I2C5MD	I2C4MD	I2C3MD	I2C2MD	I2C1MD	0000
		15:0	—	—	SPI6MD	SPI5MD	SPI4MD	SPI3MD	SPI2MD	SPI1MD	—	—	U6MD	U5MD	U4MD	U3MD	U2MD	U1MD	0000
0090	PMD6	31:16	—	—	—	ETHMD	—	—	—	—	SQ1MD	—	—	—	—	—	EBIMD	PMPMD	0000
		15:0	—	—	—	—	REFO4MD	REFO3MD	REFO2MD	REFO1MD	—	—	—	—	—	—	—	RTCCMD	0000
00A0	PMD7	31:16	—	—	—	—	—	—	—	—	—	CRYPTMD	—	RNGMD	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	DMAMD	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

TABLE 34-3: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets ⁽¹⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	CFGCON	31:16	—	—	—	—	—	—	DMAPRI	CPUPRI	—	—	—	—	—	—	ICACLK	OCACLK	0000
		15:0	—	—	IOLOCK	PMDLOCK	PGLOCK	—	—	USBSSSEN	IOANCPEN	—	ECCCON<1:0>		JTAGEN	TROEN	—	TDOEN	000B
0020	DEVID	31:16	VER<3:0>					DEVID<27:16>											XXXX
		15:0	DEVID<15:0>																XXXX
0030	SYSKEY	31:16	SYSKEY<31:0>																0000
		15:0	SYSKEY<31:0>																0000
00C0	CFGEBIA ⁽²⁾	31:16	EBIPINEN	—	—	—	—	—	—	—	EBIA23EN	EBIA22EN	EBIA21EN	EBIA20EN	EBIA19EN	EBIA18EN	EBIA17EN	EBIA16EN	0000
		15:0	EBIA15EN	EBIA14EN	EBIA13EN	EBIA12EN	EBIA11EN	EBIA10EN	EBIA9EN	EBIA8EN	EBIA7EN	EBIA6EN	EBIA5EN	EBIA4EN	EBIA3EN	EBIA2EN	EBIA1EN	EBIA0EN	0000
00D0	CFGEBIC ⁽²⁾	31:16	EBI RDYINV3	EBI RDYINV2	EBI RDYINV1	—	EBI RDYEN3	EBI RDYEN2	EBI RDYEN1	—	—	—	—	—	—	—	EBI RDYLV1	EBIRPEN	0000
		15:0	—	—	EBIWEEN	EBIOEEN	—	—	EBIBSEN1	EBIBSEN0	EBICSEN3	EBICSEN2	EBICSEN1	EBICSEN0	—	—	EBIDEN1	EBIDEN0	0000
00E0	CFGPG	31:16	ICD1PG<1:0>		—	—	—	—	CRYPTPG<1:0>		FCPG<1:0>		SQ1PG<1:0>		—	—	ETHPG<1:0>		0000
		15:0	CAN2PG<1:0>		CAN1PG<1:0>		—	—	USBPG<1:0>		—	—	DMAPG<1:0>		—	—	CPUPG<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

Note 2: This register is not available on 64-pin devices.

TABLE 34-4: DEVICE SERIAL NUMBER SUMMARY

Virtual Address (BFC5_#)	Register Name	Bit Range	Bits																All Resets ⁽¹⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4020	DEVSN0	31:16	Device Serial Number <31:16>																XXXX
		15:0	Device Serial Number <15:0>																XXXX
4024	DEVSN1	31:16	Device Serial Number <31:16>																XXXX
		15:0	Device Serial Number <15:0>																XXXX

Legend: x = unknown value on Reset.

Note 1: Reset values are dependent on the device variant.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 37-35: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	Symbol	Characteristics		Min. ⁽¹⁾	Max.	Units	Conditions
IM21	TR:SCL	SDA _x and SCL _x Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode (Note 2)	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode (Note 2)	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode (Note 2)	0	0.3	μs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	
			1 MHz mode (Note 2)	TPBCLK2 * (BRG + 2)	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	
			1 MHz mode (Note 2)	TPBCLK2 * (BRG + 2)	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	
			1 MHz mode (Note 2)	TPBCLK2 * (BRG + 2)	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	
			1 MHz mode (Note 2)	TPBCLK2 * (BRG + 2)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	—
			1 MHz mode (Note 2)	—	350	ns	—
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode (Note 2)	0.5	—	μs	
IM50	Cb	Bus Capacitive Loading	—	—	—	pF	See parameter DO58
IM51	TPGD	Pulse Gobbler Delay	—	52	312	ns	See Note 3

Note 1: BRG is the value of the I²C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.