



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efg144-i-ph

3.7 M-Class Core Configuration

Register 3-1 through Register 3-4 show the default configuration of the M-Class core, which is included on the PIC32MZ EF family of devices.

REGISTER 3-1: CONFIG: CONFIGURATION REGISTER; CP0 REGISTER 16, SELECT 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	ISP
23:16	R-0	R-0	R-1	R-0	U-0	R-1	R-0	R-0
	DSP	UDI	SB	MDU	—	MM<1:0>		BM
15:8	R-0	R-0	R-0	R-0	R-0	R-1	R-0	R-0
	BE	AT<1:0>		AR<2:0>			MT<2:1>	
7:0	R-1	U-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-0
	MT<0>	—	—	—	—	K0<2:0>		

Legend:

r = Reserved bit
R = Readable bit
-n = Value at POR
W = Writable bit
'1' = Bit is set
U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

- bit 31 **Reserved:** This bit is hardwired to '1' to indicate the presence of the Config1 register.
- bit 30-25 **Unimplemented:** Read as '0'
- bit 24 **ISP:** Instruction Scratch Pad RAM bit
0 = Instruction Scratch Pad RAM is not implemented
- bit 23 **DSP:** Data Scratch Pad RAM bit
0 = Data Scratch Pad RAM is not implemented
- bit 22 **UDI:** User-defined bit
0 = CorExtend User-Defined Instructions are not implemented
- bit 21 **SB:** SimpleBE bit
1 = Only Simple Byte Enables are allowed on the internal bus interface
- bit 20 **MDU:** Multiply/Divide Unit bit
0 = Fast, high-performance MDU
- bit 19 **Unimplemented:** Read as '0'
- bit 18-17 **MM<1:0>:** Merge Mode bits
10 = Merging is allowed
- bit 16 **BM:** Burst Mode bit
0 = Burst order is sequential
- bit 15 **BE:** Endian Mode bit
0 = Little-endian
- bit 14-13 **AT<1:0>:** Architecture Type bits
00 = MIPS32
- bit 12-10 **AR<2:0>:** Architecture Revision Level bits
001 = MIPS32 Release 2
- bit 9-7 **MT<2:0>:** MMU Type bits
001 = M-Class MPU Microprocessor core uses a TLB-based MMU
- bit 6-3 **Unimplemented:** Read as '0'
- bit 2-0 **K0<2:0>:** Kseg0 Coherency Algorithm bits
011 = Cacheable, non-coherent, write-back, write allocate
010 = Uncached
001 = Cacheable, non-coherent, write-through, write allocate
000 = Cacheable, non-coherent, write-through, no write allocate
All other values are not used and mapped to other values. 100, 101, and 110 are mapped to 010. 111 is mapped to 010.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 3-4: CONFIG5: CONFIGURATION REGISTER 5; CP0 REGISTER 16, SELECT 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-1
	—	—	—	—	—	—	—	NF

Legend:

r = Reserved
R = Readable bit
-n = Value at POR
W = Writable bit
'1' = Bit is set
U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **NF:** Nested Fault bit

1 = Nested Fault feature is implemented

REGISTER 3-5: CONFIG7: CONFIGURATION REGISTER 7; CP0 REGISTER 16, SELECT 7

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	WII	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit
-n = Value at POR
W = Writable bit
'1' = Bit is set
U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31 **WII:** Wait IE Ignore bit

1 = Indicates that this processor will allow an interrupt to unblock a WAIT instruction

bit 30-0 **Unimplemented:** Read as '0'

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 3-6: FIR: FLOATING POINT IMPLEMENTATION REGISTER; CP1 REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-1	U-0	U-0	U-0	R-1
	—	—	—	UFRP	—	—	—	FC
23:16	R-1	R-1	R-1	R-1	R-0	R-0	R-1	R-1
	HAS2008	F64	L	W	MIPS3D	PS	D	S
15:8	R-1	R-0	R-1	R-0	R-0	R-1	R-1	R-1
	PRID<7:0>							
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	REVISION<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **UFRP:** User Mode FR Switching Instruction bit

1 = User mode FR switching instructions are supported

0 = User mode FR switching instructions are not supported

bit 27-25 **Unimplemented:** Read as '0'

bit 24 **FC:** Full Convert Ranges bit

1 = Full convert ranges are implemented (all numbers can be converted to another type by the FPU)

0 = Full convert ranges are not implemented

bit 23 **HAS008:** IEEE-754-2008 bit

1 = MAC2008, ABS2008, NAN2008 bits exist within the FCSR register

0 = MAC2009, ABS2008, and NAN2008 bits do not exist within the FCSR register

bit 22 **F64:** 64-bit FPU bit

1 = This is a 64-bit FPU

0 = This is not a 64-bit FPU

bit 21 **L:** Long Fixed Point Data Type bit

1 = Long fixed point data types are implemented

0 = Long fixed point data types are not implemented

bit 20 **W:** Word Fixed Point data type bit

1 = Word fixed point data types are implemented

0 = Word fixed point data types are not implemented

bit 19 **MIPS3D:** MIPS-3D ASE bit

1 = MIPS-3D is implemented

0 = MIPS-3D is not implemented

bit 18 **PS:** Paired Single Floating Point data bit

1 = PS floating point is implemented

0 = PS floating point is not implemented

bit 17 **D:** Double-precision (64-bit) Floating Point Data bit

1 = Double-precision floating point data types are implemented

0 = Double-precision floating point data types are not implemented

bit 16 **S:** Single-precision (32-bit) Floating Point Data bit

1 = Single-precision floating point data types are implemented

0 = Single-precision floating point data types are not implemented

bit 15-8 **PRID<7:0>:** Processor Identification bits

These bits allow software to distinguish between the various types of MIPS processors. For

PIC32 devices with the M-Class core, this value is 0xA7.

bit 7-0 **REVISION<7:0>:** Processor Revision Identification bits

These bits allow software to distinguish between one revision and another of the same processor type. This number is increased on major revisions of the processor core

FIGURE 4-2: MEMORY MAP FOR DEVICES WITH 1024 KB OF PROGRAM MEMORY AND 256 KB OF RAM^(1,2)

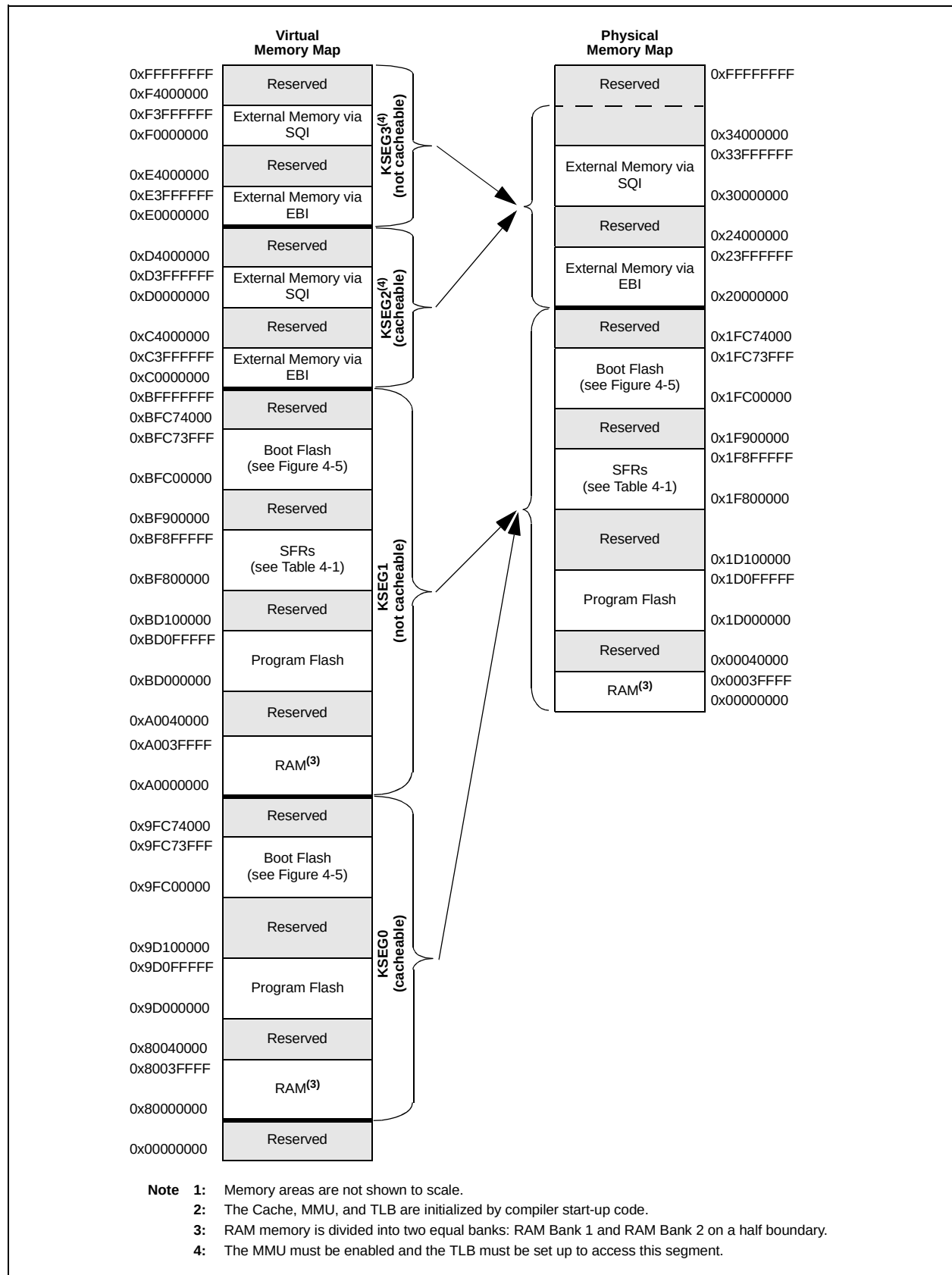


TABLE 4-2: BOOT FLASH 1 SEQUENCE AND CONFIGURATION WORDS SUMMARY

Virtual Address (BFC4_#)	Register Name	Bit Range	Bits																All Reset
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FF40	ABF1DEVCFG3	31:0	Note: See Table 34-2 for the bit descriptions.																XXXX
FF44	ABF1DEVCFG2	31:0																	XXXX
FF48	ABF1DEVCFG1	31:0																	XXXX
FF4C	ABF1DEVCFG0	31:0																	XXXX
FF50	ABF1DEVCP3	31:0																	XXXX
FF54	ABF1DEVCP2	31:0																	XXXX
FF58	ABF1DEVCP1	31:0																	XXXX
FF5C	ABF1DEVCP0	31:0																	XXXX
FF60	ABF1DEVSIGN3	31:0																	XXXX
FF64	ABF1DEVSIGN2	31:0																	XXXX
FF68	ABF1DEVSIGN1	31:0																	XXXX
FF6C	ABF1DEVSIGN0	31:0																	XXXX
FFC0	BF1DEVCFG3	31:0	Note: See Table 34-1 for the bit descriptions.																XXXX
FFC4	BF1DEVCFG2	31:0																	XXXX
FFC8	BF1DEVCFG1	31:0																	XXXX
FFCC	BF1DEVCFG0	31:0																	XXXX
FFD0	BF1DEVCP3	31:0																	XXXX
FFD4	BF1DEVCP2	31:0																	XXXX
FFD8	BF1DEVCP1	31:0																	XXXX
FFDC	BF1DEVCP0	31:0																	XXXX
FFE0	BF1DEVSIGN3	31:0																	XXXX
FFE4	BF1DEVSIGN2	31:0																	XXXX
FFE8	BF1DEVSIGN1	31:0																	XXXX
FFEC	BF1DEVSIGN0	31:0																	XXXX
FFF0	BF1SEQ3	31:16	CSEQ<15:0>																XXXX
		15:0	TSEQ<15:0>																XXXX
FFF4	BF1SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FFF8	BF1SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FFFC	BF1SEQ0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 5-5: NVMDATAx: FLASH DATA REGISTER (x = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **NVMDATA<31:0>**: Flash Data bits

Word Program: Writes NVMDATA0 to the target Flash address defined in NVMADDR

Quad Word Program: Writes NVMDATA3:NVMDATA2:NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR. NVMDATA0 contains the Least Significant Instruction Word.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

REGISTER 5-6: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **NVMSRCADDR<31:0>**: Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3340	USB DPBFD	31:16	—	—	—	—	—	—	—	—	EP7TXD	EP6TXD	EP5TXD	EP4TXD	EP3TXD	EP2TXD	EP1TXD	—	0000
		15:0	—	—	—	—	—	—	—	—	EP7RXD	EP6RXD	EP5RXD	EP4RXD	EP3RXD	EP2RXD	EP1RXD	—	0000
3344	USB TMCON1	31:16	THHSRTN<15:0>																05E6
		15:0	TUCH<15:0>																4074
3348	USB TMCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	THSBT<3:0>				0000
3360	USB LPMR1	31:16	—	—	LPM ERRIE	LPM RESIE	LPMACKIE	LPMNYIE	LPMSTIE	LPMTOIE	—	—	—	LPMNAK ⁽¹⁾ __ ⁽²⁾	LPMEN<1:0> __ ⁽²⁾ __ ⁽²⁾		LPMRES	LPMXMT	0000 0000
		15:0	ENDPOINT<3:0>					—	—	RMTWAK	HIRD<3:0>				LNKSTATE<3:0>				0000
3364	USB LPMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	LPMFADDR<6:0>							—	—	LPMERR ⁽¹⁾ __ ⁽²⁾	LPMRES	LPMNC	LPMACK	LPMNY	LPMST	0000
													0000						

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: Device mode.
 - 2: Host mode.
 - 3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
 - 4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

TABLE 11-2: USB REGISTER MAP 2

Virtual Address (BF88 #)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4000	USB CRCON	31:16	—	—	—	—	—	USBIF	USBRF	USBWKUP	—	—	—	—	—	—	—	—	0100
		15:0	—	—	—	—	—	—	USB IDOVEN	USB IDVAL	PHYIDEN	VBUS MONEN	ASVAL MONEN	BSVAL MONEN	SEND MONEN	USBIE	USBRIE	USB WKUPEN	8000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 12-7: PORTC REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	—	—	—	—	—	F000
0220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUC15	CNPUC14	CNPUC13	CNPUC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
0260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDC15	CNPDC14	CNPDC13	CNPDC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
0270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0280	CNENC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNENC15	CNENC14	CNENC13	CNENC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
0290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATC15	CNSTATC14	CNSTATC13	CNSTATC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
02A0	CNNEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEC15	CNNEC14	CNNEC13	CNNEC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
02B0	CNFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFC15	CNFC14	CNFC13	CNFC12	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

TABLE 12-21: PORTK REGISTER MAP FOR 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0910	TRISK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRISK7	TRISK6	TRISK5	TRISK4	TRISK3	TRISK2	TRISK1	TRISK0	00FF
0920	PORTK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	RK7	RK6	RK5	RK4	RK3	RK2	RK1	RK0	xxxx
0930	LATK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LATK7	LATK6	LATK5	LATK4	LATK3	LATK2	LATK1	LATK0	xxxx
0940	ODCK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ODCK7	ODCK6	ODCK5	ODCK4	ODCK3	ODCK2	ODCK1	ODCK0	0000
0950	CNPUK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPUK7	CNPUK6	CNPUK5	CNPUK4	CNPUK3	CNPUK2	CNPUK1	CNPUK0	0000
0960	CNPDK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPDK7	CNPDK6	CNPDK5	CNPDK4	CNPDK3	CNPDK2	CNPDK1	CNPDK0	0000
0970	CNCONK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0980	CNENK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNENK7	CNENK6	CNENK5	CNENK4	CNENK3	CNENK2	CNENK1	CNENK0	0000
0990	CNSTATK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CN STATK7	CN STATK6	CN STATK5	CN STATK4	CN STATK3	CN STATK2	CN STATK1	CN STATK0	0000
09A0	CNNEK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNNEK7	CNNEK6	CNNEK5	CNNEK4	CNNEK3	CNNEK2	CNNEK1	CNNEK0	0000
09B0	CNFK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNFK7	CNFK6	CNFK5	CNFK4	CNFK3	CNFK2	CNFK1	CNFK0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

The timer source for each Output Compare module depends on the setting of the OCACLK bit in the CFGCON register. The available configurations are shown in Table 18-1.

TABLE 18-1: TIMER SOURCE CONFIGURATIONS

Output Compare Module	Timerx	Timery
OCACLK (CFGCON<16>) = 0		
OC1	Timer2	Timer3
⋮	⋮	⋮
OC9	Timer2	Timer3
OCACLK (CFGCON<16>) = 1		
OC1	Timer4	Timer5
OC2	Timer4	Timer5
OC3	Timer4	Timer5
OC4	Timer2	Timer3
OC5	Timer2	Timer3
OC6	Timer2	Timer3
OC7	Timer6	Timer7
OC8	Timer6	Timer7
OC9	Timer6	Timer7

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 24-5: EBISMCN: EXTERNAL BUS INTERFACE STATIC MEMORY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0
	SMDWIDTH2<2:0>			SMDWIDTH1<2:0>			SMDWIDTH0<2:1>	
7:0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1
	SMDWIDTH0<0>	—	—	—	—	—	—	SMRP

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **SMDWIDTH2<2:0>**: Static Memory Width for Register EBISMT2 bits

111 = Reserved
 110 = Reserved
 101 = Reserved
 100 = 8 bits
 011 = Reserved
 010 = Reserved
 001 = Reserved
 000 = 16 bits

bit 12-10 **SMDWIDTH1<2:0>**: Static Memory Width for Register EBISMT1 bits

111 = Reserved
 110 = Reserved
 101 = Reserved
 100 = 8 bits
 011 = Reserved
 010 = Reserved
 001 = Reserved
 000 = 16 bits

bit 9-7 **SMDWIDTH0<2:0>**: Static Memory Width for Register EBISMT0 bits

111 = Reserved
 110 = Reserved
 101 = Reserved
 100 = 8 bits
 011 = Reserved
 010 = Reserved
 001 = Reserved
 000 = 16 bits

bit 6-1 **Unimplemented:** Read as '0'

bit 0 **SMRP**: Flash Reset/Power-down mode Select bit

After a Reset, the controller internally performs a power-down for Flash, and then sets this bit to '1'.

1 = Flash is taken out of Power-down mode

0 = Flash is forced into Power-down mode

27.0 RANDOM NUMBER GENERATOR (RNG)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 49. “Crypto Engine (CE) and Random Number Generator (RNG)”** (DS60001246) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Random Number Generator (RNG) core implements a thermal noise-based, True Random Number Generator (TRNG) and a cryptographically secure Pseudo-Random Number Generator (PRNG).

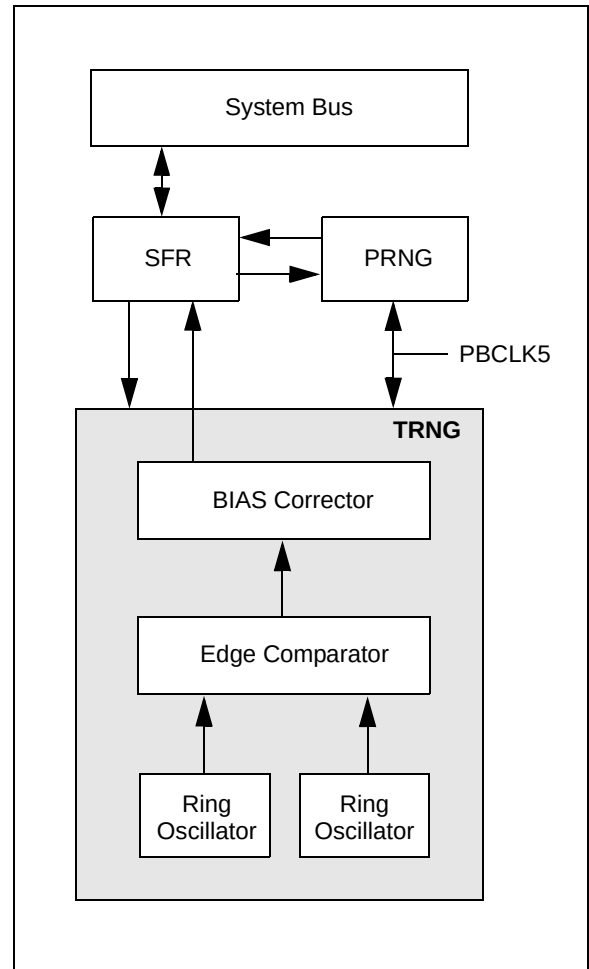
The TRNG uses multiple ring oscillators and the inherent thermal noise of integrated circuits to generate true random numbers that can initialize the PRNG.

The PRNG is a flexible LSFR, which is capable of manifesting a maximal length LFSR of up to 64-bits.

The following are some of the key features of the Random Number Generator:

- TRNG:
 - Up to 25 Mbps of random bits
 - Multi-Ring Oscillator based design
 - Built-in Bias Corrector
- PRNG:
 - LSFR-based
 - Up to 64-bit polynomial length
 - Programmable polynomial
 - TRNG can be seed value

TABLE 27-1: RANDOM NUMBER GENERATOR BLOCK DIAGRAM



REGISTER 29-3: CiINT: CAN INTERRUPT REGISTER (CONTINUED)

- bit 14 **WAKIF:** CAN Bus Activity Wake-up Interrupt Flag bit
1 = A bus wake-up activity interrupt has occurred
0 = A bus wake-up activity interrupt has not occurred
- bit 13 **CERRIF:** CAN Bus Error Interrupt Flag bit
1 = A CAN bus error has occurred
0 = A CAN bus error has not occurred
- bit 12 **SERRIF:** System Error Interrupt Flag bit
1 = A system error occurred (typically an illegal address was presented to the System Bus)
0 = A system error has not occurred
- bit 11 **RBOVIF:** Receive Buffer Overflow Interrupt Flag bit
1 = A receive buffer overflow has occurred
0 = A receive buffer overflow has not occurred
- bit 10-4 **Unimplemented:** Read as '0'
- bit 3 **MODIF:** CAN Mode Change Interrupt Flag bit
1 = A CAN module mode change has occurred (OPMOD<2:0> has changed to reflect REQOP)
0 = A CAN module mode change has not occurred
- bit 2 **CTMRIF:** CAN Timer Overflow Interrupt Flag bit
1 = A CAN timer (CANTMR) overflow has occurred
0 = A CAN timer (CANTMR) overflow has not occurred
- bit 1 **RBIF:** Receive Buffer Interrupt Flag bit
1 = A receive buffer interrupt is pending
0 = A receive buffer interrupt is not pending
- bit 0 **TBIF:** Transmit Buffer Interrupt Flag bit
1 = A transmit buffer interrupt is pending
0 = A transmit buffer interrupt is not pending

Note 1: This bit can only be cleared by turning the CAN module off and on by clearing or setting the ON bit (CiCON<15>).

REGISTER 30-1: ETHCON1: ETHERNET CONTROLLER CONTROL REGISTER 1 (CONTINUED)

bit 7 **AUTOFC:** Automatic Flow Control bit

1 = Automatic Flow Control enabled
0 = Automatic Flow Control disabled

Setting this bit will enable automatic Flow Control. If set, the full and empty watermarks are used to automatically enable and disable the Flow Control, respectively. When the number of received buffers BUFCNT (ETHSTAT<16:23>) rises to the full watermark, Flow Control is automatically enabled. When the BUFCNT falls to the empty watermark, Flow Control is automatically disabled.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **MANFC:** Manual Flow Control bit

1 = Manual Flow Control is enabled
0 = Manual Flow Control is disabled

Setting this bit will enable manual Flow Control. If set, the Flow Control logic will send a PAUSE frame using the PAUSE timer value in the PTV register. It will then resend a PAUSE frame every $128 * PTV < 15:0 > / 2$ TX clock cycles until the bit is cleared.

Note: For 10 Mbps operation, TX clock runs at 2.5 MHz. For 100 Mbps operation, TX clock runs at 25 MHz.

When this bit is cleared, the Flow Control logic will automatically send a PAUSE frame with a 0x0000 PAUSE timer value to disable Flow Control.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **BUFCDEC:** Descriptor Buffer Count Decrement bit

The BUFCDEC bit is a write-1 bit that reads as '0'. When written with a '1', the Descriptor Buffer Counter, BUFCNT, will decrement by one. If BUFCNT is incremented by the RX logic at the same time that this bit is written, the BUFCNT value will remain unchanged. Writing a '0' will have no effect.

This bit is only used for RX operations.

Note 1: It is not recommended to clear the RXEN bit and then make changes to any RX related field/register. The Ethernet Controller must be reinitialized (ON cleared to '0'), and then the RX changes applied.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 34-1: DEVSIGN0/ADEVSIGN0: DEVICE SIGNATURE WORD 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —
23:16	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —
15:8	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —
7:0	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —

Legend: r = Reserved bit
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31 **Reserved:** Write as '0'

bit 30-0 **Reserved:** Write as '1'

Note: The DEVSIGN1 through DEVSIGN3 and ADEVSIGN1 through ADEVSIGN3 registers are used for Quad Word programming operation when programming the DEVSIGN0/ADEVSIGN0 registers, and do not contain any valid information.

REGISTER 34-2: DEVCP0/ADEVCP0: DEVICE CODE-PROTECT 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1 —	r-1 —	r-1 —	R/P CP	r-1 —	r-1 —	r-1 —	r-1 —
23:16	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —
15:8	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —
7:0	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —

Legend: r = Reserved bit P = Programmable bit
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-29 **Reserved:** Write as '1'

bit 28 **CP:** Code-Protect bit

Prevents boot and program Flash memory from being read or modified by an external programming device.

1 = Protection is disabled

0 = Protection is enabled

bit 27-0 **Reserved:** Write as '1'

Note: The DEVCP1 through DEVCP3 and ADEVCP1 through ADEVCP3 registers are used for Quad Word programming operation when programming the DEVCP0/ADEVCP0 registers, and do not contain any valid information.

37.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MZ EF device AC characteristics and timing parameters.

FIGURE 37-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

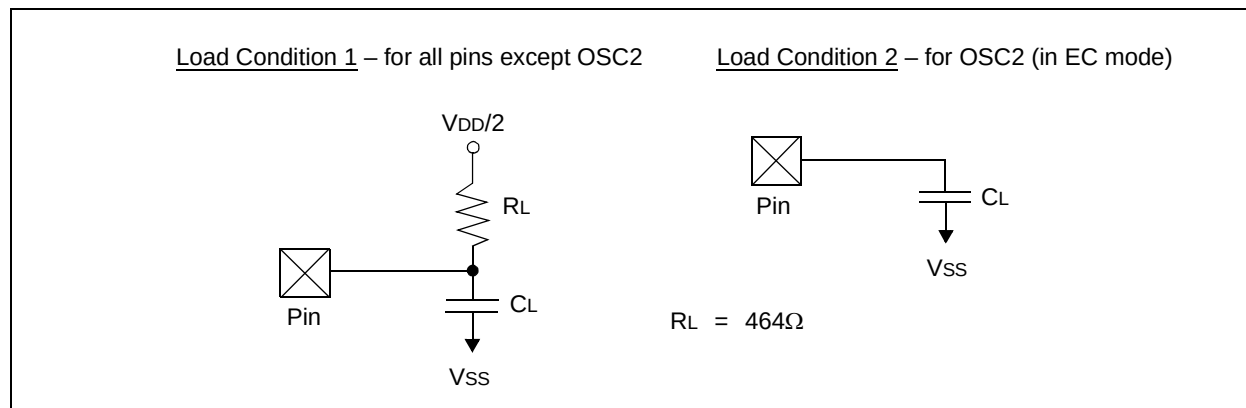


TABLE 37-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

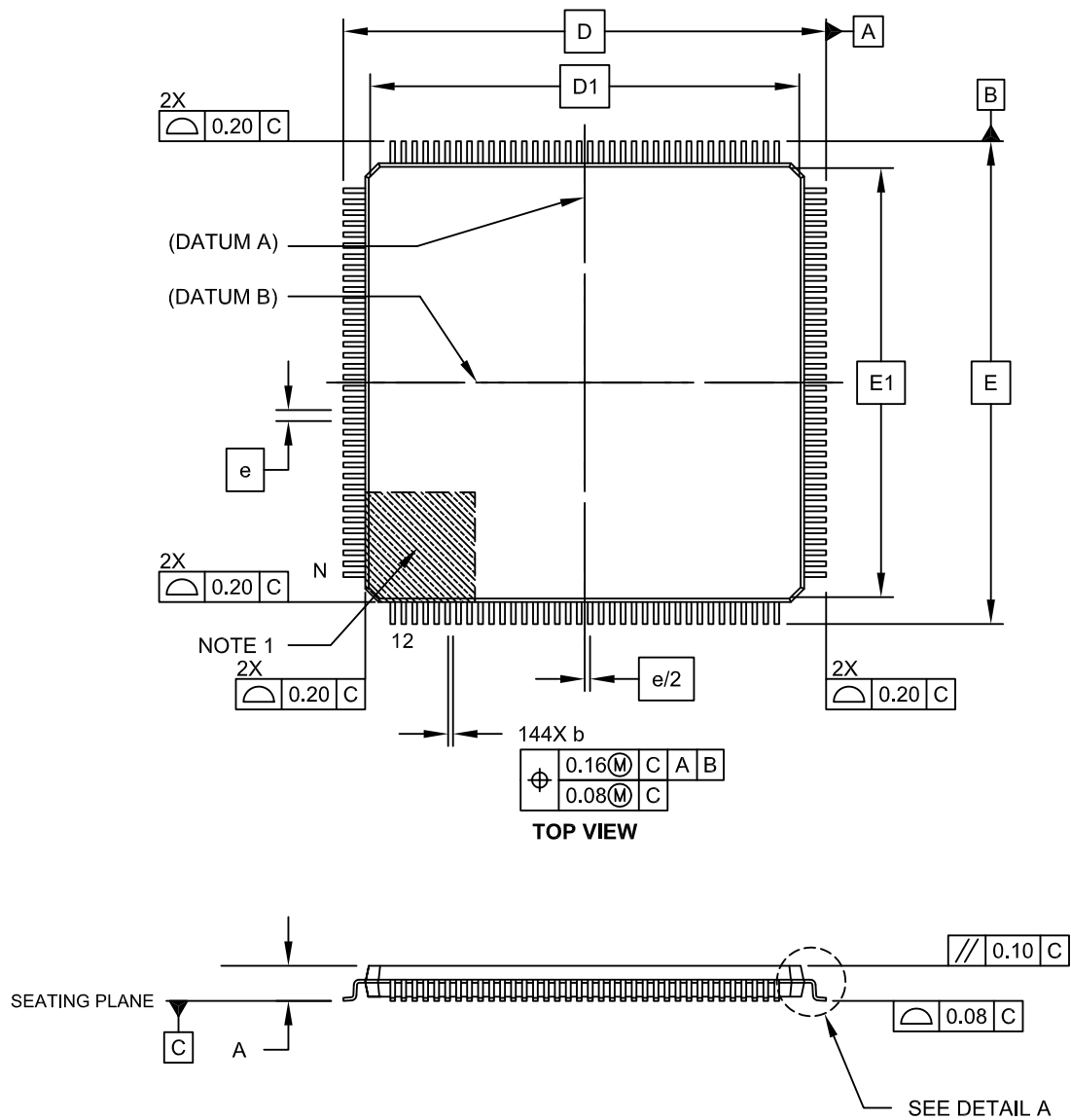
AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
DO56	CL	All I/O pins (except pins used as CxOUT)	—	—	50	pF	EC mode for OSC2
DO58	Cb	SCLx, SDAx	—	—	400	pF	In I ² C mode
DO59	CsQI	All SQI pins	—	—	10	pF	—

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

144-Lead Plastic Low Profile Quad Flatpack (PL) – 20x20x1.40 mm Body, with 2.00 mm Footprint [LQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-044B Sheet 1 of 2

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

B.6 Resets

On PIC32MZ EF devices, the Reset module adds eight bits to the NMICNT field to make the time-out period before device Reset longer, as described in Table B-5.

TABLE B-5: RESETS DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
Countdown to Reset During NMIs	
On PIC32MZ EC devices, the NMICNT<7:0> field is eight bits long, giving a maximum of 256 instructions before the device Reset.	On PIC32MZ EF devices, the NMICNT<15:0> field is now 16 bits long, giving a longer period of time (up to 65,536 instructions) prior to a device Reset.

B.7 USB

On PIC32MZ EF devices, a new USBRCRCON register has been added to assist in controlling the reset of the USB module, and triggering interrupts based on VBUS voltage levels. This register also overcomes an errata on PIC32MZ EC devices that requires a three second start-up on the USB module.

B.8 I/O Ports

On PIC32MZ EF devices, many of the I/O pins now feature slew rate control bits to control how fast the pin makes a low-to-high or high-to-low transition. The Change Notification feature has also been enhanced to allow detection of level events in addition to edge detection. However, the SIDL bit is not present in the CNCONx registers on PIC32MZ EF devices, as it is on PIC32MZ EC devices.

B.9 Watchdog Timer

PIC32MZ EF devices use a new Watchdog Timer, although the overall control through the DEVCFGx words remains identical to that of PIC32MZ EC devices. Table B-6 lists two more changes, as well.

TABLE B-6: WATCHDOG TIMER DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
Watchdog Timer Postscaler	
On PIC32MZ EC devices, the SWDTPS<4:0> bits (WDTCON<6:2>) reflect the postscaler setting for the Watchdog Timer.	On PIC32MZ EF devices, the field has been changed to the RUNDIV<4:0> bits (WDTCON<12:8>).
Watchdog Windowed Mode	
On PIC32MZ EC devices, WDTWINEN is at bit position 1 (WDTCON<1>).	On PIC32MZ EF devices, WDTWINEN is now at bit position 0 (WDTCON<0>).

INDEX

A

AC Characteristics	624, 667, 673
ADC Specifications	650
Analog-to-Digital Conversion Requirements	651
EJTAG Timing Requirements	662
Ethernet	658
Internal BFRC Accuracy	627
Internal FRC Accuracy	627
Internal LPRC Accuracy	627
Parallel Master Port Read Requirements	655
Parallel Master Port Write	656
Parallel Master Port Write Requirements	656
Parallel Slave Port Requirements	654
PLL Clock Timing	626, 667, 673
USB OTG Electrical Specifications	657
Assembler	
MPASM Assembler	608

B

Block Diagrams	
Comparator I/O Operating Modes	567
Comparator Voltage Reference	571
CPU	44
Crypto Engine	401
DMA	173
EBI System	383
Ethernet Controller	523
I2C	354
Input Capture	305
Interrupt Controller	115
JTAG Programming, Debugging and Trace Ports	603
Output Compare Module	309
PIC32 CAN Module	485
PMP Pinout and Connections to External Devices	369
Prefetch Module	169
Random Number Generator (RNG)	421
RTCC	391
Serial Quad Interface (SQI)	325
SPI/I2S Module	315
System Reset	109
Timer1	283
Timer2-Timer9 (16-Bit)	287
Typical Multiplexed Port Structure	247
UART	361
WDT	301
Brown-out Reset (BOR)	
and On-Chip Voltage Regulator	603

C

C Compilers	
MPLAB	608
Comparator	
Specifications	623
Comparator Module	567
Comparator Voltage Reference (CVref)	571
Configuration Bits	581
Configuring Analog Port Pins	248
Controller Area Network (CAN)	485
CPU	
Architecture Overview	45
Coprocesor 0 Registers	46
Core Exception Types	116

EJTAG Debug Support	50
Power Management	49
CPU Module	43
Crypto	
Buffer Descriptors	412
Format of BD_CTRL	413
Format of BD_DSTADDR	414
Format of BD_ENC_OFF	415
Format of BD_MSG_LEN	415
Format of BD_NXTADDR	414
Format of BD_SADDR	413
Format of BD_SRCADDR	414
Format of BD_UPDPTR	415
Format of SA_CTRL	419
Security Association Structure	416
Crypto Engine	401
Customer Change Notification Service	733
Customer Notification Service	733
Customer Support	733

D

DC Characteristics	612, 664, 670
I/O Pin Input Specifications	617, 618
I/O Pin Output Specifications	619
Idle Current (I _{IDLE})	615, 665, 671
Power-Down Current (I _{PD})	616, 666
Program Flash Memory Wait States	622, 672
Program Memory	622
Temperature and Voltage Specifications	613
Development Support	607
Direct Memory Access (DMA) Controller	173

E

Electrical Characteristics	611, 663, 669
Errata	12
Ethernet Controller	523
External Bus Interface (EBI)	383
External Clock	
Timer1 Timing Requirements	633
Timer2-Timer9 Timing Requirements	634
Timing Requirements	625

F

Flash Program Memory	99
----------------------------	----

G

Getting Started	37
-----------------------	----

H

Hi-Speed USB On-The-Go (OTG)	197
------------------------------------	-----

I

I/O Ports	247
Parallel I/O (PIO)	248
Write/Read Timing	248
Input Change Notification	248
Instruction Set	605
Inter-Integrated Circuit (I2C)	353
Internet Address	733
Interrupt Controller	
IRG, Vector and Bit Location	118

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

ADCCMPx (ADC Digital Comparator 'x' Limit Value Register ('x' = 1 through 6)).....	461
ADCCMPxCON (ADC Digital Comparator 'x' Control Register ('x' = 1 through 6)).....	469
ADCCON1 (ADC Control Register 1).....	437
ADCCON2 (ADC Control Register 2).....	440
ADCCON3 (ADC Control Register 3).....	442
ADCCSS1 (ADC Common Scan Select Register 1).....	457
ADCCSS2 (ADC Common Scan Select Register 2).....	458
ADCDATAx (ADC Output Data Register ('x' = 0 through 44)).....	474
ADCDSTAT1 (ADC Data Ready Status Register 1).....	459
ADCDSTAT2 (ADC Data Ready Status Register 2).....	459
ADCEIEN1 (ADC Early Interrupt Enable Register 1).....	477
ADCEIEN2 (ADC Early Interrupt Enable Register 2).....	477
ADCEISTAT2 (ADC Early Interrupt Status Register 2).....	479
ADCFLTRx (ADC Digital Filter 'x' Register ('x' = 1 through 6)).....	462
ADCGIRQEN1 (ADC Interrupt Enable Register 1).....	456
ADCIMCON1 (ADC Input Mode Control Register 1).....	447
ADCIMCON2 (ADC Input Mode Control Register 2).....	450
ADCIMCON3 (ADC Input Mode Control Register 3).....	453
ADCIRQEN2 (ADC Interrupt Enable Register 2).....	456
ADCSYSCFG1 (ADC System Configuration Register 1).....	483
ADCSYSCFG2 (ADC System Configuration Register 2).....	483
ADCTRG1 (ADC Trigger Source 1 Register).....	464
ADCTRG2 (ADC Trigger Source 2 Register).....	465
ADCTRG3 (ADC Trigger Source 3 Register).....	466
ADCTRGMODE (ADC Triggering Mode for Dedicated ADC).....	445
ADCTRGSNS (ADC Trigger Level/Edge Sensitivity).....	475
ADCxCFG (ADCx Configuration Register 'x' ('x' = 1 through 6)).....	482
ADCxTIME (Dedicated ADCx Timing Register 'x' ('x' = 0 through 4)).....	476
ALRMTIME (Alarm Time Value).....	399
BFXSEQ3/ABFXSEQ3 (Boot Flash 'x' Sequence Word 3 Register).....	70
CEBDADDR (Crypto Engine Buffer Descriptor).....	405
CEBDPADDR (Crypto Engine Buffer Descriptor Processor).....	405
CECON (Crypto Engine Control).....	404
CEHDLEN (Crypto Engine Header Length).....	411
CEINTEN (Crypto Engine Interrupt Enable).....	409
CEINTSRC (Crypto Engine Interrupt Source).....	408
CEPOLLCON (Crypto Engine Poll Control).....	410
CESTAT (Crypto Engine Status).....	406
CETRLLEN (Crypto Engine Trailer Length).....	411
CEVER (Crypto Engine Revision, Version, and ID).....	403
CFGEBIA (External Bus Interface Address Pin Configuration).....	597
CFGEBIC (External Bus Interface Control Pin Configuration).....	598
CFGPG (Permission Group Configuration).....	600
CiCFG (CAN Baud Rate Configuration).....	492
CiCON (CAN Module Control).....	490
CiFIFOBA (CAN Message Buffer Base Address).....	517
CiFIFOIn (CAN Module Message Index Register 'n' ('n' = 0-31)).....	522
CiFIFOCONn (CAN FIFO Control Register 'n' ('n' = 0-31)).....	518
CiFIFOINTn (CAN FIFO Interrupt Register 'n' ('n' = 0-31)).....	520
CiFIFOUn (CAN FIFO User Address Register 'n' ('n' = 0-31)).....	522
CiFLTCON0 (CAN Filter Control Register 0).....	500
CiFLTCON1 (CAN Filter Control Register 1).....	502
CiFLTCON2 (CAN Filter Control Register 2).....	504
CiFLTCON3 (CAN Filter Control Register 3).....	506
CiFLTCON4 (CAN Filter Control Register 4).....	508
CiFLTCON5 (CAN Filter Control Register 5).....	510
CiFLTCON6 (CAN Filter Control Register 6).....	512
CiFLTCON7 (CAN Filter Control Register 7).....	514
CiFSTAT (CAN FIFO Status).....	497
CiRXFn (CAN Acceptance Filter 'n' Register 7 ('n' = 0-31)).....	516
CiRXMn (CAN Acceptance Filter Mask 'n' Register ('n' = 0-3)).....	499
CiRXOVF (CAN Receive FIFO Overflow Status).....	498
CiTMR (CAN Timer).....	498
CiTREC (CAN Transmit/Receive Error Count).....	497
CiVEC (CAN Interrupt Code).....	496
CMSTAT (Comparator Control Register).....	570
CMxCON (Comparator Control).....	569
CNCONx (Change Notice Control for PORTx).....	282
CONFIG (Configuration Register - CP0 Register 16, Select 0).....	51
CONFIG1 (Configuration Register 1 - CP0 Register 16, Select 1).....	52
CONFIG3 (Configuration Register 3 - CP0 Register 16, Select 3).....	53
CONFIG5 (Configuration Register 5 - CP0 Register 16, Select 5).....	54
CONFIG7 (Configuration Register 7 - CP0 Register 16, Select 7).....	54
CVRCON (Comparator Voltage Reference Control).....	573
DCHxCON (DMA Channel x Control).....	186
DCHxCPTR (DMA Channel x Cell Pointer).....	194
DCHxCsIZ (DMA Channel x Cell-Size).....	194
DCHxDAT (DMA Channel x Pattern Data).....	195
DCHxDPTR (Channel x Destination Pointer).....	193
DCHxDSA (DMA Channel x Destination Start Address).....	191
DCHxDsIZ (DMA Channel x Destination Size).....	192
DCHxECON (DMA Channel x Event Control).....	188
DCHxINT (DMA Channel x Interrupt Control).....	189
DCHxSPTR (DMA Channel x Source Pointer).....	193
DCHxSSA (DMA Channel x Source Start Address).....	191
DCHxSSIZ (DMA Channel x Source Size).....	192
DCRCCON (DMA CRC Control).....	183
DCRCDATA (DMA CRC Data).....	185
DCRCXOR (DMA CRCXOR Enable).....	185
DEVCFG0/ADEVCFG0 (Device Configuration Word 0).....	587
DEVCFG1/ADEVCFG1 (Device Configuration Word 1).....	589
DEVCFG2/ADEVCFG2 (Device Configuration Word 2).....	592
DEVCFG3/ADEVCFG3 (Device Configuration Word 3).....	594
DEVCP0/ADEVCP0 (Device Code-Protect 0).....	586
DEVID (Device and Revision ID).....	601
DEVSIGN0/ADEVSIGN0 (Device Signature Word 0).....	586
DMAADDR (DMA Address).....	182
DMACON (DMA Controller Control).....	181
DMASTAT (DMA Status).....	182