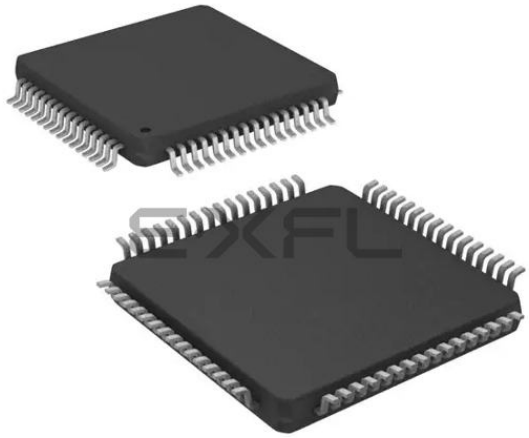
Microchip Technology - PIC32MZ1024EFH064-I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	46
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efh064-i-pt

REGISTER 11-1: USBCSR0: USB CONTROL STATUS REGISTER 0 (CONTINUED)

bit 10 **RESUME:** Resume from Suspend control bit
1 = Generate Resume signaling when the device is in Suspend mode
0 = Stop Resume signaling

In *Device mode*, the software should clear this bit after 10 ms (a maximum of 15 ms) to end Resume signaling. In *Host mode*, the software should clear this bit after 20 ms.

bit 9 **SUSPMODE:** Suspend Mode status bit
1 = The USB module is in Suspend mode
0 = The USB module is in Normal operations

This bit is read-only in Device mode. In Host mode, it can be set by software, and is cleared by hardware.

bit 8 **SUSPEN:** Suspend Mode Enable bit
1 = Suspend mode is enabled
0 = Suspend mode is not enabled

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **FUNC<6:0>:** Device Function Address bits

These bits are only available in *Device mode*. This field is written with the address received through a SET_ADDRESS command, which will then be used for decoding the function address in subsequent token packets.

REGISTER 11-15: USBHWVER: USB HARDWARE VERSION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-1	R-0	R-0	R-0
	RC	VERMAJOR<4:0>					VERMINOR<9:8>	
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERMINOR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **RC:** Release Candidate bit
1 = USB module was created using a release candidate
0 = USB module was created using a full release

bit 14-10 **VERMAJOR<4:0>:** USB Module Major Version number bits
This read-only number is the Major version number for the USB module.

bit 9-0 **VERMINOR<9:0>:** USB Module Minor Version number bits
This read-only number is the Minor version number for the USB module.

REGISTER 11-29: USBLPMR2: USB LINK POWER MANAGEMENT CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	LPMFADDR<6:0>						
7:0	U-0	U-0	R-0	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS
	—	—	LPMERRIF	LPMRESIF	LPMNCIF	LPMACKIF	LPMNYIF	LPMSTIF

Legend:	HS = Hardware Set		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14-8 **LPMFADDR<6:0>:** LPM Payload Function Address bits
These bits contain the address of the LPM payload function.

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **LPMERRIF:** LPM Error Interrupt Flag bit (*Device mode*)
1 = An LPM transaction was received that had a LINKSTATE field that is not supported. The response will be a STALL.
0 = No error condition

bit 4 **LPMRESIF:** LPM Resume Interrupt Flag bit
1 = The USB module has resumed (for any reason)
0 = No Resume condition

bit 3 **LPMNCIF:** LPM NC Interrupt Flag bit
When in *Device mode*:
1 = The USB module received a LPM transaction and responded with a NYET due to data pending in the RX FIFOs.
0 = No NC interrupt condition

When in *Host mode*:
1 = A LPM transaction is transmitted and the device responded with an ACK
0 = No NC interrupt condition

bit 2 **LPMACKIF:** LPM ACK Interrupt Flag bit
When in *Device mode*:
1 = A LPM transaction was received and the USB Module responded with an ACK
0 = No ACK interrupt condition

When in *Host mode*:
1 = The LPM transaction is transmitted and the device responds with an ACK
0 = No ACK interrupt condition

bit 1 **LPMNYIF:** LPM NYET Interrupt Flag bit
When in *Device mode*:
1 = A LPM transaction is received and the USB Module responded with a NYET
0 = No NYET interrupt flag

When in *Host mode*:
1 = A LPM transaction is transmitted and the device responded with an NYET
0 = No NYET interrupt flag

TABLE 12-11: PORTE REGISTER MAP FOR 100-PIN, 124-PIN, AND 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0400	ANSELE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSE9	ANSE8	ANSE7	ANSE6	ANSE5	ANSE4	—	—	—	—	03F0
0410	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISE9	TRISE8	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	03FF
0420	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
0430	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATE9	LATE8	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
0440	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCE9	ODCE8	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000
0450	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUE9	CNPUE8	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPUE3	CNPUE2	CNPUE1	CNPUE0	0000
0460	CNPDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDE9	CNPDE8	CNPDE7	CNPDE6	CNPDE5	CNPDE4	CNPDE3	CNPDE2	CNPDE1	CNPDE0	0000
0470	CNCONE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0480	CNENE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNENE9	CNENE8	CNENE7	CNENE6	CNENE5	CNENE4	CNENE3	CNENE2	CNENE1	CNENE0	0000
0490	CNSTATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CN STATE9	CN STATE8	CN STATE7	CN STATE6	CN STATE5	CN STATE4	CN STATE3	CN STATE2	CN STATE1	CN STATE0	0000
04A0	CNNEE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNNEE9	CNNEE8	CNNEE7	CNNEE6	CNNEE5	CNNEE4	CNNEE3	CNNEE2	CNNEE1	CNNEE0	0000
04B0	CNFE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNFE9	CNFE8	CNFE7	CNFE6	CNFE5	CNFE4	CNFE3	CNFE2	CNFE1	CNFE0	0000
04C0	SRCON0E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR0E3	SR0E2	SR0E1	SR0E0	0000
04D0	SRCON1E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR1E3	SR1E2	SR1E1	SR1E0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

13.0 TIMER1

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MZ EF devices feature one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the Low-Power Secondary Oscillator (SOSC) for real-time clock applications.

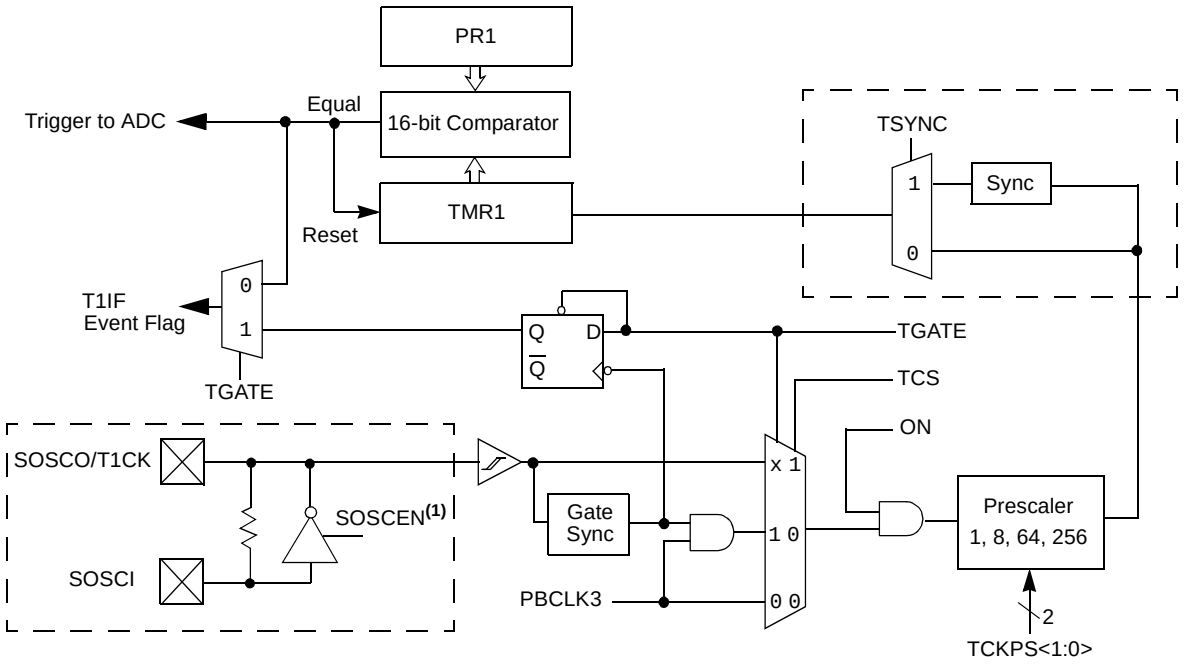
The following modes are supported by Timer1:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

13.1 Additional Supported Features

- Selectable clock prescaler
- Timer operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the SOSC to function as a real-time clock
- ADC event trigger

FIGURE 13-1: TIMER1 BLOCK DIAGRAM



Note 1: The default state of the SOSCEN bit (OSCCON<1>) during a device Reset is controlled by the FSOSCEN bit in Configuration Word, DEVCFG1.

REGISTER 15-5: DMTCNT: DEADMAN TIMER COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **COUNTER<31:0>:** Read current contents of DMT counter

REGISTER 15-6: DMTPSCNT: POST STATUS CONFIGURE DMT COUNT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<15:8>							
7:0	R-0	R-0	R-0	R-y	R-y	R-y	R-y	R-y
	PSCNT<7:0>							

Legend:		y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **PSCNT<31:0>:** DMT Instruction Count Value Configuration Status bits
This is always the value of the DMTCNT<4:0> bits in the DEVCFG1 Configuration register.

REGISTER 20-24: SQI1MEMSTAT: SQI MEMORY STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	STATPOS	STATTYPE<1:0>		STATBYTES<1:0>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STATDATA<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STATCMD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **STATPOS:** Status Bit Position in Flash bit
Indicates the BUSY bit position in the Flash Status register. This bit is added to support all Flash types (with BUSY bit at 0 and at 7).
1 = BUSY bit position is bit 7 in status register
0 = BUSY bit position is bit 0 in status register

bit 19-18 **STATTYPE<1:0>:** Status Command/Read Lane Mode bits
11 = Reserved
10 = Status command and read are executed in Quad Lane mode
01 = Status command and read are executed in Dual Lane mode
00 = Status command and read are executed in Single Lane mode

bit 17-16 **STATBYTES<1:0>:** Number of Status Bytes bits
11 = Reserved
10 = Status command/read is 2 bytes long
01 = Status command/read is 1 byte long
00 = Reserved

bit 15-8 **STATDATA<7:0>:** Status Data bits
These bits contain the status value of the Flash device

bit 7-0 **STATCMD<7:0>:** Status Command bits
The status check command is written into these bits

REGISTER 26-7: CEINTEN: CRYPTO ENGINE INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	AREIE	PKTIE	BDPIE	PENDIE(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **AREIE:** Access Response Error Interrupt Enable bit
- 1 = Access response error interrupts are enabled
- 0 = Access response error interrupts are not enabled

bit 2 **PKTIE:** DMA Packet Completion Interrupt Enable bit
- 1 = DMA packet completion interrupts are enabled
- 0 = DMA packet completion interrupts are not enabled

bit 1 **BDPIE:** DMA Buffer Descriptor Processor Interrupt Enable bit
- 1 = BDP interrupts are enabled
- 0 = BDP interrupts are not enabled

bit 0 **PENDIE:** Master Interrupt Enable bit(1)
- 1 = Crypto Engine interrupts are enabled
- 0 = Crypto Engine interrupts are not enabled

Note 1: The PENDIE bit is a global enable bit and must be enabled together with the other interrupts desired.

REGISTER 29-1: CiCON: CAN MODULE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	S/HC-0	R/W-1	R/W-0	R/W-0
	—	—	—	—	ABAT	REQOP<2:0>		
23:16	R-1	R-0	R-0	R/W-0	U-0	U-0	U-0	U-0
	OPMOD<2:0>			CANCAP	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R-0	U-0	U-0	U-0
	ON(1)	—	SIDLE	—	CANBUSY	—	—	—
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DNCNT<4:0>				

Legend:	HC = Hardware Clear	S = Settable bit	
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-28 **Unimplemented:** Read as ‘0’

bit 27 **ABAT:** Abort All Pending Transmissions bit
1 = Signal all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions aborted

bit 26-24 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved - Do not use
101 = Reserved - Do not use
100 = Set Configuration mode
011 = Set Listen Only mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode

bit 23-21 **OPMOD<2:0>:** Operation Mode Status bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 20 **CANCAP:** CAN Message Receive Time Stamp Timer Capture Enable bit
1 = CANTMR value is stored on valid message reception and is stored with the message
0 = Disable CAN message receive time stamp timer capture and stop CANTMR to conserve power

bit 19-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** CAN On bit(1)
1 = CAN module is enabled
0 = CAN module is disabled

bit 14 **Unimplemented:** Read as ‘0’

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

REGISTER 30-5: ETHHT0: ETHERNET CONTROLLER HASH TABLE 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **HT<31:0>:** Hash Table Bytes 0-3 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the HTEN bit (ETHRXFC<15>) = 0.

REGISTER 30-6: ETHHT1: ETHERNET CONTROLLER HASH TABLE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<63:56>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<55:48>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<47:40>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<39:32>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **HT<63:32>:** Hash Table Bytes 4-7 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the HTEN bit (ETHRXFC<15>) = 0.

REGISTER 30-37: EMAC1SA0: ETHERNET CONTROLLER MAC STATION ADDRESS 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR6<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR5<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STNADDR6<7:0>:** Station Address Octet 6 bits
These bits hold the sixth transmitted octet of the station address.

bit 7-0 **STNADDR5<7:0>:** Station Address Octet 5 bits
These bits hold the fifth transmitted octet of the station address.

Note 1: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

2: This register is loaded at reset from the factory preprogrammed station address.

31.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

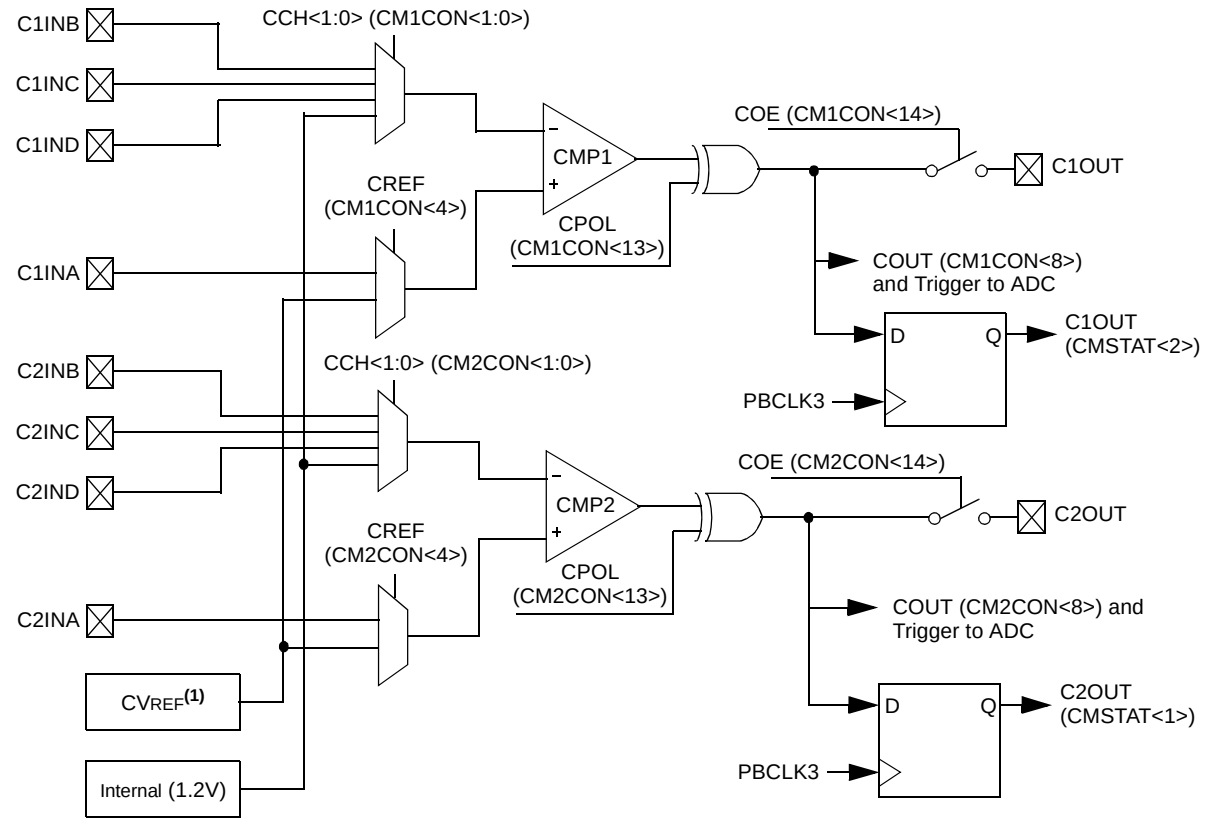
The Analog Comparator module consists of two comparators that can be configured in a variety of ways.

The following are key features of the Analog Comparator module:

- Differential inputs
- Rail-to-rail operation
- Selectable output polarity
- Selectable inputs:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference
  - Comparator voltage reference (CVREF)
- Selectable interrupt generation

A block diagram of the comparator module is illustrated in Figure 31-1.

FIGURE 31-1: COMPARATOR BLOCK DIAGRAM



Note 1: Internally connected. See **Section 32.0 "Comparator Voltage Reference (CVREF)"** for more information.

REGISTER 34-9: CFGEBIC: EXTERNAL BUS INTERFACE CONTROL PIN CONFIGURATION REGISTER (CONTINUED)

bit 12 **EBIOEEN:** $\overline{\text{EBIOE}}$ Pin Enable bit
1 = $\overline{\text{EBIOE}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIOE}}$ pin is available for general use

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **EBIBSEN1:** $\overline{\text{EBIBS1}}$ Pin Enable bit
1 = $\overline{\text{EBIBS1}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIBS1}}$ pin is available for general use

bit 8 **EBIBSEN1:** $\overline{\text{EBIBS0}}$ Pin Enable bit
1 = $\overline{\text{EBIBS0}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIBS0}}$ pin is available for general use

bit 7 **EBICSEN3:** $\overline{\text{EBICS3}}$ Pin Enable bit
1 = $\overline{\text{EBICS3}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS3}}$ pin is available for general use

bit 6 **EBICSEN2:** $\overline{\text{EBICS2}}$ Pin Enable bit
1 = $\overline{\text{EBICS2}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS2}}$ pin is available for general use

bit 5 **EBICSEN1:** $\overline{\text{EBICS1}}$ Pin Enable bit
1 = $\overline{\text{EBICS1}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS1}}$ pin is available for general use

bit 4 **EBICSEN0:** $\overline{\text{EBICS0}}$ Pin Enable bit
1 = $\overline{\text{EBICS0}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS0}}$ pin is available for general use

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **EBIDEN1:** EBI Data Upper Byte Pin Enable bit
1 = EBID<15:8> pins are enabled for use by the EBI module
0 = EBID<15:8> pins have reverted to general use

bit 0 **EBIDEN0:** EBI Data Lower Byte Pin Enable bit
1 = EBID<7:0> pins are enabled for use by the EBI module
0 = EBID<7:0> pins have reverted to general use

Note: When EBIMD = 1, the bits in this register are ignored and the pins are available for general use.

TABLE 37-10: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
DI60a	IICL	**Input Low Injection Current**	0	—	-5(2,5)	mA	This parameter applies to all pins, with the exception of RB10. Maximum IICH current for this exception is 0 mA.
DI60b	IICH	**Input High Injection Current**	0	—	+5(3,4,5)	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, OSCI, OSCO, SOSCI, SOSCO, D+, D- and RB10. Maximum IICH current for these exceptions is 0 mA.
DI60c	∑IICT	**Total Input Injection Current (sum of all I/O and control pins)**	-20(6)	—	+20(6)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL + | IICH |) ≤ ∑IICT

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: VIL source < (VSS - 0.3). Characterized but not tested.

3: VIH source > (VDD + 0.3) for non-5V tolerant pins only.

4: Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any “positive” input injection current.

5: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

6: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. If **Note 2**, IICL = (((Vss - 0.3) - VIL source) / Rs). If **Note 3**, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

TABLE 37-34: SQI TIMING REQUIREMENTS

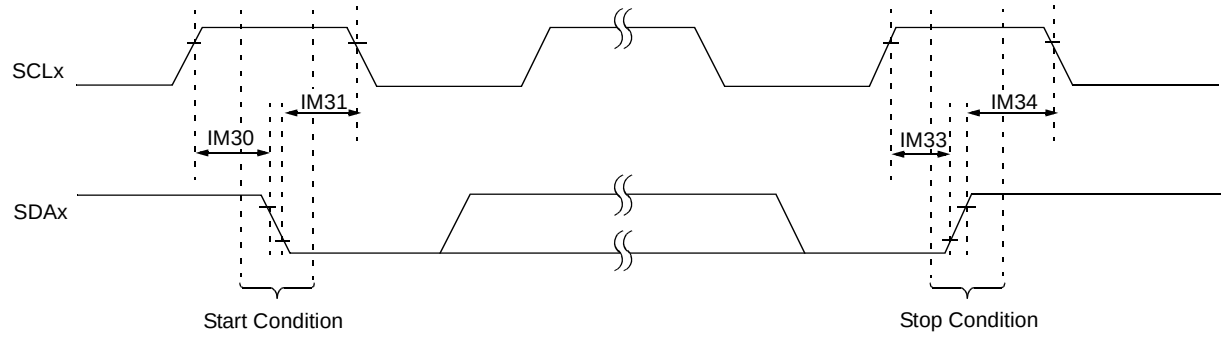
AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristic(1,3)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SQ10	FCLK	Serial Clock Frequency (1/TSQI)	—	66	—	MHz	DMA mode Read, SPI mode 0
			—	33	—	MHz	DMA mode Read, SPI mode 3
			—	100	—	MHz	PIO mode Write
SQ11	TSCKH	Serial Clock High Time	5	—	—	ns	—
SQ12	TSCKL	Serial Clock Low Time	5	—	—	ns	—
SQ13	TSCKR	Serial Clock Rise Time	—	—	—	ns	See parameter DO31
SQ14	TSCKF	Serial Clock Fall Time	—	—	—	ns	See parameter DO32
SQ15	TCSS (TCES)	$\overline{CS}$ Active Setup Time	5	—	—	ns	—
SQ16	TCSH (TCEH)	$\overline{CS}$ Active Hold Time	5	—	—	ns	—
SQ17	TCHS	$\overline{CS}$ Not Active Setup Time	3	—	—	ns	—
SQ18	TCHH	$\overline{CS}$ Not Active Hold Time	3	—	—	ns	—
SQ22	TDIS	Data In Setup Time	6	—	—	ns	—
SQ23	TDIH	Data In Hold Time	3	—	—	ns	—
SQ24	TDOH	Data Out Hold	0	—	—	ns	—
SQ25	TDOV	Data Out Valid	—	—	6	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the Typical column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SQIx pins

FIGURE 37-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 37-1 for load conditions.

FIGURE 37-17: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)

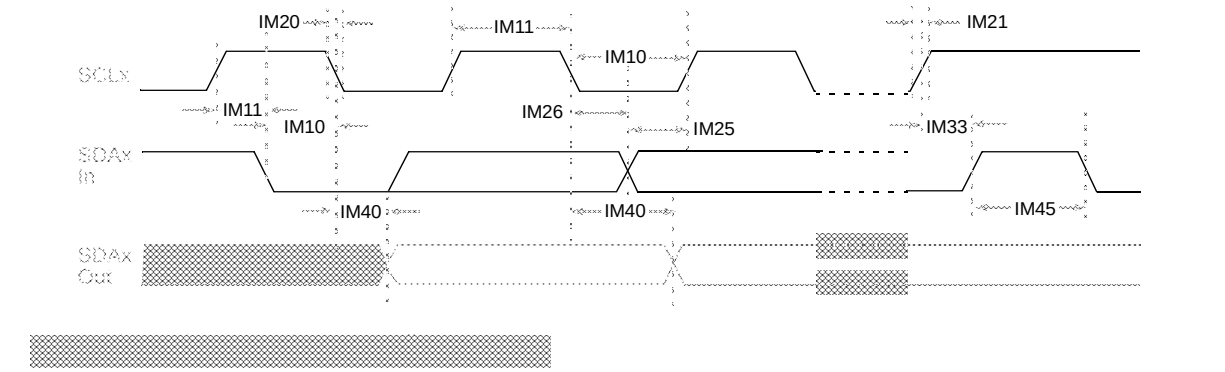


TABLE 37-35: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	—
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	—
IM11	THI:SCL	Clock High Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	—
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	—
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 2)**	—	100	ns	

Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

TABLE 37-35: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 2)**	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode **(Note 2)**	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	—
			400 kHz mode	0	0.9	µs	
			1 MHz mode **(Note 2)**	0	0.3	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	—
			1 MHz mode **(Note 2)**	—	350	ns	—
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode **(Note 2)**	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	—	pF	See parameter DO58
IM51	TPGD	Pulse Gobbler Delay		52	312	ns	See **Note 3**

Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

FIGURE 37-20: CANx MODULE I/O TIMING CHARACTERISTICS

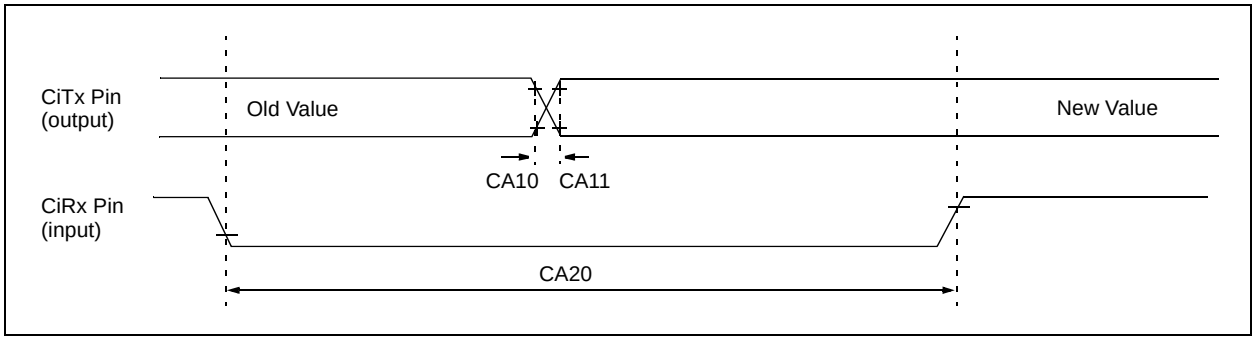


TABLE 37-37: CANx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
CA10	TioF	Port Output Fall Time	—	—	—	ns	See parameter DO32
CA11	TioR	Port Output Rise Time	—	—	—	ns	See parameter DO31
CA20	Tcwf	Pulse Width to Trigger CAN Wake-up Filter	700	—	—	ns	—

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 37-21: PARALLEL SLAVE PORT TIMING

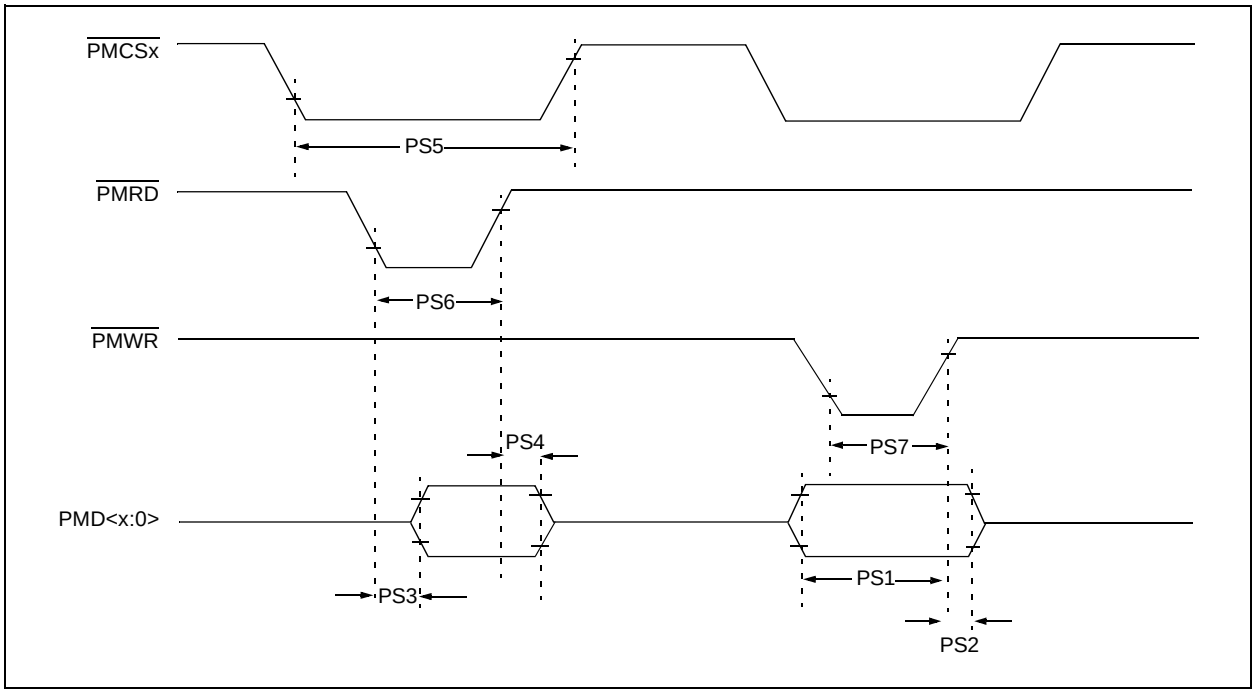


TABLE 37-42: PARALLEL SLAVE PORT REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PS1	TdtV2wrH	Data In Valid before $\overline{\text{PMWR}}$ or $\overline{\text{PMCSx}}$ Inactive (setup time)	20	—	—	ns	—
PS2	TwrH2dtI	$\overline{\text{PMWR}}$ or $\overline{\text{PMCSx}}$ Inactive to Data-in Invalid (hold time)	40	—	—	ns	—
PS3	TrdL2dtV	$\overline{\text{PMRD}}$ and $\overline{\text{PMCSx}}$ Active to Data-out Valid	—	—	60	ns	—
PS4	TrdH2dtI	$\overline{\text{PMRD}}$ Active or $\overline{\text{PMCSx}}$ Inactive to Data-out Invalid	0	—	10	ns	—
PS5	Tcs	$\overline{\text{PMCSx}}$ Active Time	TPBCLK2 + 40	—	—	ns	—
PS6	TWR	$\overline{\text{PMWR}}$ Active Time	TPBCLK2 + 25	—	—	ns	—
PS7	TRD	$\overline{\text{PMRD}}$ Active Time	TPBCLK2 + 25	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

NOTES: