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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	MIPS32 [®] M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	46
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efh064t-i-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

The FPU implements a high-performance 7-stage pipeline:

- Decode, register read and unpack (FR stage)
- Multiply tree, double pumped for double (M1 stage)
- Multiply complete (M2 stage)
- Addition first step (A1 stage)
- Addition second and final step (A2 stage)
- Packing to IEEE format (FP stage)
- Register writeback (FW stage)

The FPU implements a bypass mechanism that allows the result of an operation to be forwarded directly to the instruction that needs it without having to write the result to the FPU register and then read it back.

Table 3-5 lists the Coprocessor 1 Registers for the FPU.

Register Number	Register Name	Function
0	FIR	Floating Point implementation register. Contains information that identifies the FPU.
25	FCCR	Floating Point condition codes register.
26	FEXR	Floating Point exceptions register.
28	FENR	Floating Point enables register.
31	FCSR	Floating Point Control and Status register.

TABLE 3-5: FPU (CP1) REGISTERS

3.2 Power Management

The processor core offers a number of power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or halting the clocks, which reduces system power consumption during Idle periods.

3.2.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the WAIT instruction. For more information on power management, see Section 33.0 "Power-Saving Features".

3.2.2 LOCAL CLOCK GATING

The majority of the power consumed by the processor core is in the clock tree and clocking registers. The PIC32MZ family makes extensive use of local gatedclocks to reduce this dynamic power consumption.

3.3 L1 Instruction and Data Caches

3.3.1 INSTRUCTION CACHE (I-CACHE)

The I-Cache is an on-core memory block of 16 Kbytes. Because the I-Cache is virtually indexed, the virtual-tophysical address translation occurs in parallel with the cache access rather than having to wait for the physical address translation. The tag holds 22 bits of physical address, a valid bit, and a lock bit. The LRU replacement bits are stored in a separate array.

The I-Cache block also contains and manages the instruction line fill buffer. Besides accumulating data to be written to the cache, instruction fetches that reference data in the line fill buffer are serviced either by a bypass of that data, or data coming from the external interface. The I-Cache control logic controls the bypass function.

The processor core supports I-Cache locking. Cache locking allows critical code or data segments to be locked into the cache on a per-line basis, enabling the system programmer to maximize the efficiency of the system cache.

The cache locking function is always available on all I-Cache entries. Entries can then be marked as locked or unlocked on a per entry basis using the CACHE instruction.

3.3.2 DATA CACHE (D-CACHE)

The D-Cache is an on-core memory block of 4 Kbytes. This virtually indexed, physically tagged cache is protected. Because the D-Cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access. The tag holds 22 bits of physical address, a valid bit, and a lock bit. There is an additional array holding dirty bits and LRU replacement algorithm bits for each set of the cache.

In addition to I-Cache locking, the processor core also supports a D-Cache locking mechanism identical to the I-Cache. Critical data segments are locked into the cache on a per-line basis. The locked contents can be updated on a store hit, but cannot be selected for replacement on a cache miss.

The D-Cache locking function is always available on all D-Cache entries. Entries can then be marked as locked or unlocked on a per-entry basis using the CACHE instruction.

3.3.3 ATTRIBUTES

The processor core I-Cache and D-Cache attributes are listed in the Configuration registers (see Register 3-1 through Register 3-4).

TABLE 4-2: BO	OT FLASH 1 SEQUENCE	AND CONFIGURATION	WORDS SUMMARY
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SS										B	its								
Virtual Addre (BFC4_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
FF40	ABF1DEVCFG3	31:0																·	xxxx
FF44	ABF1DEVCFG2	31:0																	xxxx
FF48	ABF1DEVCFG1	31:0											xxxx						
FF4C	ABF1DEVCFG0	31:0																	
FF50	ABF1DEVCP3	31:0																	XXXX
FF54	ABF1DEVCP2	31:0							Note	• See Tab	le 34-2 for	the hit desc	rintions						XXXX
FF58	ABF1DEVCP1	31:0							Note	. Occ 100	04-2101		npuona.						xxxx
FF5C	ABF1DEVCP0	31:0																	xxxx
FF60	ABF1DEVSIGN3	31:0																	xxxx
FF64	ABF1DEVSIGN2	31:0																	xxxx
FF68	ABF1DEVSIGN1	31:0																	xxxx
FF6C	ABF1DEVSIGN0	31:0																	xxxx
FFC0	BF1DEVCFG3	31:0																	xxxx
FFC4	BF1DEVCFG2	31:0																	xxxx
FFC8	BF1DEVCFG1	31:0																	xxxx
FFCC	BF1DEVCFG0	31:0																	xxxx
FFD0	BF1DEVCP3	31:0																	xxxx
FFD4	BF1DEVCP2	31:0							Note	• See Tab	le 34-1 for	the hit desc	rintions						xxxx
FFD8	BF1DEVCP1	31:0							Hote	. 000 100			inpuorio.						xxxx
FFDC	BF1DEVCP0	31:0																	xxxx
FFE0	BF1DEVSIGN3	31:0																	xxxx
FFE4	BF1DEVSIGN2	31:0																	xxxx
FFE8	BF1DEVSIGN1	31:0																	xxxx
FFEC	BF1DEVSIGN0	31:0																	xxxx
FFF0	BF1SEQ3	31:16								CSEQ	<15:0>								xxxx
	ļļ	10:0								ISEQ	<15:0>								XXXX
FFF4	BF1SEQ2	31:16 15:0	_															$\vdash =$	XXXX
		31.16	_	_	_	_	_		_	_	_	_	_	_	_	_	_	<u> </u>	XXXX
FFF8	BF1SEQ1	15:0	_																XXXX
	ł ł	31.16	_				_	_					_		_		_		XXXX
FFFC	BF1SEQ0	15:0	_	_	_	_	_	_		_	_	_	_	_	_	_	_		XXXX

x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal. Legend:

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

The System Bus arbitration scheme implements a nonprogrammable, Least Recently Serviced (LRS) priority, which provides Quality Of Service (QOS) for most initiators. However, some initiators can use Fixed High Priority (HIGH) arbitration to guarantee their access to data.

The arbitration scheme for the available initiators is shown in Table 4-5.

Name	ID	QOS
CPU	1	LRS ⁽¹⁾
CPU	2	HIGH ^(1,2)
DMA Read	3	LRS ⁽¹⁾
DMA Read	4	HIGH ^(1,2)
DMA Write	5	LRS ⁽¹⁾
DMA Write	6	HIGH ^(1,2)
USB	7	LRS
Ethernet Read	8	LRS
Ethernet Write	9	LRS
CAN1	10	LRS
CAN2	11	LRS
SQI1	12	LRS
Flash Controller	13	HIGH ⁽²⁾
Crypto	14	LRS

TABLE 4-5:INITIATOR ID AND QOS

- Note 1: When accessing SRAM, the DMAPRI bit (CFGCON<25>) and the CPUPRI bit (CFGCON<24>) provide arbitration control for the DMA and CPU (when servicing an interrupt (i.e., EXL = 1)), respectively, by selecting the use of LRS or HIGH When using HIGH, the DMA and CPU get arbitration preference over all initiators using LRS.
 - 2: Using HIGH arbitration can have serious negative effects on other initiators. Therefore, it is recommended to not enable this type of arbitration for an initiator that uses significant system bandwidth. HIGH arbitration is intended to be used for low bandwidth applications that require low latency, such as LCC graphics applications.

4.3 Permission Access and System Bus Registers

The System Bus on PIC32MZ EF family of microcontrollers provides access control capabilities for the transaction initiators on the System Bus.

The System Bus divides the entire memory space into fourteen target regions and permits access to each target by initiators via permission groups. Four Permission Groups (0 through 3) can be assigned to each initiator. Each permission group is independent of the others and can have exclusive or shared access to a region.

Using the CFGPG register (see Register 34-10 in **Section 34.0 "Special Features"**), Boot firmware can assign a permission group to each initiator, which can make requests on the System Bus.

The available targets and their regions, as well as the associated control registers to assign protection, are described and listed in Table 4-6.

Register 4-2 through Register 4-10 are used for setting and controlling access permission groups and regions.

To change these registers, they must be unlocked in hardware. The register lock is controlled by the PGLOCK Configuration bit (CFGCON<11>). Setting PGLOCK prevents writes to the control registers; clearing PGLOCK allows writes.

To set or clear the PGLOCK bit, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** in the *"PIC32 Family Reference Manual"* for details.

					-	-				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
04.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
31.24				NVMDA	TA<31:24>					
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23:16	NVMDATA<23:16>									
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	NVMDATA<15:8>									
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
		NVMDATA<7:0>								

REGISTER 5-5: NVMDATAX: FLASH DATA REGISTER (x = 0-3)

Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMDATA<31:0>: Flash Data bits

Word Program: Writes NVMDATA0 to the target Flash address defined in NVMADDR Quad Word Program: Writes NVMDATA3:NVMDATA2:NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR. NVMDATA0 contains the Least Significant Instruction Word.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

REGISTER 5-6: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31.24	NVMSRCADDR<31:24>										
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23:16	NVMSRCADDR<23:16>										
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	NVMSRCADDR<15:8>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7.0				NVMSRC	ADDR<7:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMSRCADDR<31:0>: Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other reset sources.



FIGURE 8-1: PIC32MZ EF FAMILY OSCILLATOR DIAGRAM

3. Refer to Section 42. "Oscillators with Enhanced PLL" (DS60001250) in the "PIC32 Family Reference Manual" for help in determining the best oscillator components.

- 4. PBCLK1 divided by 2 is available on the OSC2 pin in certain clock modes.
- 5. Shaded regions indicate multiple instantiations of a peripheral or feature.
- 6. Refer to Table 37-19 in Section 37.0 "Electrical Characteristics" for frequency limitations.

7. If the DEVCFG registers are configured for a SYSCLK speed greater than 200 MHz, these PBCLKs will be running faster than the maximum rating when the device comes out of Reset. To ensure proper operation, firmware must start the device at a speed less than or equal to 200 MHz, adjust the speed of the PBCLKs, and then raise the SYSCLK speed to the desired speed.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31:24		CHSSA<31:24>									
00-10	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23:16	CHSSA<23:16>										
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	CHSSA<15:8>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0		CHSSA<7:0>									

REGISTER 10-10: DCHxSSA: DMA CHANNEL x SOURCE START ADDRESS REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 CHSSA<31:0> Channel Source Start Address bits Channel source start address. Note: This must be the physical address of the source.

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REGISTER 10-11: DCHxDSA: DMA CHANNEL x DESTINATION START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31:24				CHDSA<	:31:24>				
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23:16	CHDSA<23:16>								
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15:8	CHDSA<15:8>								
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0				CHDSA	<7:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 CHDSA<31:0>: Channel Destination Start Address bits Channel destination start address.

Note: This must be the physical address of the destination.

REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)

bit 18 **OVERRUN:** Data Overrun Status bit (*Device mode*)

- 1 = An OUT packet cannot be loaded into the RX FIFO.
- 0 = Written by software to clear this bit

This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.

ERROR: No Data Packet Received Status bit (Host mode)

- 1 = Three attempts have been made to receive a packet and no data packet has been received. An interrupt is generated.
- 0 = Written by the software to clear this bit.

This bit is only valid when the RX endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns zero.

- bit 17 FIFOFULL: FIFO Full Status bit
 - 1 = No more packets can be loaded into the RX FIFO
 - 0 = The RX FIFO has at least one free space
- bit 16 RXPKTRDY: Data Packet Reception Status bit
 - 1 = A data packet has been received. An interrupt is generated.
 - 0 = Written by software to clear this bit when the packet has been unloaded from the RX FIFO.
- bit 15-11 MULT<4:0>: Multiplier Control bits

For Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints, multiplies TXMAXP by MULT+1 for the payload size.

For Bulk endpoints, MULT can be up to 32 and defines the number of "USB" packets of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. The data packet is required to be an exact multiple of the payload specified by TXMAXP.

For Isochronous/Interrupts endpoints operating in Hi-Speed mode, MULT may be either 2 or 3 and specifies the maximum number of such transactions that can take place in a single microframe.

bit 10-0 RXMAXP<10:0>: Maximum RX Payload Per Transaction Control bits

This field sets the maximum payload (in bytes) transmitted in a single transaction. The value is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-Speed and Hi-Speed operations.

RXMAXP must be set to an even number of bytes for proper interrupt generation in DMA Mode 1.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31.24	—		TXHUBPRT<6:0>						
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23.10	MULTTRAN		TXHUBADD<6:0>						
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
15.0	—	_	—	—	—	—	—	—	
7.0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0	_		TXFADDR<6:0>						

REGISTER 11-18: USBExTXA: USB ENDPOINT 'x' TRANSMIT ADDRESS REGISTER

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Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 Unimplemented: Read as '0'

bit 30-24 **TXHUBPRT<6:0>:** TX Hub Port bits (Host mode) When a Low-Speed or Full-Speed device is connected to this endpoint through a Hi-Speed USB 2.0 hub, this field records the port number of that USB 2.0 hub.

- bit 23 MULTTRAN: TX Hub Multiple Translators bit (Host mode) 1 = The USB 2.0 hub has multiple transaction translators
 - 0 = The USB 2.0 hub has a single transaction translator

bit 22-16 **TXHUBADD<6:0>:** TX Hub Address bits (Host mode) When a Low-Speed or Full-Speed device is connected to this endpoint through a Hi-Speed USB 2.0 hub, these bits record the address of the USB 2.0 hub.

- bit 15-7 Unimplemented: Read as '0'
- bit 6-0 TXFADDR<6:0>: TX Functional Address bits (Host mode)

Specifies the address for the target function that is be accessed through the associated endpoint. It needs to be defined for each TX endpoint that is used.

TABLE 12-10: PORTD REGISTER MAP FOR 64-PIN DEVICES ONLY

ess		0								В	its								
Virtual Addr (BF86_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0310	TRISD	31:16	_	_	—		—	—	—	_	_		—	-	—	—	—		0000
0310	INIOD	15:0	—	—	—		TRISD11	TRISD10	TRISD9	—	—		TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	0E3F
0320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0020	TORTE	15:0	—	—	—	—	RD11	RD10	RD9	—	—	_	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
0330	LATD	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	—	_	_	0000
	2.12	15:0	_	—	—	_	LATD11	LATD10	LATD9	—	—	_	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
0340	ODCD	31:16	_	_					—	_	—		—	—				—	0000
		15:0	_	—	—	_	ODCD11	ODCD10	ODCD9	_	_	_	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
0350	CNPUD	31:16	_	_	_	_	—	—	—	_	_	_	—	—	—	—	—	—	0000
		15:0	_	_	_	—	CNPUD11	CNPUD10	CNPUD9	_	_	_	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
0360	CNPDD	31:16	_	_	_		-	-	-	_	_		-	-	-	-	-	-	0000
		15:0	_	_			CNPDD11	CNPDD10	CNPDD9				CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
0270		31:16	_	_	_	_	-	_	_	_	_	_	_	_	_	_	_	_	0000
0370	CINCOIND	15:0	ON	_	—		DETECT	—	—	—	—	-	—	-	—	—	—	-	0000
0380		31:16	-	-	_		_	_	_	-	-		_		_	_	-		0000
0380	CINEIND	15:0	-	_	_		CNEND11	CNEND10	CNEND9				CNEND5	CNEND4	CNEND3	CNEND2	CNEND1	CNEND0	0000
		31:16	—	—	—	_	—	—	—	—	—	-	—	-	—	—	—	—	0000
0390	CNSTATD	15:0	—	—	—	—	CN STATD11	CN STATD10	CN STATD9	—	—	—	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	CN STATD0	0000
00 4 0		31:16	_	_	_		_	_	_	_	_	_	_	-	_	_	_		0000
03A0	CININED	15:0	_	_	—	_	CNNED11	CNNED10	CNNED9	_	_	_	CNNED5	CNNED4	CNNED3	CNNED2	CNNED1	CNNED0	0000
0200		31:16	_	_		_	_	_	_	_	_	_	—	_	_	_	_	—	0000
03B0	CINFD	15:0	_	_	_		CNFD11	CNFD10	CNFD9	_	_		CNFD5	CNFD4	CNFD3	CNFD2	CNFD1	CNFD0	0000

Legend:

x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal. All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.3 "CLR, SET, and INV Registers" for Note 1: more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	-	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	-	—	—
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	_	—	—
7.0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
7:0		_		_	_	START	POLLEN	DMAEN

REGISTER 20-14: SQI1BDCON: SQI BUFFER DESCRIPTOR CONTROL REGISTER

Legend:

bit 0

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-3 Unimplemented: Read as '0'

- bit 2 START: Buffer Descriptor Processor Start bit
 - 1 = Start the buffer descriptor processor
 - 0 = Disable the buffer descriptor processor
- bit 1 POLLEN: Buffer Descriptor Poll Enable bit
 - 1 = BDP poll is enabled
 - 0 = BDP poll is not enabled
 - DMAEN: DMA Enable bit
 - 1 = DMA is enabled
 - 0 = DMA is disabled

REGISTER 20-15: SQI1BDCURADD: SQI BUFFER DESCRIPTOR CURRENT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
31.24	BDCURRADDR<31:24>							
00.40	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
23:16	BDCURRADDR<23:16>							
45.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
15:8	BDCURRADDR<15:8>							
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7.0				BDCURRAD	DDR<7:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 BDCURRADDR<31:0>: Current Buffer Descriptor Address bits

These bits contain the address of the current descriptor being processed by the Buffer Descriptor Processor.

	R	EGISTER							
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	U-0	U-0	U-0	R-x	R-x R-x R-x R-x		U-0		
31:24	—	—	—		RXSTATE<3:0>				
22.16	U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x	
23.10	—	—			RXBUFCNT<4:0>				
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
15:8	—	—		_	—			_	
7.0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x	
7:0	RXCURBUFLEN<7:0>								

REGISTER 20-20: SQI1BDRXDSTAT: SQI BUFFER DESCRIPTOR DMA RECEIVE STATUS REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 Unimplemented: Read as '0'

- bit 28-25 **RXSTATE<3:0>:** Current DMA Receive State Status bits These bits provide information on the current DMA receive states.
- bit 24-21 Unimplemented: Read as '0'
- bit 20-16 **RXBUFCNT<4:0>:** DMA Buffer Byte Count Status bits These bits provide information on the internal FIFO space.
- bit 15-8 Unimplemented: Read as '0'
- bit 7-0 **RXCURBUFLEN<7:0>:** Current DMA Receive Buffer Length Status bits These bits provide the length of the current DMA receive buffer.

REGISTER 20-21: SQI1THR: SQI THRESHOLD CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10		—	—	—	—	—	—	—
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0		_	_	THRES<4:0>				

Legend:

Logona.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-5 Unimplemented: Read as '0'

bit 4-0 THRES<4:0>: SQI Control Threshold Value bits

The SQI control threshold interrupt is asserted when the amount of space indicated by THRES<4:0> is available in the SQI control buffer.

23.0 PARALLEL MASTER PORT (PMP)

Note:	This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive refer- ence source. To complement the informa-
	tion in this data sheet, refer to Section 13.
	"Parallel Master Port (PMP)"
	(DS60001128) in the "PIC32 Family Ref-
	erence Manual", which is available from
	the Microchip web site (www.micro- chip.com/PIC32).

The PMP is a parallel 8-bit/16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable. The following are key features of the PMP module:

- 8-bit,16-bit interface
- Up to 16 programmable address lines
- Up to two Chip Select lines
- Programmable strobe options:
 - Individual read and write strobes, or
 - Read/write strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Parallel Slave Port support:
 - Legacy addressable
 - Address support
 - 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Operate during Sleep and Idle modes
- Separate configurable read/write registers or dual buffers for Master mode
- Fast bit manipulation using CLR, SET, and INV registers

Note: On 64-pin devices, data pins PMD<15:8> are not available in 16-bit Master modes.





									1		
Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
	15:8				ENCKEY<	15:8>					
	7:0				ENCKEY<	:7:0>					
SA_ENCKEY3	31:24		ENCKEY<31:24>								
	23:16				ENCKEY<2	23:16>					
	15:8	ENCKEY<15:8>									
	7:0				ENCKEY<	:7:0>					
SA_ENCKEY4	31:24				ENCKEY<3	81:24>					
	23:16				ENCKEY<2	23:16>					
	15:8				ENCKEY<	15:8>					
	7:0				ENCKEY<	:7:0>					
SA_ENCKEY5	31:24				ENCKEY<3	81:24>					
	23:16				ENCKEY<2	23:16>					
	15:8				ENCKEY<	15:8>					
	7:0				ENCKEY<	:7:0>					
SA_ENCKEY6	31:24				ENCKEY<3	81:24>					
	23:16				ENCKEY<2	23:16>					
	15:8				ENCKEY<	15:8>					
	7:0				ENCKEY<	:7:0>					
SA_ENCKEY7	31:24				ENCKEY<3	81:24>					
	23:16				ENCKEY<2	23:16>					
	15:8				ENCKEY<	15:8>					
	7:0				ENCKEY<	:7:0>					
SA_ENCKEY8	31:24				ENCKEY<3	31:24>					
	23:16				ENCKEY<2	23:16>					
	15:8		ENCKEY<15:8>								
	7:0				ENCKEY<	:7:0>					
SA_AUTHIV1	31:24		AUTHIV<31:24>								
	23:16	AUTHIV<23:16>									
	15:8				AUTHIV<1	5:8>					
	7:0				AUTHIV<	7:0>					
SA_AUTHIV2	31:24				AUTHIV<3	1:24>					
	23:16		AUTHIV<23:16>								
	15:8				AUTHIV<1	15:8>					
	7:0				AUTHIV<	7:0>					
SA_AUTHIV3	31:24				AUTHIV<3	1:24>					
	23:16		AUTHIV<23:16>								
	15:8				AUTHIV<1	15:8>					
	7:0				AUTHIV<	7:0>					
SA_AUTHIV4	31:24				AUTHIV<3	1:24>					
	23:16				AUTHIV<2	3:16>					
	15:8				AUTHIV<1	5:8>					
	7:0				AUTHIV<	7:0>					
SA_AUTHIV5	31:24				AUTHIV<3	1:24>					
	23:16				AUTHIV<2	3:16>					
	15:8				AUTHIV<1	15:8>					
	7:0				AUTHIV<	7:0>					
SA_AUTHIV6	31:24				AUTHIV<3	1:24>					
	23:16				AUTHIV<2	3:16>					
	15:8				AUTHIV<1	15:8>					
0.4. AL 171 III /7	7:0	AUTHIV<7:0>									
SA_AUTHIV7	31:24	24 AUTHIV<31:24>									
	23:16	23:16 AUTHIV<23:16>									
	15:8	5:8 AUTHIV<15:8>									
0.4 41171 111 15	7:0				AUTHIV<	/:U>					
SA_AUTHIV8	31:24				AUTHIV<3	1:24>					
	23:16				AUTHIV<2	3:16>					
	15:8					15:8>					
	1:0				AUTHIV<	1:0>					

TABLE 26-4: CRYPTO ENGINE SECURITY ASSOCIATION STRUCTURE (CONTINUED)

REGISTER 28-14: ADCCMPENX: ADC DIGITAL COMPARATOR 'x' ENABLE REGISTER ('x' = 1 THROUGH 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-0							
31.24	CMPE31 ⁽¹⁾	CMPE30 ⁽¹⁾	CMPE29 ⁽¹⁾	CMPE28 ⁽¹⁾	CMPE27 ⁽¹⁾	CMPE26 ⁽¹⁾	CMPE25 ⁽¹⁾	CMPE24 ⁽¹⁾
00.40	R/W-0							
23:16	CMPE23 ⁽¹⁾	CMPE22 ⁽¹⁾	CMPE21 ⁽¹⁾	CMPE20 ⁽¹⁾	CMPE19 ⁽¹⁾	CMPE18	CMPE17	CMPE16
15.0	R/W-0							
15.0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8
7.0	R/W-0							
7:0	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 CMPE31:CMPE0: ADC Digital Comparator 'x' Enable bits^(2,3)

These bits enable conversion results corresponding to the Analog Input to be processed by the Digital Comparator. CMPE0 enables AN0, CMPE1 enables AN1, and so on.

Note 1: This bit is not available on 64-pin devices.

- **2**: CMPEx = ANx, where 'x' = 0.31 (Digital Comparator inputs are limited to AN0 through AN31).
- **3:** Changing the bits in this register while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	S/HC-0	R/W-1	R/W-0	R/W-0
31.24	—	—	—	—	ABAT	F	REQOP<2:0>	>
22.16	R-1	R-0	R-0	R/W-0	U-0	U-0	U-0	U-0
23.10	(OPMOD<2:0>		CANCAP	—	—	—	—
45.0	R/W-0	U-0	R/W-0	U-0	R-0	U-0	U-0	U-0
15:8	ON ⁽¹⁾	—	SIDLE	—	CANBUSY	—	—	—
7.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_	_			DNCNT<4:0>		

REGISTER 29-1: CICON: CAN MODULE CONTROL REGISTER

Legend:	HC = Hardware Clear	S = Settable bit	
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	t -n = Bit Value at POR: ('	0'. '1'. x = Unknown)	

bit 31-28 Unimplemented: Read as '0'

bit 27 **ABAT:** Abort All Pending Transmissions bit

- 1 = Signal all transmit buffers to abort transmission
- 0 = Module will clear this bit when all transmissions aborted

bit 26-24 REQOP<2:0>: Request Operation Mode bits

- 111 = Set Listen All Messages mode
- 110 = Reserved Do not use
- 101 = Reserved Do not use
- 100 = Set Configuration mode
- 011 = Set Listen Only mode
- 010 = Set Loopback mode
- 001 = Set Disable mode
- 000 = Set Normal Operation mode

bit 23-21 OPMOD<2:0>: Operation Mode Status bits

- 111 = Module is in Listen All Messages mode
- 110 = Reserved
- 101 = Reserved
- 100 = Module is in Configuration mode
- 011 = Module is in Listen Only mode
- 010 = Module is in Loopback mode
- 001 = Module is in Disable mode
- 000 = Module is in Normal Operation mode

bit 20 CANCAP: CAN Message Receive Time Stamp Timer Capture Enable bit

- 1 = CANTMR value is stored on valid message reception and is stored with the message
- 0 = Disable CAN message receive time stamp timer capture and stop CANTMR to conserve power
- bit 19-16 Unimplemented: Read as '0'
- bit 15 **ON:** CAN On bit⁽¹⁾
 - 1 = CAN module is enabled
 - 0 = CAN module is disabled
- bit 14 Unimplemented: Read as '0'
- **Note 1:** If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	FLTEN31	MSEL31<1:0>				FSEL31<4:0>		
22:46	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16	FLTEN30	MSEL30<1:0>			FSEL30<4:0>			
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
0.61	FLTEN29	MSEL2	9<1:0>			FSEL29<4:0>		
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	FLTEN28	MSEL2	28<1:0>			FSEL28<4:0>		

REGISTER 29-17: CIFLTCON7: CAN FILTER CONTROL REGISTER 7

Legend:

L:L 04

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

011.31	FLIENSI: Filler ST Enable bit
	1 = Filter is enabled

0 = Filter is disabled

bit 30-29 MSEL31<1:0>: Filter 31 Mask Select bits

ELTENDA: Eller OA Exclusion

- 11 = Acceptance Mask 3 selected
- 10 = Acceptance Mask 2 selected
- 01 = Acceptance Mask 1 selected
- 00 = Acceptance Mask 0 selected

bit 28-24 FSEL31<4:0>: FIFO Selection bits

- 11111 = Message matching filter is stored in FIFO buffer 31
- 11110 = Message matching filter is stored in FIFO buffer 30
- •

•

- 00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0
- bit 23 **FLTEN30:** Filter 30Enable bit
 - 1 = Filter is enabled
 - 0 = Filter is disabled

bit 22-21 MSEL30<1:0>: Filter 30Mask Select bits

- 11 = Acceptance Mask 3 selected
- 10 = Acceptance Mask 2 selected
- 01 = Acceptance Mask 1 selected
- 00 = Acceptance Mask 0 selected

bit 20-16 FSEL30<4:0>: FIFO Selection bits

- 11111 = Message matching filter is stored in FIFO buffer 31
- 11110 = Message matching filter is stored in FIFO buffer 30
- 00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTE	R 30-33:	EM	AC1MADR:	ETHERNET	CONTROLL	LER MAC N	III MANAG	EMENT AD	DRESS
REGISTER									
Dit									

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10		—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
15.0		—	—		PH	HYADDR<4:0	>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	_	_	_		RE	GADDR<4:0)>	

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 Unimplemented: Read as '0'

- bit 12-8 **PHYADDR<4:0>:** MII Management PHY Address bits This field represents the 5-bit PHY Address field of Management cycles. Up to 31 PHYs can be addressed (0 is reserved).
- bit 7-5 Unimplemented: Read as '0'
- bit 4-0 **REGADDR<4:0>:** MII Management Register Address bits This field represents the 5-bit Register Address field of Management cycles. Up to 32 registers can be accessed.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.



TABLE 37-25: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS⁽¹⁾

AC CHARACTERISTICS				Star (un Ope	Standard Operating Conditions: 2.1V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param. No.	Symbol	Characteristics ⁽²⁾			Min.		Max.	Units	Conditions	
TA10	ТтхН	TxCK High Time	Synchronous, with prescaler		[(12.5 ns or 1 TPBCLK3) /N] + 20 ns	—		ns	Must also meet parameter TA15 (Note 3)	
			Asynchronous, with prescaler		10 —		—	ns	—	
TA11	ΤτxL	TxCK Synchrono Low Time with presca		ous, aler	[(12.5 ns or 1 TPBCLK3) /N] + 20 ns	—	_	ns	Must also meet parameter TA15 (Note 3)	
			Asynchronous, with prescaler		10	—	_	ns	_	
TA15 TTXP TxCK Synchronous Input Period with prescale		ous, aler	[(Greater of 20 ns or 2 TPBCLK3)/N] + 30 ns	—	_	ns	VDD > 2.7V (Note 3)			
					[(Greater of 20 ns or 2 ТРВСLК3)/N] + 50 ns	—	_	ns	VDD < 2.7V (Note 3)	
			Asynchro	nous,	20	—	-	ns	Vdd > 2.7V	
			with prescaler		50 –		—	ns	Vdd < 2.7V	
OS60	FT1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by settin TCS bit (T1CON<1>))		r etting	32	—	50	kHz	—	
TA20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		CK	—		1	ТРВСЬКЗ	—	

Note 1: Timer1 is a Type A timer.

2: This parameter is characterized, but not tested in manufacturing.

3: N = Prescale Value (1, 8, 64, 256).

38.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MZ EF device AC characteristics and timing parameters.

TABLE 38-5:	SYSTEM TIMING REQUIREMENTS
-------------	----------------------------

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param. No.	Param. No. Symbol Characteristics		Min.	Тур.	Max.	Units	Conditions
EOS51	Fsys	System Frequency	DC	—	180	MHz	USB module disabled
			30	_	180	MHz	USB module enabled
EOS55a	Fрв	Peripheral Bus Frequency	DC		90	MHz	For PBCLKx, 'x' \neq 4, 7
EOS55b			DC		180	MHz	For PBCLK4, PBCLK7
EOS56	Fref	Reference Clock Frequency	_		45	MHz	For REFCLKI1, 3, 4 and REFCLKO1, 3, 4 pins

TABLE 38-6: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS (uni Ope			Standard (unless of Operating	Standard Operating Conditions: 2.1V to 3.6V unless otherwise stated) Derating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param. No.	Symbol	Characteristics ⁽¹⁾		Min.	Typical	Max.	Units	Conditions	
EOS54a	Fpll	PLL Output Frequency Range		10	_	180	MHz		

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{PBCLK2}{\sqrt{CommunicationClock}}}}$$

For example, if PBCLK2 = 100 MHz and SPI bit rate = 50 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{100}{50}}} = \frac{D_{CLK}}{1.41}$$

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.70 x 7.70 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Number of Pins	Ν	64			
Pitch	е		0.50 BSC		
Overall Height	Α	0.80 0.85 0.90			
Standoff	A1	0.00 0.02 0.05			
Contact Thickness	A3	0.20 REF			
Overall Width	E	9.00 BSC			
Exposed Pad Width	E2	7.60 7.70 7.80			
Overall Length	D	9.00 BSC			
Exposed Pad Length	D2	7.60 7.70 7.80			
Contact Width	b	0.20	0.25	0.30	
Contact Length	L	0.30 0.40 0.50			
Contact-to-Exposed Pad	K	< 0.20			

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

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