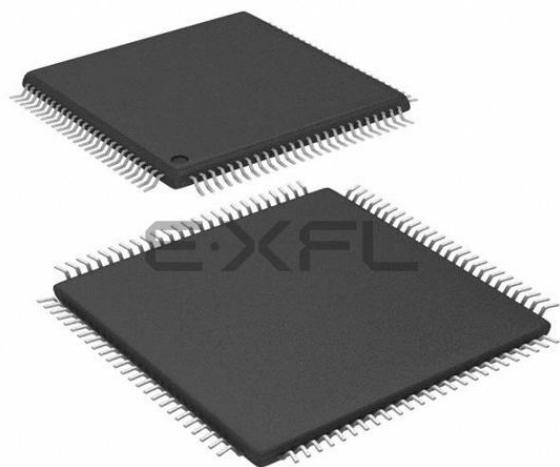




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Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efh100-i-pt

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
System Bus Protection Violation	_SYSTEM_BUS_PROTECTION_VECTOR	106	OFF106<17:1>	IFS3<10>	IEC3<10>	IPC26<20:18>	IPC26<17:16>	Yes
Crypto Engine Event	_CRYPTO_VECTOR	107	OFF107<17:1>	IFS3<11>	IEC3<11>	IPC26<28:26>	IPC26<25:24>	Yes
Reserved	—	108	—	—	—	—	—	—
SPI1 Fault	_SPI1_FAULT_VECTOR	109	OFF109<17:1>	IFS3<13>	IEC3<13>	IPC27<12:10>	IPC27<9:8>	Yes
SPI1 Receive Done	_SPI1_RX_VECTOR	110	OFF110<17:1>	IFS3<14>	IEC3<14>	IPC27<20:18>	IPC27<17:16>	Yes
SPI1 Transfer Done	_SPI1_TX_VECTOR	111	OFF111<17:1>	IFS3<15>	IEC3<15>	IPC27<28:26>	IPC27<25:24>	Yes
UART1 Fault	_UART1_FAULT_VECTOR	112	OFF112<17:1>	IFS3<16>	IEC3<16>	IPC28<4:2>	IPC28<1:0>	Yes
UART1 Receive Done	_UART1_RX_VECTOR	113	OFF113<17:1>	IFS3<17>	IEC3<17>	IPC28<12:10>	IPC28<9:8>	Yes
UART1 Transfer Done	_UART1_TX_VECTOR	114	OFF114<17:1>	IFS3<18>	IEC3<18>	IPC28<20:18>	IPC28<17:16>	Yes
I2C1 Bus Collision Event	_I2C1_BUS_VECTOR	115	OFF115<17:1>	IFS3<19>	IEC3<19>	IPC28<28:26>	IPC28<25:24>	Yes
I2C1 Slave Event	_I2C1_SLAVE_VECTOR	116	OFF116<17:1>	IFS3<20>	IEC3<20>	IPC29<4:2>	IPC29<1:0>	Yes
I2C1 Master Event	_I2C1_MASTER_VECTOR	117	OFF117<17:1>	IFS3<21>	IEC3<21>	IPC29<12:10>	IPC29<9:8>	Yes
PORTA Input Change Interrupt ⁽²⁾	_CHANGE_NOTICE_A_VECTOR	118	OFF118<17:1>	IFS3<22>	IEC3<22>	IPC29<20:18>	IPC29<17:16>	Yes
PORTB Input Change Interrupt	_CHANGE_NOTICE_B_VECTOR	119	OFF119<17:1>	IFS3<23>	IEC3<23>	IPC29<28:26>	IPC29<25:24>	Yes
PORTC Input Change Interrupt	_CHANGE_NOTICE_C_VECTOR	120	OFF120<17:1>	IFS3<24>	IEC3<24>	IPC30<4:2>	IPC30<1:0>	Yes
PORTD Input Change Interrupt	_CHANGE_NOTICE_D_VECTOR	121	OFF121<17:1>	IFS3<25>	IEC3<25>	IPC30<12:10>	IPC30<9:8>	Yes
PORTE Input Change Interrupt	_CHANGE_NOTICE_E_VECTOR	122	OFF122<17:1>	IFS3<26>	IEC3<26>	IPC30<20:18>	IPC30<17:16>	Yes
PORTF Input Change Interrupt	_CHANGE_NOTICE_F_VECTOR	123	OFF123<17:1>	IFS3<27>	IEC3<27>	IPC30<28:26>	IPC30<25:24>	Yes
PORTG Input Change Interrupt	_CHANGE_NOTICE_G_VECTOR	124	OFF124<17:1>	IFS3<28>	IEC3<28>	IPC31<4:2>	IPC31<1:0>	Yes
PORTH Input Change Interrupt ^(2,3)	_CHANGE_NOTICE_H_VECTOR	125	OFF125<17:1>	IFS3<29>	IEC3<29>	IPC31<12:10>	IPC31<9:8>	Yes
PORTJ Input Change Interrupt ^(2,3)	_CHANGE_NOTICE_J_VECTOR	126	OFF126<17:1>	IFS3<30>	IEC3<30>	IPC31<20:18>	IPC31<17:16>	Yes
PORTK Input Change Interrupt ^(2,3,4)	_CHANGE_NOTICE_K_VECTOR	127	OFF127<17:1>	IFS3<31>	IEC3<31>	IPC31<28:26>	IPC31<25:24>	Yes
Parallel Master Port	_PMP_VECTOR	128	OFF128<17:1>	IFS4<0>	IEC4<0>	IPC32<4:2>	IPC32<1:0>	Yes
Parallel Master Port Error	_PMP_ERROR_VECTOR	129	OFF129<17:1>	IFS4<1>	IEC4<1>	IPC32<12:10>	IPC32<9:8>	Yes
Comparator 1 Interrupt	_COMPARATOR_1_VECTOR	130	OFF130<17:1>	IFS4<2>	IEC4<2>	IPC32<20:18>	IPC32<17:16>	No
Comparator 2 Interrupt	_COMPARATOR_2_VECTOR	131	OFF131<17:1>	IFS4<3>	IEC4<3>	IPC32<28:26>	IPC32<25:24>	No
USB General Event	_USB1_VECTOR	132	OFF132<17:1>	IFS4<4>	IEC4<4>	IPC33<4:2>	IPC33<1:0>	Yes
USB DMA Event	_USB1_DMA_VECTOR	133	OFF133<17:1>	IFS4<5>	IEC4<5>	IPC33<12:10>	IPC33<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MZ EF Family Features”** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

4: This interrupt source is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
01F0	IPC11	31:16	—	—	—	ADCDC2IP<2:0>			ADCDC2IS<1:0>			—	—	—	ADCDC1IP<2:0>			ADCDC1IS<1:0>		0000
		15:0	—	—	—	ADCFIFOIP<2:0>			ADCFIFOIS<1:0>			—	—	—	ADCIP<2:0>			ADCIS<1:0>		0000
0200	IPC12	31:16	—	—	—	ADCDC6IP<2:0>			ADCDC6IS<1:0>			—	—	—	ADCDC5IP<2:0>			ADCDC5IS<1:0>		0000
		15:0	—	—	—	ADCDC4IP<2:0>			ADCDC4IS<1:0>			—	—	—	ADCDC3IP<2:0>			ADCDC3IS<1:0>		0000
0210	IPC13	31:16	—	—	—	ADCDF4IP<2:0>			ADCDF4IS<1:0>			—	—	—	ADCDF3IP<2:0>			ADCDF3IS<1:0>		0000
		15:0	—	—	—	ADCDF2IP<2:0>			ADCDF2IS<1:0>			—	—	—	ADCDF1IP<2:0>			ADCDF1IS<1:0>		0000
0220	IPC14	31:16	—	—	—	ADCD0IP<2:0>			ADCD0IS<1:0>			—	—	—	ADCDFLTIP<2:0>			ADCDFLTIS<1:0>		0000
		15:0	—	—	—	ADCDF6IP<2:0>			ADCDF6IS<1:0>			—	—	—	ADCDF5IP<2:0>			ADCDF5IS<1:0>		0000
0230	IPC15	31:16	—	—	—	ADCD4IP<2:0>			ADCD4IS<1:0>			—	—	—	ADCD3IP<2:0>			ADCD3IS<1:0>		0000
		15:0	—	—	—	ADCD2IP<2:0>			ADCD2IS<1:0>			—	—	—	ADCD1IP<2:0>			ADCD1IS<1:0>		0000
0240	IPC16	31:16	—	—	—	ADCD8IP<2:0>			ADCD8IS<1:0>			—	—	—	ADCD7IP<2:0>			ADCD7IS<1:0>		0000
		15:0	—	—	—	ADCD6IP<2:0>			ADCD6IS<1:0>			—	—	—	ADCD5IP<2:0>			ADCD5IS<1:0>		0000
0250	IPC17	31:16	—	—	—	ADCD12IP<2:0>			ADCD12IS<1:0>			—	—	—	ADCD11IP<2:0>			ADCD11IS<1:0>		0000
		15:0	—	—	—	ADCD10IP<2:0>			ADCD10IS<1:0>			—	—	—	ADCD9IP<2:0>			ADCD9IS<1:0>		0000
0260	IPC18	31:16	—	—	—	ADCD16IP<2:0>			ADCD16IS<1:0>			—	—	—	ADCD15IP<2:0>			ADCD15IS<1:0>		0000
		15:0	—	—	—	ADCD14IP<2:0>			ADCD14IS<1:0>			—	—	—	ADCD13IP<2:0>			ADCD13IS<1:0>		0000
0270	IPC19	31:16	—	—	—	ADCD20IP<2:0>(2)			ADCD20IS<1:0>(2)			—	—	—	ADCD19IP<2:0>(2)			ADCD19IS<1:0>(2)		0000
		15:0	—	—	—	ADCD18IP<2:0>			ADCD18IS<1:0>			—	—	—	ADCD17IP<2:0>			ADCD17IS<1:0>		0000
0280	IPC20	31:16	—	—	—	ADCD24IP<2:0>(2)			ADCD24IS<1:0>(2)			—	—	—	ADCD23IP<2:0>(2)			ADCD23IS<1:0>(2)		0000
		15:0	—	—	—	ADCD22IP<2:0>(2)			ADCD22IS<1:0>(2)			—	—	—	ADCD21IP<2:0>(2)			ADCD21IS<1:0>(2)		0000
0290	IPC21	31:16	—	—	—	ADCD28IP<2:0>(2)			ADCD28IS<1:0>(2)			—	—	—	ADCD27IP<2:0>(2)			ADCD27IS<1:0>(2)		0000
		15:0	—	—	—	ADCD26IP<2:0>(2)			ADCD26IS<1:0>(2)			—	—	—	ADCD25IP<2:0>(2)			ADCD25IS<1:0>(2)		0000
02A0	IPC22	31:16	—	—	—	ADCD32IP<2:0>(2)			ADCD32IS<1:0>(2)			—	—	—	ADCD31IP<2:0>(2)			ADCD31IS<1:0>(2)		0000
		15:0	—	—	—	ADCD30IP<2:0>(2)			ADCD30IS<1:0>(2)			—	—	—	ADCD29IP<2:0>(2)			ADCD29IS<1:0>(2)		0000
02B0	IPC23	31:16	—	—	—	ADCD36IP<2:0>(2,4)			ADCD36IS<1:0>(2,4)			—	—	—	ADCD35IP<2:0>(2,4)			ADCD35IS<1:0>(2,4)		0000
		15:0	—	—	—	ADCD34IP<2:0>(2)			ADCD34IS<1:0>(2)			—	—	—	ADCD33IP<2:0>(2)			ADCD33IS<1:0>(2)		0000
02C0	IPC24	31:16	—	—	—	ADCD40IP<2:0>(2,4)			ADCD40IS<1:0>(2,4)			—	—	—	ADCD39IP<2:0>(2,4)			ADCD39IS<1:0>(2,4)		0000
		15:0	—	—	—	ADCD38IP<2:0>(2,4)			ADCD38IS<1:0>(2,4)			—	—	—	ADCD37IP<2:0>(2,4)			ADCD37IS<1:0>(2,4)		0000
02D0	IPC25	31:16	—	—	—	ADCD44IP<2:0>			ADCD44IS<1:0>			—	—	—	ADCD43IP<2:0>			ADCD43IS<1:0>		0000
		15:0	—	—	—	ADCD42IP<2:0>(2,4)			ADCD42IS<1:0>(2,4)			—	—	—	ADCD41IP<2:0>(2,4)			ADCD41IS<1:0>(2,4)		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.
- 2: This bit or register is not available on 64-pin devices.
- 3: This bit or register is not available on devices without a CAN module.
- 4: This bit or register is not available on 100-pin devices.
- 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
- 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
- 7: This bit or register is not available on devices without a Crypto module.
- 8: This bit or register is not available on 124-pin devices.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 8-3: SPLLCN: SYSTEM PLL CONTROL REGISTER

bit 10-8 **PLLIDIV<2:0>**: System PLL Input Clock Divider bits

111 = Divide by 8
110 = Divide by 7
101 = Divide by 6
100 = Divide by 5
011 = Divide by 4
010 = Divide by 3
001 = Divide by 2
000 = Divide by 1

The default setting is specified by the FPLLIDIV<2:0> Configuration bits in the DEVCFG2 register. If the PLLICLK is set for FRC, this setting is ignored by the PLL and the divider is set for Divide-by-1. Refer to Register 34-5 in **Section 34.0 “Special Features”** for information.

bit 7 **PLLICLK**: System PLL Input Clock Source bit

1 = FRC is selected as the input to the System PLL
0 = Posc is selected as the input to the System PLL

The POR default is specified by the FPLLICLK Configuration bit in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 “Special Features”** for information.

bit 6-3 **Unimplemented**: Read as '0'

bit 2-0 **PLLRRANGE<2:0>**: System PLL Frequency Range Selection bits

111 = Reserved
110 = Reserved
101 = 34-64 MHz
100 = 21-42 MHz
011 = 13-26 MHz
010 = 8-16 MHz
001 = 5-10 MHz
000 = Bypass

The default setting is specified by the FPLLRRNG<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 “Special Features”** for information.

Note 1: Writes to this register require an unlock sequence. Refer to **Section 42. “Oscillators with Enhanced PLL”** (DS60001250) in the *PIC32 Family Reference Manual* for details.

2: Writes to this register are not allowed if the SPLLCN is selected as a clock source (COSC<2:0> = 001).

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 9-1: PRECON: PREFETCH MODULE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
	—	—	—	—	—	PFMSECEN	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
	—	—	PREFEN<1:0>		—	PFMWS<2:0> ⁽¹⁾		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **PFMSECEN:** Flash SEC Interrupt Enable bit

1 = Generate an interrupt when the PFMSEC bit (PRESTAT<26>) is set

0 = Do not generate an interrupt when the PFMSEC bit is set

bit 25-6 **Unimplemented:** Read as '0'

bit 5-4 **PREFEN<1:0>:** Predictive Prefetch Enable bits

11 = Enable predictive prefetch for any address

10 = Enable predictive prefetch for CPU instructions and CPU data

01 = Enable predictive prefetch for CPU instructions only

00 = Disable predictive prefetch

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **PFMWS<2:0>:** PFM Access Time Defined in Terms of SYSCLK Wait States bits⁽¹⁾

111 = Seven Wait states

•
•
•

010 = Two Wait states

001 = One Wait state

000 = Zero Wait states

Note 1: For the Wait states to SYSCLK relationship, refer to Table 37-13 in **Section 37.0 “Electrical Characteristics”**.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 11-15: USBHWVER: USB HARDWARE VERSION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-1	R-0	R-0	R-0
	RC	VERMAJOR<4:0>					VERMINOR<9:8>	
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERMINOR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **RC:** Release Candidate bit

1 = USB module was created using a release candidate

0 = USB module was created using a full release

bit 14-10 **VERMAJOR<4:0>:** USB Module Major Version number bits

This read-only number is the Major version number for the USB module.

bit 9-0 **VERMINOR<9:0>:** USB Module Minor Version number bits

This read-only number is the Minor version number for the USB module.

TABLE 12-5: PORTB REGISTER MAP

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0100	ANSELB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSB15	ANSB14	ANSB13	ANSB12	ANSB11	ANSB10	ANSB9	ANSB8	ANSB7	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	FFFF
0110	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
0120	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
0130	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
0140	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
0150	CNPUB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
0160	CNPDB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
0170	CNCONB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0180	CNENB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNENB15	CNENB14	CNENB13	CNENB12	CNENB11	CNENB10	CNENB9	CNENB8	CNENB7	CNENB6	CNENB5	CNENB4	CNENB3	CNENB2	CNENB1	CNENB0	0000
0190	CNSTATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATB15	CN STATB14	CN STATB13	CN STATB12	CN STATB11	CN STATB10	CN STATB9	CN STATB8	CN STATB7	CN STATB6	CN STATB5	CN STATB4	CN STATB3	CN STATB2	CN STATB1	CN STATB0	0000
01A0	CNNEB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEB15	CNNEB14	CNNEB13	CNNEB12	CNNEB11	CNNEB10	CNNEB9	CNNEB8	CNNEB7	CNNEB6	CNNEB5	CNNEB4	CNNEB3	CNNEB2	CNNEB1	CNNEB0	0000
01B0	CNFB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFB15	CNFB14	CNFB13	CNFB12	CNFB11	CNFB10	CNFB9	CNFB8	CNFB7	CNFB6	CNFB5	CNFB4	CNFB3	CNFB2	CNFB1	CNFB0	0000
01C0	SRCON0B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	SR0B14	—	—	—	SR0B10	SR0B9	SR0B8	—	—	SR0B5	—	SR0B3	—	—	—	0000
01D0	SRCON1B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	SR1B14	—	—	—	SR1B10	SR1B9	SR1B8	—	—	SR1B5	—	SR1B3	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 20-2: SQI1XCON2: SQI XIP CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DEVSEL<1:0>		MODEBYTES<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MODECODE<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11-10 **DEVSEL<1:0>:** Device Select bits

11 = Reserved

10 = Reserved

01 = Device 1 is selected

00 = Device 0 is selected

bit 9-8 **MODEBYTES<1:0>:** Mode Byte Cycle Enable bits

11 = Three cycles

10 = Two cycles

01 = One cycle

00 = Zero cycles

bit 7-0 **MODECODE<7:0>:** Mode Code Value bits

These bits contain the 8-bit code value for the mode bits.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 20-3: SQI1CFG: SQI CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0
	CSEN<1:0>							
23:16	R/W-0 SQIEN	U-0 —	R/W-0	R/W-0	R/W-0, HC CON FIFORST	R/W-0, HC RX FIFORST	R/W-0, HC TX FIFORST	R/W-0, HC RESET
15:8	U-0 —	r-0 —	r-0 —	R/W-0 BURSTEN ⁽¹⁾	r-0 —	R/W-0 HOLD	R/W-0 WP	U-0 —
7:0	U-0 —	U-0 —	R/W-0 LSBF	R/W-0 CPOL	R/W-0 CPHA	R/W-0	R/W-0	R/W-0 MODE<2:0>

Legend:

R = Readable bit

-n = Value at POR

HC = Hardware Cleared

W = Writable bit

'1' = Bit is set

r = Reserved

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25-24 **CSEN<1:0>:** Chip Select Output Enable bits

11 = Chip Select 0 and Chip Select 1 are used

10 = Chip Select 1 is used (Chip Select 0 is not used)

01 = Chip Select 0 is used (Chip Select 1 is not used)

00 = Chip Select 0 and Chip Select 1 are not used

bit 23 **SQIEN:** SQI Enable bit

1 = SQI module is enabled

0 = SQI module is disabled

bit 22 **Unimplemented:** Read as '0'

bit 21-20 **DATAEN<1:0>:** Data Output Enable bits

11 = Reserved

10 = SQID3-SQID0 outputs are enabled

01 = SQID1 and SQID0 data outputs are enabled

00 = SQID0 data output is enabled

bit 19 **CONFIFORST:** Control FIFO Reset bit

1 = A reset pulse is generated clearing the control FIFO

0 = A reset pulse is not generated

bit 18 **RXFIFORST:** Receive FIFO Reset bit

1 = A reset pulse is generated clearing the receive FIFO

0 = A reset pulse is not generated

bit 17 **TXFIFORST:** Transmit FIFO Reset bit

1 = A reset pulse is generated clearing the transmit FIFO

0 = A reset pulse is not generated

bit 16 **RESET:** Software Reset Select bit

This bit is automatically cleared by the SQI module. All of the internal state machines and FIFO pointers are reset by this reset pulse.

1 = A reset pulse is generated

0 = A reset pulse is not generated

bit 15 **Unimplemented:** Read as '0'

bit 14-13 **Reserved:** Must be programmed as '0'

Note 1: This bit must be programmed as '1'.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 20-24: SQI1MEMSTAT: SQI MEMORY STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	R/W-0 STATPOS	R/W-0 STATTYPE<1:0>	R/W-0 STATTYPE<1:0>	R/W-0 STATBYTES<1:0>	R/W-0 STATBYTES<1:0>
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STATDATA<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STATCMD<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **STATPOS:** Status Bit Position in Flash bit

Indicates the BUSY bit position in the Flash Status register. This bit is added to support all Flash types (with BUSY bit at 0 and at 7).

1 = BUSY bit position is bit 7 in status register

0 = BUSY bit position is bit 0 in status register

bit 19-18 **STATTYPE<1:0>:** Status Command/Read Lane Mode bits

11 = Reserved

10 = Status command and read are executed in Quad Lane mode

01 = Status command and read are executed in Dual Lane mode

00 = Status command and read are executed in Single Lane mode

bit 17-16 **STATBYTES<1:0>:** Number of Status Bytes bits

11 = Reserved

10 = Status command/read is 2 bytes long

01 = Status command/read is 1 byte long

00 = Reserved

bit 15-8 **STATDATA<7:0>:** Status Data bits

These bits contain the status value of the Flash device

bit 7-0 **STATCMD<7:0>:** Status Command bits

The status check command is written into these bits

26.1 Crypto Engine Control Registers

TABLE 26-2: CRYPTO ENGINE REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5000	CEVER	31:16	REVISION<7:0>								VERSION<7:0>								0000
		15:0	ID<15:0>																0000
5004	CECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	SWAPOEN	SWRST	SWAPEN	—	—	BDPCHST	BDPPLEN	DMAEN	0000
5008	CEBDADDR	31:16	BDPADDR<31:0>																0000
		15:0																	0000
500C	CEBDPADDR	31:16	BASEADDR<31:0>																0000
		15:0																	0000
5010	CESTAT	31:16	ERRMODE<2:0>			ERROP<2:0>			ERRPHASE<1:0>		—	—	BDSTATE<3:0>			START	ACTIVE	0000	
		15:0	BDCTRL<15:0>																0000
5014	CEINTSRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIF	PKTIF	CBDIF	PENDIF	0000
5018	CEINTEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIE	PKTIE	CBDIE	PENDIE	0000
501C	CEPOLLCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	BDPPLCON<15:0>																0000
5020	CEHDLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	HDRLEN<7:0>								0000
5024	CETRLLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	TRLRLLEN<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

28.1 ADC Control Registers

TABLE 28-1: ADC REGISTER MAP

Virtual Address (BF84_#)	Register Name	Bit Range	Bits															All Resets			
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0		
B000	ADCCON1	31:16	TRBEN	TRBERR	TRBMST<2:0>			TRBSLV<2:0>			FRACT	SELRES<1:0>			STRGSRC<4:0>				0060		
		15:0	ON	—	SIDL	AICMPEN	CVDEN	FSSCLKEN	FSPBCLKEN	—	—	IRQVS<2:0>			STRGLVL	—	—	—	1000		
B004	ADCCON2	31:16	BGVRRDY	REFFLT	EOSRDY	CVDCLP<2:0>			SAMC<9:0>									0000			
		15:0	BGVRIEN	REFFLTEN	EOSIEN	ADCEIOVR	—	ADCEIS<2:0>			—	ADCCDIV<6:0>									0000
B008	ADCCON3	31:16	ADCSEL<1:0>		CONCLKDIV<5:0>						DIGEN7	—	—	—	DIGEN4	DIGEN3	DIGEN2	DIGEN1	DIGEN0	0000	
		15:0	VREFSEL<2:0>			TRGSUSP	UPDIEN	UPDRDY	SAMP	RQCNVRT	GLSWTRG	GSWTRG	ADINSEL<5:0>							0000	
B00C	ADCTRGMODE	31:16	—	—	—	—	—	—	SH4ALT<1:0>		SH3ALT<1:0>		SH2ALT<1:0>		SH1ALT<1:0>		SH0ALT<1:0>		0000		
		15:0	—	—	—	STRGEN4	STRGEN3	STRGEN2	STRGEN1	STRGEN0	—	—	—	SSAMPEN4	SSAMPEN3	SSAMPEN2	SSAMPEN1	SSAMPEN0	0000		
B010	ADCIMCON1	31:16	DIFF15	SIGN15	DIFF14	SIGN14	DIFF13	SIGN13	DIFF12	SIGN12	DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8	0000		
		15:0	DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4	DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0	0000		
B014	ADCIMCON2	31:16	DIFF31 ⁽¹⁾	SIGN31 ⁽¹⁾	DIFF30 ⁽¹⁾	SIGN30 ⁽¹⁾	DIFF29 ⁽¹⁾	SIGN29 ⁽¹⁾	DIFF28 ⁽¹⁾	SIGN28 ⁽¹⁾	DIFF27 ⁽¹⁾	SIGN27 ⁽¹⁾	DIFF26 ⁽¹⁾	SIGN26 ⁽¹⁾	DIFF25 ⁽¹⁾	SIGN25 ⁽¹⁾	DIFF24 ⁽¹⁾	SIGN24 ⁽¹⁾	0000		
		15:0	DIFF23 ⁽¹⁾	SIGN23 ⁽¹⁾	DIFF22 ⁽¹⁾	SIGN22 ⁽¹⁾	DIFF21 ⁽¹⁾	SIGN21 ⁽¹⁾	DIFF20 ⁽¹⁾	SIGN20 ⁽¹⁾	DIFF19 ⁽¹⁾	SIGN19 ⁽¹⁾	DIFF18	SIGN18	DIFF17	SIGN17	DIFF16	SIGN16	0000		
B018	ADCIMCON3	31:16	—	—	—	—	—	—	DIFF44	SIGN44	DIFF43	SIGN43	DIFF42 ⁽²⁾	SIGN42 ⁽²⁾	DIFF41 ⁽²⁾	SIGN41 ⁽²⁾	DIFF40 ⁽²⁾	SIGN40 ⁽²⁾	0000		
		15:0	DIFF39 ⁽²⁾	SIGN39 ⁽²⁾	DIFF38 ⁽²⁾	SIGN38 ⁽²⁾	DIFF37 ⁽²⁾	SIGN37 ⁽²⁾	DIFF36 ⁽²⁾	SIGN36 ⁽²⁾	DIFF35 ⁽²⁾	SIGN35 ⁽²⁾	DIFF34 ⁽¹⁾	SIGN34 ⁽¹⁾	DIFF33 ⁽¹⁾	SIGN33 ⁽¹⁾	DIFF32 ⁽¹⁾	SIGN32 ⁽¹⁾	0000		
B020	ADCGIRQEN1	31:16	AGIEN31 ⁽¹⁾	AGIEN30 ⁽¹⁾	AGIEN29 ⁽¹⁾	AGIEN28 ⁽¹⁾	AGIEN27 ⁽¹⁾	AGIEN26 ⁽¹⁾	AGIEN25 ⁽¹⁾	AGIEN24 ⁽¹⁾	AGIEN23 ⁽¹⁾	AGIEN22 ⁽¹⁾	AGIEN21 ⁽¹⁾	AGIEN20 ⁽¹⁾	AGIEN19 ⁽¹⁾	AGIEN18	AGIEN17	AGIEN16	0000		
		15:0	AGIEN15	AGIEN14	AGIEN13	AGIEN12	AGIEN11	AGIEN10	AGIEN9	AGIEN8	AGIEN7	AGIEN6	AGIEN5	AGIEN4	AGIEN3	AGIEN2	AGIEN1	AGIEN0	0000		
B024	ADCGIRQEN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	—	—	—	AGIEN44	AGIEN43	AGIEN42 ⁽²⁾	AGIEN41 ⁽²⁾	AGIEN40 ⁽²⁾	AGIEN39 ⁽²⁾	AGIEN38 ⁽²⁾	AGIEN37 ⁽²⁾	AGIEN36 ⁽²⁾	AGIEN35 ⁽²⁾	AGIEN34 ⁽¹⁾	AGIEN33 ⁽¹⁾	AGIEN32 ⁽¹⁾	0000		
B028	ADCCSS1	31:16	CSS31 ⁽¹⁾	CSS30 ⁽¹⁾	CSS29 ⁽¹⁾	CSS28 ⁽¹⁾	CSS27 ⁽¹⁾	CSS26 ⁽¹⁾	CSS25 ⁽¹⁾	CSS24 ⁽¹⁾	CSS23 ⁽¹⁾	CSS22 ⁽¹⁾	CSS21 ⁽¹⁾	CSS20 ⁽¹⁾	CSS19 ⁽¹⁾	CSS18	CSS17	CSS16	0000		
		15:0	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000		
B02C	ADCCSS2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	—	—	—	CSS44	CSS43	CSS42 ⁽²⁾	CSS41 ⁽²⁾	CSS40 ⁽²⁾	CSS39 ⁽²⁾	CSS38 ⁽²⁾	CSS37 ⁽²⁾	CSS36 ⁽²⁾	CSS35 ⁽²⁾	CSS34 ⁽¹⁾	CSS33 ⁽¹⁾	CSS32 ⁽¹⁾	0000		
B030	ADCDSTAT1	31:16	ARDY31 ⁽¹⁾	ARDY30 ⁽¹⁾	ARDY29 ⁽¹⁾	ARDY28 ⁽¹⁾	ARDY27 ⁽¹⁾	ARDY26 ⁽¹⁾	ARDY25 ⁽¹⁾	ARDY24 ⁽¹⁾	ARDY23 ⁽¹⁾	ARDY22 ⁽¹⁾	ARDY21 ⁽¹⁾	ARDY20 ⁽¹⁾	ARDY19 ⁽¹⁾	ARDY18	ARDY17	ARDY16	0000		
		15:0	ARDY15	ARDY14	ARDY13	ARDY12	ARDY11	ARDY10	ARDY9	ARDY8	ARDY7	ARDY6	ARDY5	ARDY4	ARDY3	ARDY2	ARDY1	ARDY0	0000		
B034	ADCDSTAT2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	—	—	—	ARDY44	ARDY43	ARDY42 ⁽²⁾	ARDY41 ⁽²⁾	ARDY40 ⁽²⁾	ARDY39 ⁽²⁾	ARDY38 ⁽²⁾	ARDY37 ⁽²⁾	ARDY36 ⁽²⁾	ARDY35 ⁽²⁾	ARDY34 ⁽¹⁾	ARDY33 ⁽¹⁾	ARDY32 ⁽¹⁾	0000		
B038	ADCCMPEN1	31:16	CMPE31 ⁽¹⁾	CMPE30 ⁽¹⁾	CMPE29 ⁽¹⁾	CMPE28 ⁽¹⁾	CMPE27 ⁽¹⁾	CMPE26 ⁽¹⁾	CMPE25 ⁽¹⁾	CMPE24 ⁽¹⁾	CMPE23 ⁽¹⁾	CMPE22 ⁽¹⁾	CMPE21 ⁽¹⁾	CMPE20 ⁽¹⁾	CMPE19 ⁽¹⁾	CMPE18	CMPE17	CMPE16	0000		
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000		
B03C	ADCCMP1	31:16	DCMPHI<15:0>																0000		
		15:0	DCMPLO<15:0>																0000		
B040	ADCCMPEN2	31:16	CMPE31 ⁽¹⁾	CMPE30 ⁽¹⁾	CMPE29 ⁽¹⁾	CMPE28 ⁽¹⁾	CMPE27 ⁽¹⁾	CMPE26 ⁽¹⁾	CMPE25 ⁽¹⁾	CMPE24 ⁽¹⁾	CMPE23 ⁽¹⁾	CMPE22 ⁽¹⁾	CMPE21 ⁽¹⁾	CMPE20 ⁽¹⁾	CMPE19 ⁽¹⁾	CMPE18	CMPE17	CMPE16	0000		
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000		
B044	ADCCMP2	31:16	DCMPHI<15:0>																0000		
		15:0	DCMPLO<15:0>																0000		
B048	ADCCMPEN3	31:16	CMPE31 ⁽¹⁾	CMPE30 ⁽¹⁾	CMPE29 ⁽¹⁾	CMPE28 ⁽¹⁾	CMPE27 ⁽¹⁾	CMPE26 ⁽¹⁾	CMPE25 ⁽¹⁾	CMPE24 ⁽¹⁾	CMPE23 ⁽¹⁾	CMPE22 ⁽¹⁾	CMPE21 ⁽¹⁾	CMPE20 ⁽¹⁾	CMPE19 ⁽¹⁾	CMPE18	CMPE17	CMPE16	0000		
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000		

Note

- 1: This bit or register is not available on 64-pin devices.
- 2: This bit or register is not available on 64-pin and 100-pin devices.
- 3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

REGISTER 28-3: ADCCON3: ADC CONTROL REGISTER 3 (CONTINUED)

bit 18 **DIGEN2:** ADC2 Digital Enable bit
1 = ADC2 is digital enabled
0 = ADC2 is digital disabled

bit 17 **DIGEN1:** ADC1 Digital Enable bit
1 = ADC1 is digital enabled
0 = ADC1 is digital disabled

bit 16 **DIGEN0:** ADC0 Digital Enable bit
1 = ADC0 is digital enabled
0 = ADC0 is digital disabled

bit 15-13 **VREFSEL<2:0>:** Voltage Reference (VREF) Input Selection bits

VREFSEL<2:0>	ADREF+	ADREF-
1xx	Reserved; do not use	
011	External VREFH	External VREFL
010	AVDD	External VREFL
001	External VREFH	AVss
000	AVDD	AVss

bit 12 **TRGSUSP:** Trigger Suspend bit
1 = Triggers are blocked from starting a new analog-to-digital conversion, but the ADC module is not disabled
0 = Triggers are not blocked

bit 11 **UPDIEN:** Update Ready Interrupt Enable bit
1 = Interrupt will be generated when the UPDRDY bit is set by hardware
0 = No interrupt is generated

bit 10 **UPDRDY:** ADC Update Ready Status bit
1 = ADC SFRs can be updated
0 = ADC SFRs cannot be updated

Note: This bit is only active while the TRGSUSP bit is set and there are no more running conversions of any ADC modules.

bit 9 **SAMP:** Class 2 and Class 3 Analog Input Sampling Enable bit^(1,2,3,4)
1 = The ADC S&H amplifier is sampling
0 = The ADC S&H amplifier is holding

bit 8 **RQCNVRT:** Individual ADC Input Conversion Request bit
This bit and its associated ADINSEL<5:0> bits enable the user to individually request an analog-to-digital conversion of an analog input through software.
1 = Trigger the conversion of the selected ADC input as specified by the ADINSEL<5:0> bits
0 = Do not trigger the conversion

Note: This bit is automatically cleared in the next ADC clock cycle.

bit 7 **GLSWTRG:** Global Level Software Trigger bit
1 = Trigger conversion for ADC inputs that have selected the GLSWTRG bit as the trigger signal, either through the associated TRGSRC<4:0> bits in the ADCTRGx registers or through the STRGSRC<4:0> bits in the ADCCON1 register
0 = Do not trigger an analog-to-digital conversion

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit will cause settings of SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

2: The SAMP bit only connects Class 2 and Class 3 analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

3: The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion.

4: Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx<4:0> bits and STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

REGISTER 29-17: C_iFLTCON7: CAN FILTER CONTROL REGISTER 7 (CONTINUED)

- bit 15 **FLTEN29**: Filter 29 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 14-13 **MSEL29<1:0>**: Filter 29 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 12-8 **FSEL29<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 •
 •
 •
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0
- bit 7 **FLTEN28**: Filter 28 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 6-5 **MSEL28<1:0>**: Filter 28 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 4-0 **FSEL28<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 •
 •
 •
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTEN _n) bit is '0'.
--

32.1 Comparator Voltage Reference Control Registers

TABLE 32-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0E00	CVRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	CVROE	CVRR	CVRSS	CVR<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 34-5: DEVCFG2/ADEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1 —	R/P UPLLFSEL	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —
23:16	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	R/P FPLLODIV<2:0>	R/P	R/P
15:8	r-1 —	R/P	R/P	R/P	R/P	R/P	R/P	R/P
7:0	R/P FPLLICK	R/P	R/P	R/P	r-1 —	R/P	R/P	R/P
		FPLLCLK				FPLLIDIV<2:0>		

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 31 **Reserved:** Write as '1'
- bit 30 **UPLLFSEL:** USB PLL Input Frequency Select bit
1 = UPLL input clock is 24 MHz
0 = UPLL input clock is 12 MHz
- bit 29-19 **Reserved:** Write as '1'
- bit 18-16 **FPLLODIV<2:0>:** Default System PLL Output Divisor bits
111 = PLL output divided by 32
110 = PLL output divided by 32
101 = PLL output divided by 32
100 = PLL output divided by 16
011 = PLL output divided by 8
010 = PLL output divided by 4
001 = PLL output divided by 2
000 = PLL output divided by 2
- bit 15 **Reserved:** Write as '1'
- bit 14-8 **FPLLMULT<6:0>:** System PLL Feedback Divider bits
1111111 = Multiply by 128
1111110 = Multiply by 127
1111101 = Multiply by 126
1111100 = Multiply by 125
•
•
•
0000000 = Multiply by 1
- bit 7 **FPLLICK:** System PLL Input Clock Select bit
1 = FRC is selected as input to the System PLL
0 = Posc is selected as input to the System PLL
- bit 6-4 **FPLLNRNG<2:0>:** System PLL Divided Input Clock Frequency Range bits
111 = Reserved
110 = Reserved
101 = 34-64 MHz
100 = 21-42 MHz
011 = 13-26 MHz
010 = 8-16 MHz
001 = 5-10 MHz
000 = Bypass

36.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

36.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

36.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

36.9 PICkit 3 In-Circuit Debugger/Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

36.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

FIGURE 37-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS

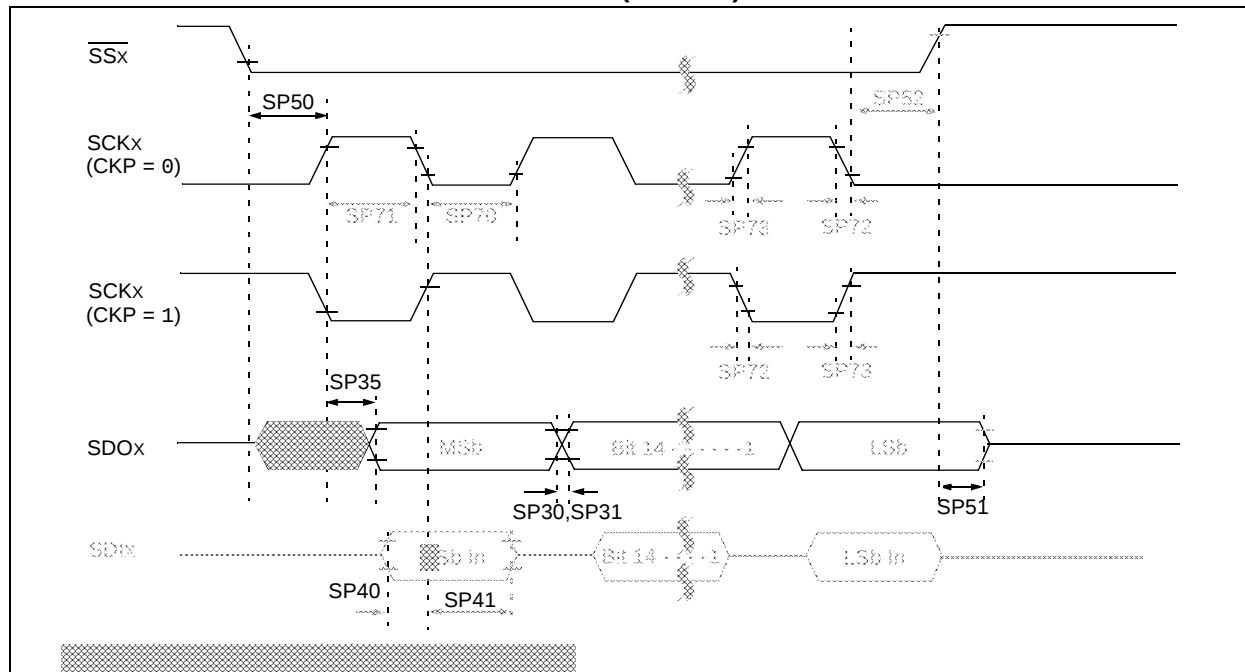


TABLE 37-32: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	TscL	SCKx Input Low Time (Note 3)	Tsck/2	—	—	ns	—
SP71	Tsch	SCKx Input High Time (Note 3)	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See parameter DO32
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See parameter DO31
SP30	Tdof	SDOx Data Output Fall Time (Note 4)	—	—	—	ns	See parameter DO32
SP31	Tdor	SDOx Data Output Rise Time (Note 4)	—	—	—	ns	See parameter DO31
SP35	Tsch2boV, TscL2boV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	VDD > 2.7V
			—	—	10	ns	VDD < 2.7V
SP40	TdIV2sch, TdIV2scL	Setup Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP50	Tssl2sch, Tssl2scL	SSx ↓ to SCKx ↑ or SCKx Input	88	—	—	ns	—
SP51	TssH2boZ	SSx ↑ to SDOx Output High-Impedance (Note 3)	2.5	—	12	ns	—
SP52	Tsch2ssh, TscL2ssh	SSx after SCKx Edge	10	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 20 ns.

4: Assumes 30 pF load on all SPIx pins.

FIGURE 37-20: CANx MODULE I/O TIMING CHARACTERISTICS

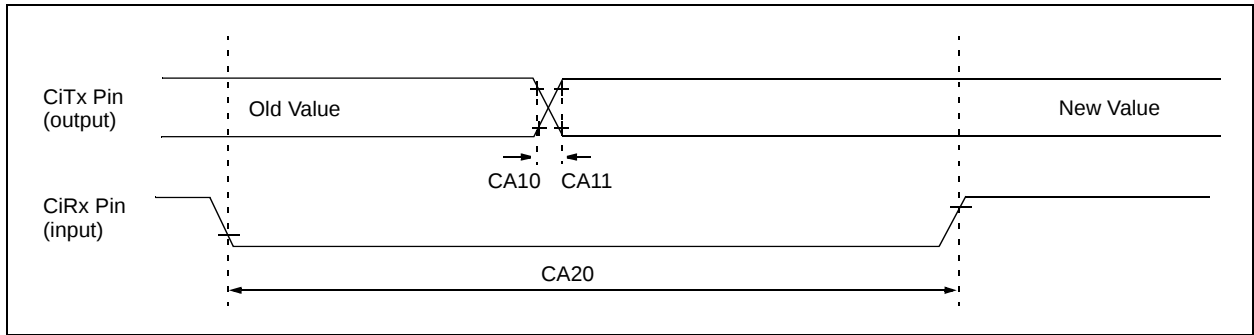


TABLE 37-37: CANx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated)				
			Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
CA10	TioF	Port Output Fall Time	—	—	—	ns	See parameter DO32
CA11	TioR	Port Output Rise Time	—	—	—	ns	See parameter DO31
CA20	Tcwf	Pulse Width to Trigger CAN Wake-up Filter	700	—	—	ns	—

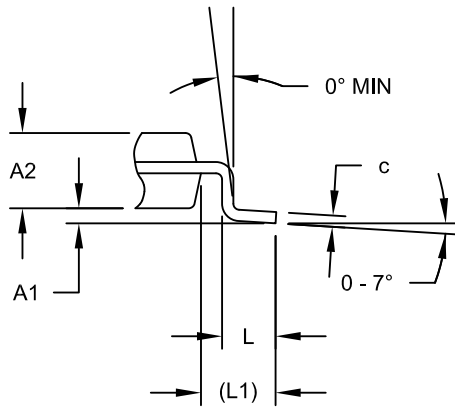
Note 1: These parameters are characterized but not tested in manufacturing.

Note 2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

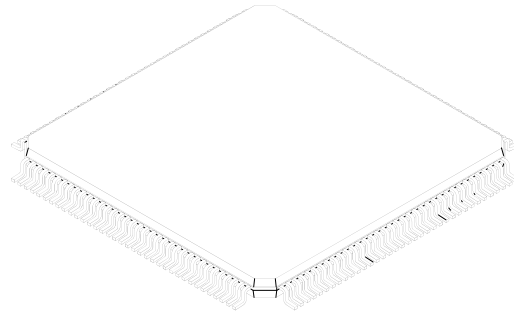
PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

144-Lead Plastic Thin Quad Flatpack (PH)-16x16x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



DETAIL A



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	144		
Lead Pitch	e	0.40 BSC		
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Overall Width	D	18.00 BSC		
Overall Length	E	18.00 BSC		
Molded Body Width	D1	16.00 BSC		
Molded Body Length	E1	16.00 BSC		
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.13	-	0.23

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-155B Sheet 2 of 2

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

A.4 Resets

The PIC32MZ EF family of devices has updated the resets modules to incorporate the new handling of NMI resets from the WDT, DMT, and the FSCM. In addition, some bits have been moved, as summarized in Table A-5.

TABLE A-5: RESET DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Power Reset	
VREGS (RCON<8>) 1 = Regulator is enabled and is on during Sleep mode 0 = Regulator is disabled and is off during Sleep mode	The VREGS bit, which controls whether the internal regulator is enabled in Sleep mode, has been moved from RCON in PIC32MX5XX/6XX/7XX devices to a new PWRCON register in PIC32MZ EF devices. VREGS (PWRCON<0>) 1 = Voltage regulator will remain active during Sleep 0 = Voltage regulator will go to Stand-by mode during Sleep
Watchdog Timer Reset	
On PIC32MX devices, a WDT expiration immediately triggers a device reset. WDT expiration immediately causes a device reset.	On PIC32MZ EF devices, the WDT expiration now causes a NMI. The WDTO bit in RNMICON indicates that the WDT caused the NMI. A new timer, NMICNT, runs when the WDT NMI is triggered, and if it expires, the device is reset. WDT expiration causes a NMI, which can then trigger the device reset. WDTO (RNMICON<24>) 1 = WDT time-out has occurred and caused a NMI 0 = WDT time-out has not occurred NMICNT<7:0> (RNMICON<7:0>)

A.5 USB

The PIC32MZ EF family of devices has a new Hi-Speed USB module, which requires the updated USB stack from Microchip. In addition, the USB PLL was also updated. See **A.1 “Oscillator and PLL Configuration”** for more information and Table A-6 for a list of additional differences.

TABLE A-6: USB DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Debug Mode	
On PIC32MX devices, when stopping on a breakpoint during debugging, the USB module can be configured to stop or continue execution from the Freeze Peripherals dialog in MPLAB X IDE.	On PIC32MZ EF devices, the USB module continues operating when stopping on a breakpoint during debugging.
VBUSON Pin	
PIC32MX devices feature a VBUSON pin for controlling the external transceiver power supply.	On PIC32MZ EF devices, the VBUSON pin is not available. A port pin can be used to achieve the same functionality.