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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efh144t-i-ph

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTD							
RD0	46	71	A48	104	I/O	ST	PORTD is a bidirectional I/O port
RD1	49	76	A52	109	I/O	ST	
RD2	50	77	B42	110	I/O	ST	
RD3	51	78	A53	111	I/O	ST	
RD4	52	81	A56	118	I/O	ST	
RD5	53	82	B46	119	I/O	ST	
RD6	—	—	A57	120	I/O	ST	
RD7	—	—	B47	121	I/O	ST	
RD9	43	68	B38	97	I/O	ST	
RD10	44	69	A46	98	I/O	ST	
RD11	45	70	B39	99	I/O	ST	
RD12	—	79	B43	112	I/O	ST	
RD13	—	80	A54	113	I/O	ST	
RD14	—	47	B27	69	I/O	ST	
RD15	—	48	A32	70	I/O	ST	
PORTE							
RE0	58	91	B52	135	I/O	ST	PORTE is a bidirectional I/O port
RE1	61	94	A64	138	I/O	ST	
RE2	62	98	A66	142	I/O	ST	
RE3	63	99	B56	143	I/O	ST	
RE4	64	100	A67	144	I/O	ST	
RE5	1	3	A3	3	I/O	ST	
RE6	2	4	B2	4	I/O	ST	
RE7	3	5	A4	5	I/O	ST	
RE8	—	18	B10	23	I/O	ST	
RE9	—	19	A12	24	I/O	ST	
PORTF							
RF0	56	85	A59	124	I/O	ST	PORTF is a bidirectional I/O port
RF1	57	86	B49	125	I/O	ST	
RF2	—	57	B31	79	I/O	ST	
RF3	38	56	A38	78	I/O	ST	
RF4	41	64	B36	90	I/O	ST	
RF5	42	65	A44	91	I/O	ST	
RF8	—	58	A39	80	I/O	ST	
RF12	—	40	B22	58	I/O	ST	
RF13	—	39	A26	57	I/O	ST	

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 1-20: SQI1 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/LQFP			
SQICLK	57	89	A61	129	O	—	Serial Quad Interface Clock
SQICS0	52	81	A56	118	O	—	Serial Quad Interface Chip Select 0
SQICS1	53	82	B46	119	O	—	Serial Quad Interface Chip Select 1
SQID0	58	97	B55	141	I/O	ST	Serial Quad Interface Data 0
SQID1	61	96	A65	140	I/O	ST	Serial Quad Interface Data 1
SQID2	62	95	B54	139	I/O	ST	Serial Quad Interface Data 2
SQID3	63	90	B51	130	I/O	ST	Serial Quad Interface Data 3

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

TABLE 1-21: POWER, GROUND, AND VOLTAGE REFERENCE PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Power and Ground							
AVDD	19	30	B16	41	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	20	31	A21	42	P	P	Ground reference for analog modules. This pin must be connected at all times
VDD	8, 26, 39, 54, 60	14, 37, 46, 62, 74, 83, 93	B8, A15, A25, B25, B35, A50, A58, B53	18, 33, 55, 64, 88, 107, 122, 137	P	—	Positive supply for peripheral logic and I/O pins. This pin must be connected at all times.
VSS	7, 25, 35, 40, 55, 59	13, 36, 45, 53, 63, 75, 84, 92	A9, B13, B20, B29, A29, A43, A51, B48, A63	17, 32, 54, 63, 75, 89, 108, 123, 136	P	—	Ground reference for logic, I/O pins, and USB. This pin must be connected at all times.
Voltage Reference							
VREF+	16	29	A20	40	I	Analog	Analog Voltage Reference (High) Input
VREF-	15	28	B15	39	I	Analog	Analog Voltage Reference (Low) Input

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 3-2: CONFIG1: CONFIGURATION REGISTER 1; CP0 REGISTER 16, SELECT 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1 —	R-0	R-0	R-1	R-1	R-1	R-1	R-0
	MMU Size<5:0>							IS<2>
23:16	R-1	R-0	R-0	R-1	R-1	R-0	R-1	R-1
	IS<1:0>		IL<2:0>			IA<2:0>		
15:8	R-0	R-0	R-0	R-0	R-1	R-1	R-0	R-1
	DS<2:0>			DL<2:0>			DA<2:1>	
7:0	R-1 DA<0>	U-0 —	U-0 —	R-1 PC	R-1 WR	R-0 CA	R-1 EP	R-1 FP

Legend:	r = Reserved bit
R = Readable bit	W = Writable bit
-n = Value at POR	U = Unimplemented bit, read as '0'
	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to a '1' to indicate the presence of the Config2 register.

bit 30-25 **MMU Size<5:0>:** Contains the number of TLB entries minus 1

001111 = 16 TLB entries

bit 24-22 **IS<2:0>:** Instruction Cache Sets bits

010 = Contains 256 instruction cache sets per way

bit 21-19 **IL<2:0>:** Instruction-Cache Line bits

011 = Contains instruction cache line size of 16 bytes

bit 18-16 **IA<2:0>:** Instruction-Cache Associativity bits

011 = Contains 4-way instruction cache associativity

bit 15-13 **DS<2:0>:** Data-Cache Sets bits

000 = Contains 64 data cache sets per way

bit 12-10 **DL<2:0>:** Data-Cache Line bits

011 = Contains data cache line size of 16 bytes

bit 9-7 **DA<2:0>:** Data-Cache Associativity bits

011 = Contains the 4-way set associativity for the data cache

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **PC:** Performance Counter bit

1 = The processor core contains Performance Counters

bit 3 **WR:** Watch Register Presence bit

1 = No Watch registers are present

bit 2 **CA:** Code Compression Implemented bit

0 = No MIPS16e® present

bit 1 **EP:** EJTAG Present bit

1 = Core implements EJTAG

bit 0 **FP:** Floating Point Unit bit

1 = Floating Point Unit is present

TABLE 4-6: SYSTEM BUS TARGETS AND ASSOCIATED PROTECTION REGISTERS

Target Number	Target Description ⁽⁵⁾	SBTxREGy Register							SBTxRDy Register		SBTxWRy Register	
		Name	Region Base (BASE<21:0>) (see Note 2)	Physical Start Address	Region Size (SIZE<4:0>) (see Note 3)	Region Size	Priority (PRI)	Priority Level	Name	Read Permission (GROUP3, GROUP2, GROUP1, GROUP0)	Name	Write Permission (GROUP3, GROUP2, GROUP1, GROUP0)
0	System Bus	SBT0REG0	R	0x1F8F0000	R	64 KB	—	0	SBT0RD0	R/W ⁽¹⁾	SBT0WR0	R/W ⁽¹⁾
		SBT0REG1	R	0x1F8F8000	R	32 KB	—	3	SBT0RD1	R/W ⁽¹⁾	SBT0WR1	R/W ⁽¹⁾
1	Flash Memory ⁽⁶⁾ : Program Flash Boot Flash Prefetch Module	SBT1REG0	R	0x1D000000	R ⁽⁴⁾	R ⁽⁴⁾	—	0	SBT1RD0	R/W ⁽¹⁾	SBT1WR0	0, 0, 0, 0
		SBT1REG2	R	0x1F8E0000	R	4 KB	1	2	SBT1RD2	R/W ⁽¹⁾	SBT1WR2	R/W ⁽¹⁾
		SBT1REG3	R/W	R/W	R/W	R/W	1	2	SBT1RD3	R/W ⁽¹⁾	SBT1WR3	0, 0, 0, 0
		SBT1REG4	R/W	R/W	R/W	R/W	1	2	SBT1RD4	R/W ⁽¹⁾	SBT1WR4	0, 0, 0, 0
		SBT1REG5	R/W	R/W	R/W	R/W	1	2	SBT1RD5	R/W ⁽¹⁾	SBT1WR5	0, 0, 0, 0
		SBT1REG6	R/W	R/W	R/W	R/W	1	2	SBT1RD6	R/W ⁽¹⁾	SBT1WR6	0, 0, 0, 0
		SBT1REG7	R/W	R/W	R/W	R/W	0	1	SBT1RD7	R/W ⁽¹⁾	SBT1WR7	0, 0, 0, 0
		SBT1REG8	R/W	R/W	R/W	R/W	0	1	SBT1RD8	R/W ⁽¹⁾	SBT1WR8	0, 0, 0, 0
2	RAM Bank 1 Memory	SBT2REG0	R	0x00000000	R ⁽⁴⁾	R ⁽⁴⁾	—	0	SBT2RD0	R/W ⁽¹⁾	SBT2WR0	R/W ⁽¹⁾
		SBT2REG1	R/W	R/W	R/W	R/W	—	3	SBT2RD1	R/W ⁽¹⁾	SBT2WR1	R/W ⁽¹⁾
		SBT2REG2	R/W	R/W	R/W	R/W	0	1	SBT2RD2	R/W ⁽¹⁾	SBT2WR2	R/W ⁽¹⁾
3	RAM Bank 2 Memory	SBT3REG0	R ⁽⁴⁾	R ⁽⁴⁾	R ⁽⁴⁾	R ⁽⁴⁾	—	0	SBT3RD0	R/W ⁽¹⁾	SBT3WR0	R/W ⁽¹⁾
		SBT3REG1	R/W	R/W	R/W	R/W	—	3	SBT3RD1	R/W ⁽¹⁾	SBT3WR1	R/W ⁽¹⁾
		SBT3REG2	R/W	R/W	R/W	R/W	0	1	SBT3RD2	R/W ⁽¹⁾	SBT3WR2	R/W ⁽¹⁾
4	External Memory via EBI and EBI Module ⁽⁶⁾	SBT4REG0	R	0x20000000	R	64 MB	—	0	SBT4RD0	R/W ⁽¹⁾	SBT4WR0	R/W ⁽¹⁾
		SBT4REG2	R	0x1F8E1000	R	4 KB	0	1	SBT4RD2	R/W ⁽¹⁾	SBT4WR2	R/W ⁽¹⁾
5	Peripheral Set 1: System Control Flash Control DMT/WDT RTCC CVR PPS Input PPS Output Interrupts DMA	SBT5REG0	R	0x1F800000	R	128 KB	—	0	SBT5RD0	R/W ⁽¹⁾	SBT5WR0	R/W ⁽¹⁾
		SBT5REG1	R/W	R/W	R/W	R/W	—	3	SBT5RD1	R/W ⁽¹⁾	SBT5WR1	R/W ⁽¹⁾
		SBT5REG2	R/W	R/W	R/W	R/W	0	1	SBT5RD2	R/W ⁽¹⁾	SBT5WR2	R/W ⁽¹⁾

Legend: R = Read; R/W = Read/Write; 'x' in a register name = 0-13; 'y' in a register name = 0-8.

Note 1: Reset values for these bits are '0', '1', '1', '1', respectively.

Note 2: The BASE<21:0> bits must be set to the corresponding Physical Address and right shifted by 10 bits. For Read-only bits, this value is set by hardware on Reset.

Note 3: The SIZE<4:0> bits must be set to the corresponding Region Size, based on the following formula: Region Size = $2^{(SIZE-1)} \times 1024$ bytes. For read-only bits, this value is set by hardware on Reset.

Note 4: Refer to the Device Memory Maps (Figure 4-1 through Figure 4-4) for specific device memory sizes and start addresses.

Note 5: See Table 4-1 for information on specific target memory size and start addresses.

Note 6: The SBTxREG1 SFRs are reserved, and therefore, are not listed in this table for this target.

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Digital Comparator 5	_ADC_DC5_VECTOR	50	OFF050<17:1>	IFS1<18>	IEC1<18>	IPC12<20:18>	IPC12<17:16>	Yes
ADC Digital Comparator 6	_ADC_DC6_VECTOR	51	OFF051<17:1>	IFS1<19>	IEC1<19>	IPC12<28:26>	IPC12<25:24>	Yes
ADC Digital Filter 1	_ADC_DF1_VECTOR	52	OFF052<17:1>	IFS1<20>	IEC1<20>	IPC13<4:2>	IPC13<1:0>	Yes
ADC Digital Filter 2	_ADC_DF2_VECTOR	53	OFF053<17:1>	IFS1<21>	IEC1<21>	IPC13<12:10>	IPC13<9:8>	Yes
ADC Digital Filter 3	_ADC_DF3_VECTOR	54	OFF054<17:1>	IFS1<22>	IEC1<22>	IPC13<20:18>	IPC13<17:16>	Yes
ADC Digital Filter 4	_ADC_DF4_VECTOR	55	OFF055<17:1>	IFS1<23>	IEC1<23>	IPC13<28:26>	IPC13<25:24>	Yes
ADC Digital Filter 5	_ADC_DF5_VECTOR	56	OFF056<17:1>	IFS1<24>	IEC1<24>	IPC14<4:2>	IPC14<1:0>	Yes
ADC Digital Filter 6	_ADC_DF6_VECTOR	57	OFF057<17:1>	IFS1<25>	IEC1<25>	IPC14<12:10>	IPC14<9:8>	Yes
ADC Fault	_ADC_FAULT_VECTOR	58	OFF058<17:1>	IFS1<26>	IEC1<26>	IPC14<20:18>	IPC14<17:16>	No
ADC Data 0	_ADC_DATA0_VECTOR	59	OFF059<17:1>	IFS1<27>	IEC1<27>	IPC14<28:26>	IPC14<25:24>	Yes
ADC Data 1	_ADC_DATA1_VECTOR	60	OFF060<17:1>	IFS1<28>	IEC1<28>	IPC15<4:2>	IPC15<1:0>	Yes
ADC Data 2	_ADC_DATA2_VECTOR	61	OFF061<17:1>	IFS1<29>	IEC1<29>	IPC15<12:10>	IPC15<9:8>	Yes
ADC Data 3	_ADC_DATA3_VECTOR	62	OFF062<17:1>	IFS1<30>	IEC1<30>	IPC15<20:18>	IPC15<17:16>	Yes
ADC Data 4	_ADC_DATA4_VECTOR	63	OFF063<17:1>	IFS1<31>	IEC1<31>	IPC15<28:26>	IPC15<25:24>	Yes
ADC Data 5	_ADC_DATA5_VECTOR	64	OFF064<17:1>	IFS2<0>	IEC2<0>	IPC16<4:2>	IPC16<1:0>	Yes
ADC Data 6	_ADC_DATA6_VECTOR	65	OFF065<17:1>	IFS2<1>	IEC2<1>	IPC16<12:10>	IPC16<9:8>	Yes
ADC Data 7	_ADC_DATA7_VECTOR	66	OFF066<17:1>	IFS2<2>	IEC2<2>	IPC16<20:18>	IPC16<17:16>	Yes
ADC Data 8	_ADC_DATA8_VECTOR	67	OFF067<17:1>	IFS2<3>	IEC2<3>	IPC16<28:26>	IPC16<25:24>	Yes
ADC Data 9	_ADC_DATA9_VECTOR	68	OFF068<17:1>	IFS2<4>	IEC2<4>	IPC17<4:2>	IPC17<1:0>	Yes
ADC Data 10	_ADC_DATA10_VECTOR	69	OFF069<17:1>	IFS2<5>	IEC2<5>	IPC17<12:10>	IPC17<9:8>	Yes
ADC Data 11	_ADC_DATA11_VECTOR	70	OFF070<17:1>	IFS2<6>	IEC2<6>	IPC17<20:18>	IPC17<17:16>	Yes
ADC Data 12	_ADC_DATA12_VECTOR	71	OFF071<17:1>	IFS2<7>	IEC2<7>	IPC17<28:26>	IPC17<25:24>	Yes
ADC Data 13	_ADC_DATA13_VECTOR	72	OFF072<17:1>	IFS2<8>	IEC2<8>	IPC18<4:2>	IPC18<1:0>	Yes
ADC Data 14	_ADC_DATA14_VECTOR	73	OFF073<17:1>	IFS2<9>	IEC2<9>	IPC18<12:10>	IPC18<9:8>	Yes
ADC Data 15	_ADC_DATA15_VECTOR	74	OFF074<17:1>	IFS2<10>	IEC2<10>	IPC18<20:18>	IPC18<17:16>	Yes
ADC Data 16	_ADC_DATA16_VECTOR	75	OFF075<17:1>	IFS2<11>	IEC2<11>	IPC18<28:26>	IPC18<25:24>	Yes
ADC Data 17	_ADC_DATA17_VECTOR	76	OFF076<17:1>	IFS2<12>	IEC2<12>	IPC19<4:2>	IPC19<1:0>	Yes
ADC Data 18	_ADC_DATA18_VECTOR	77	OFF077<17:1>	IFS2<13>	IEC2<13>	IPC19<12:10>	IPC19<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MZ EF Family Features”** for the list of available peripherals.

- 2:** This interrupt source is not available on 64-pin devices.
3: This interrupt source is not available on 100-pin devices.
4: This interrupt source is not available on 124-pin devices.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 11-24: USBxRPC: USB ENDPOINT 'x' REQUEST PACKET COUNT REGISTER (HOST MODE ONLY) ('x' = 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RQPKTCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RQPKTCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RQPKTCNT<15:0>:** Request Packet Count bits

Sets the number of packets of size MAXP that are to be transferred in a block transfer. This register is only available in *Host mode* when AUTOREQ is set.

REGISTER 11-25: USBDPBFD: USB DOUBLE PACKET BUFFER DISABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	EP7TXD	EP6TXD	EP5TXD	EP4TXD	EP3TXD	EP2TXD	EP1TXD	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	EP7RXD	EP6RXD	EP5RXD	EP4RXD	EP3RXD	EP2RXD	EP1RXD	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-17 **EP7TXD:EP1TXD:** TX Endpoint 'x' Double Packet Buffer Disable bits

1 = TX double packet buffering is disabled for endpoint 'x'

0 = TX double packet buffering is enabled for endpoint 'x'

bit 16 **Unimplemented:** Read as '0'

bit 15-1 **EP7RXD:EP1RXD:** RX Endpoint 'x' Double Packet Buffer Disable bits

1 = RX double packet buffering is disabled for endpoint 'x'

0 = RX double packet buffering is enabled for endpoint 'x'

bit 0 **Unimplemented:** Read as '0'

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 11-30: USBCRCON: USB CLOCK/RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R/W-1, HS
	—	—	—	—	—	USBIF	USBRF	USBWKUP
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	r-1	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	USB IDOVEN	USB IDVAL
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PHYIDEN	VBUS MONEN	ASVAL MONEN	BSVAL MONEN	SEND MONEN	USBIE	USBRIE	USB WKUPEN

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **USBIF:** USB General Interrupt Flag bit

1 = An event on the USB Bus has occurred

0 = No interrupt from USB module or interrupts have not been enabled

bit 25 **USBRF:** USB Resume Flag bit

1 = Resume from Suspend state. Device wake-up activity can be started.

0 = No Resume activity detected during Suspend, or not in Suspend state

bit 24 **USBWK:** USB Activity Status bit

1 = Connect, disconnect, or other activity on USB detected since last cleared

0 = No activity detected on USB

Note: This bit should be cleared just prior to entering sleep, but it should be checked that no activity has already occurred on USB before actually entering sleep.

bit 23-14 **Unimplemented:** Read as '0'

bit 15 **Reserved:** Read as '1'

bit 14-10 **Unimplemented:** Read as '0'

bit 9 **USBIDOVEN:** USB ID Override Enable bit

1 = Enable use of USBIDVAL bit

0 = Disable use of USBIDVAL and instead use the PHY value

bit 8 **USBIDVAL:** USB ID Value bit

1 = ID override value is 1

0 = ID override value is 0

bit 7 **PHYIDEN:** PHY ID Monitoring Enable bit

1 = Enable monitoring of the ID bit from the USB PHY

0 = Disable monitoring of the ID bit from the USB PHY

bit 6 **VBUSMONEN:** VBus Monitoring for OTG Enable bit

1 = Enable monitoring for VBus in VBUS Valid range (between 4.4V and 4.75V)

0 = Disable monitoring for VBus in VBUS Valid range

bit 5 **ASVALMONEN:** A-Device VBus Monitoring for OTG Enable bit

1 = Enable monitoring for VBus in Session Valid range for A-device (between 0.8V and 2.0V)

0 = Disable monitoring for VBus in Session Valid range for A-device

bit 4 **BSVALMONEN:** B-Device VBus Monitoring for OTG Enable bit

1 = Enable monitoring for VBus in Session Valid range for B-device (between 0.8V and 4.0V)

0 = Disable monitoring for VBus in Session Valid range for B-device

TABLE 12-11: PORTE REGISTER MAP FOR 100-PIN, 124-PIN, AND 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0400	ANSELE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSE9	ANSE8	ANSE7	ANSE6	ANSE5	ANSE4	—	—	—	—	03F0
0410	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISE9	TRISE8	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	03FF
0420	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
0430	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATE9	LATE8	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
0440	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCE9	ODCE8	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000
0450	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUE9	CNPUE8	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPUE3	CNPUE2	CNPUE1	CNPUE0	0000
0460	CNPDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDE9	CNPDE8	CNPDE7	CNPDE6	CNPDE5	CNPDE4	CNPDE3	CNPDE2	CNPDE1	CNPDE0	0000
0470	CNCONE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0480	CNENE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNENE9	CNENE8	CNENE7	CNENE6	CNENE5	CNENE4	CNENE3	CNENE2	CNENE1	CNENE0	0000
0490	CNSTATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CN STATE9	CN STATE8	CN STATE7	CN STATE6	CN STATE5	CN STATE4	CN STATE3	CN STATE2	CN STATE1	CN STATE0	0000
04A0	CNNEE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNNEE9	CNNEE8	CNNEE7	CNNEE6	CNNEE5	CNNEE4	CNNEE3	CNNEE2	CNNEE1	CNNEE0	0000
04B0	CNFE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNFE9	CNFE8	CNFE7	CNFE6	CNFE5	CNFE4	CNFE3	CNFE2	CNFE1	CNFE0	0000
04C0	SRCONOE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR0E3	SR0E2	SR0E1	SR0E0	0000
04D0	SRCON1E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR1E3	SR1E2	SR1E1	SR1E0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 19-1: SPIxCON: SPI CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 FRMEN	R/W-0 FRMSYNC	R/W-0 FRMPOL	R/W-0 MSEN	R/W-0 FRMSYPW	FRMCNT<2:0>		
23:16	R/W-0 MCLKSEL ⁽¹⁾	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0 SPIFE	R/W-0 ENHBUF ⁽¹⁾
15:8	R/W-0 ON	U-0 —	R/W-0 SIDL	R/W-0 DISSDO ⁽⁴⁾	R/W-0 MODE32	R/W-0 MODE16	R/W-0 SMP	R/W-0 CKE ⁽²⁾
7:0	R/W-0 SSEN	R/W-0 CKP ⁽³⁾	R/W-0 MSTEN	R/W-0 DISSDI ⁽⁴⁾	R/W-0 STXISEL<1:0>	SRXISEL<1:0>		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31 **FRMEN:** Framed SPI Support bit
1 = Framed SPI support is enabled ($\overline{SSx}$ pin used as FSYNC input/output)
0 = Framed SPI support is disabled
- bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on $\overline{SSx}$ pin bit (Framed SPI mode only)
1 = Frame sync pulse input (Slave mode)
0 = Frame sync pulse output (Master mode)
- bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)
1 = Frame pulse is active-high
0 = Frame pulse is active-low
- bit 28 **MSEN:** Master Mode Slave Select Enable bit
1 = Slave select SPI support is enabled. The $\overline{SS}$ pin is automatically driven during transmission in Master mode. Polarity is determined by the FRMPOL bit.
0 = Slave select SPI support is disabled.
- bit 27 **FRMSYPW:** Frame Sync Pulse Width bit
1 = Frame sync pulse is one character wide
0 = Frame sync pulse is one clock wide
- bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits. Controls the number of data characters transmitted per pulse. This bit is only valid in Framed mode.
111 = Reserved
110 = Reserved
101 = Generate a frame sync pulse on every 32 data characters
100 = Generate a frame sync pulse on every 16 data characters
011 = Generate a frame sync pulse on every 8 data characters
010 = Generate a frame sync pulse on every 4 data characters
001 = Generate a frame sync pulse on every 2 data characters
000 = Generate a frame sync pulse on every data character
- bit 23 **MCLKSEL:** Master Clock Enable bit⁽¹⁾
1 = REFCLKO1 is used by the Baud Rate Generator
0 = PBCLK2 is used by the Baud Rate Generator
- bit 22-18 **Unimplemented:** Read as '0'

- Note 1:** This bit can only be written when the ON bit = 0. Refer to **Section 37.0 “Electrical Characteristics”** for maximum clock frequency requirements.
- 2:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
- 3:** When AUDEN = 1, the SPI/I²S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.
- 4:** This bit present for legacy compatibility and is superseded by PPS functionality on these devices (see **Section 12.4 “Peripheral Pin Select (PPS)”** for more information).

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 22-1: UxMODE: UARTx MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 ON	U-0 —	R/W-0 SIDL	R/W-0 IREN	R/W-0 RTSMD	U-0 —	R/W-0 UEN<1:0> ⁽¹⁾	R/W-0
7:0	R/W-0 WAKE	R/W-0 LPBACK	R/W-0 ABAUD	R/W-0 RXINV	R/W-0 BRGH	R/W-0 PDSEL<1:0>	R/W-0	R/W-0 STSEL

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** UARTx Enable bit

1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by UEN<1:0> and UTXEN control bits

0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue operation when device enters Idle mode

0 = Continue operation in Idle mode

bit 12 **IREN:** IrDA Encoder and Decoder Enable bit

1 = IrDA is enabled

0 = IrDA is disabled

bit 11 **RTSMD:** Mode Selection for UxRTS Pin bit

1 = UxRTS pin is in Simplex mode

0 = UxRTS pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits⁽¹⁾

11 = UxTX, UxRX and UxBCLK pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register

10 = UxTX, UxRX, UxCTS and UxRTS pins are enabled and used

01 = UxTX, UxRX and UxRTS pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register

00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit

1 = Wake-up is enabled

0 = Wake-up is disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit

1 = Loopback mode is enabled

0 = Loopback mode is disabled

Note 1: These bits are present for legacy compatibility, and are superseded by PPS functionality on these devices. For additional information, see **Section 12.4 "Peripheral Pin Select (PPS)"**.

REGISTER 22-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

- bit 5 **ABAUD**: Auto-Baud Enable bit
 1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55);
 cleared by hardware upon completion
 0 = Baud rate measurement is disabled or completed
- bit 4 **RXINV**: Receive Polarity Inversion bit
 1 = UxRX Idle state is '0'
 0 = UxRX Idle state is '1'
- bit 3 **BRGH**: High Baud Rate Enable bit
 1 = High-Speed mode – 4x baud clock enabled
 0 = Standard Speed mode – 16x baud clock enabled
- bit 2-1 **PDSEL<1:0>**: Parity and Data Selection bits
 11 = 9-bit data, no parity
 10 = 8-bit data, odd parity
 01 = 8-bit data, even parity
 00 = 8-bit data, no parity
- bit 0 **STSEL**: Stop Selection bit
 1 = 2 Stop bits
 0 = 1 Stop bit

Note 1: These bits are present for legacy compatibility, and are superseded by PPS functionality on these devices. For additional information, see **Section 12.4 “Peripheral Pin Select (PPS)”**.

REGISTER 26-5: CESTAT: CRYPTO ENGINE STATUS REGISTER (CONTINUED)

bit 16 **ACTIVE:** Buffer Descriptor Processor Status bit

1 = BDP is active

0 = BDP is idle

bit 15-0 **BDCTRL<15:0>:** Descriptor Control Word Status bits

These bits contain the Control Word for the current Buffer Descriptor.

NOTES:

30.0 ETHERNET CONTROLLER

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 35. “Ethernet Controller”** (DS60001155) in the “*PIC32 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com/PIC32).

The Ethernet controller is a bus master module that interfaces with an off-chip Physical Layer (PHY) to implement a complete Ethernet node in a system.

Key features of the Ethernet Controller include:

- Supports 10/100 Mbps data transfer rates
- Supports full-duplex and half-duplex operation

- Supports RMI and MII PHY interface
- Supports MIIM PHY management interface
- Supports both manual and automatic Flow Control
- RAM descriptor-based DMA operation for both receive and transmit path
- Fully configurable interrupts
- Configurable receive packet filtering
 - CRC check
 - 64-byte pattern match
 - Broadcast, multicast and unicast packets
 - Magic Packet™
 - 64-bit hash table
 - Runt packet
- Supports packet payload checksum calculation
- Supports various hardware statistics counters

Figure 30-1 illustrates a block diagram of the Ethernet controller.

FIGURE 30-1: ETHERNET CONTROLLER BLOCK DIAGRAM

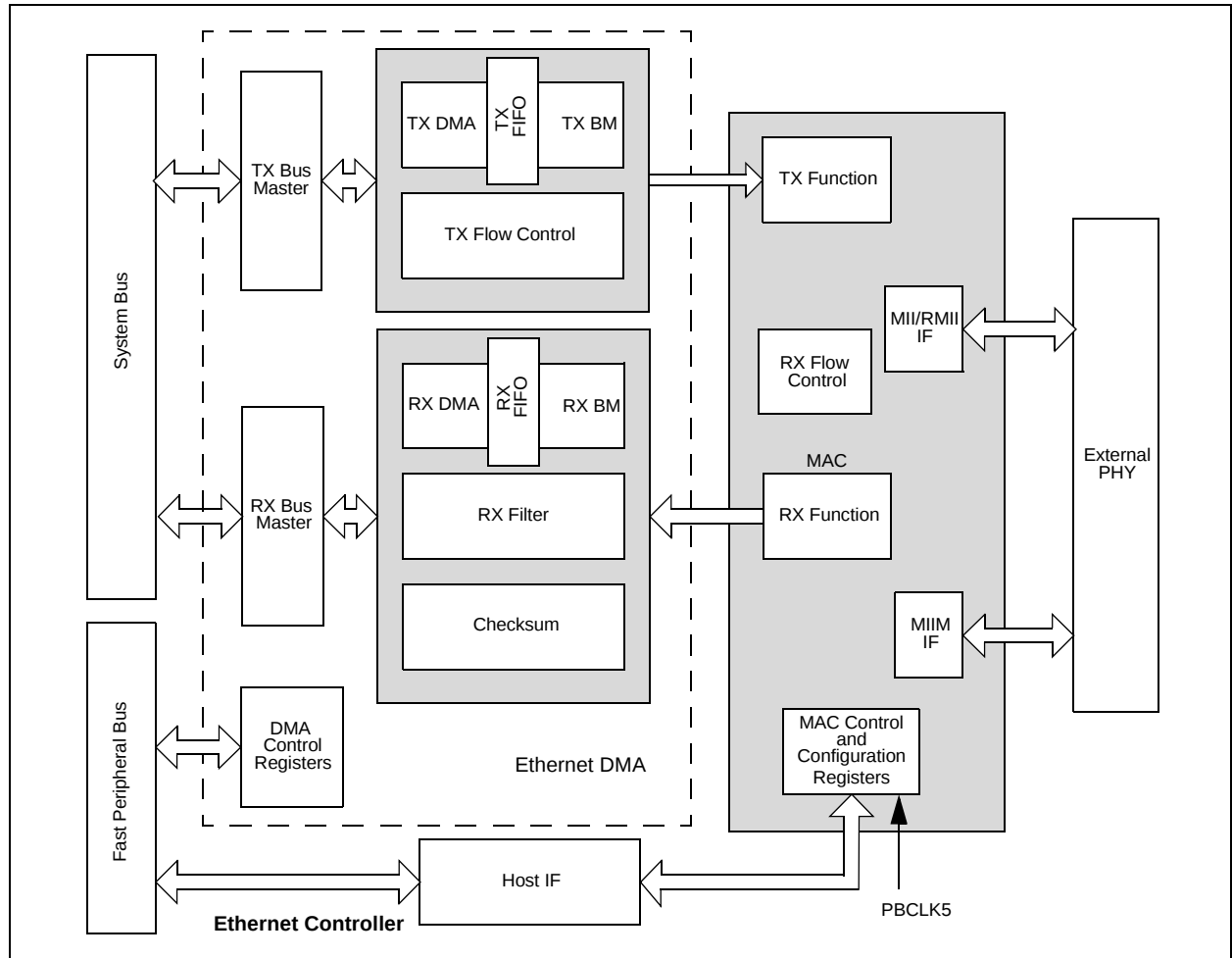


TABLE 30-5: ETHERNET CONTROLLER REGISTER SUMMARY (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
22B0	EMAC1 MWTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MWTD<15:0>																0000
22C0	EMAC1 MRDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MRDD<15:0>																0000
22D0	EMAC1 MIND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	LINKFAIL	NOTVALID	SCAN	MIIMBUSY	0000
2300	EMAC1 SA0 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	STNADDR6<7:0>								STNADDR5<7:0>								XXXX
2310	EMAC1 SA1 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	STNADDR4<7:0>								STNADDR3<7:0>								XXXX
2320	EMAC1 SA2 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	STNADDR2<7:0>								STNADDR1<7:0>								XXXX

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

2: Reset values default to the factory programmed value.

REGISTER 30-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUFCNT<7:0> ⁽¹⁾							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ETHBUSY ⁽⁵⁾	TxBUSY ^(2,6)	RxBUSY ^(3,6)	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **BUFCNT<7:0>:** Packet Buffer Count bits⁽¹⁾

Number of packet buffers received in memory. Once a packet has been successfully received, this register is incremented by hardware based on the number of descriptors used by the packet. Software decrements the counter (by writing to the BUFCDEC bit (ETHCON1<0>)) for each descriptor used) after a packet has been read out of the buffer. The register does not roll over (0xFF to 0x00) when hardware tries to increment the register and the register is already at 0xFF. Conversely, the register does not roll under (0x00 to 0xFF) when software tries to decrement the register and the register is already at 0x0000. When software attempts to decrement the counter at the same time that the hardware attempts to increment the counter, the counter value will remain unchanged.

When this register value reaches 0xFF, the RX logic will halt (only if automatic Flow Control is enabled) awaiting software to write the BUFCDEC bit in order to decrement the register below 0xFF.

If automatic Flow Control is disabled, the RxDMA will continue processing and the BUFCNT will saturate at a value of 0xFF.

When this register is non-zero, the PKTPEND status bit will be set and an interrupt may be generated, depending on the value of the ETHIEN bit <PKTPENDIE> register.

When the ETHRXST register is written, the BUFCNT counter is automatically cleared to 0x00.

Note: BUFCNT will not be cleared when ON is set to '0'. This enables software to continue to utilize and decrement this count.

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **ETHBUSY:** Ethernet Module busy bit⁽⁵⁾

1 = Ethernet logic has been turned on (ON (ETHCON1<15>) = 1) or is completing a transaction

0 = Ethernet logic is idle

This bit indicates that the module has been turned on or is completing a transaction after being turned off.

Note 1: This bit is only used for RX operations.

2: This bit is only affected by TX operations.

3: This bit is only affected by RX operations.

4: This bit is affected by TX and RX operations.

5: This bit will be *set* when the ON bit (ETHCON1<15>) = 1.

6: This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

TABLE 34-3: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets ⁽¹⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	CFGCON	31:16	—	—	—	—	—	—	DMAPRI	CPUPRI	—	—	—	—	—	—	ICACLK	OCACLK	0000
		15:0	—	—	IOLOCK	PMDLOCK	PGLOCK	—	—	USBSSSEN	IOANCPEN	—	ECCCON<1:0>		JTAGEN	TROEN	—	TDOEN	000B
0020	DEVID	31:16	VER<3:0>					DEVID<27:16>											XXXX
		15:0	DEVID<15:0>																XXXX
0030	SYSKEY	31:16	SYSKEY<31:0>																0000
		15:0	SYSKEY<31:0>																0000
00C0	CFGEBIA ⁽²⁾	31:16	EBIPINEN	—	—	—	—	—	—	—	EBIA23EN	EBIA22EN	EBIA21EN	EBIA20EN	EBIA19EN	EBIA18EN	EBIA17EN	EBIA16EN	0000
		15:0	EBIA15EN	EBIA14EN	EBIA13EN	EBIA12EN	EBIA11EN	EBIA10EN	EBIA9EN	EBIA8EN	EBIA7EN	EBIA6EN	EBIA5EN	EBIA4EN	EBIA3EN	EBIA2EN	EBIA1EN	EBIA0EN	0000
00D0	CFGEBIC ⁽²⁾	31:16	EBI RDYINV3	EBI RDYINV2	EBI RDYINV1	—	EBI RDYEN3	EBI RDYEN2	EBI RDYEN1	—	—	—	—	—	—	—	EBI RDYLV1	EBIRPEN	0000
		15:0	—	—	EBIWEEN	EBIOEEN	—	—	EBIBSEN1	EBIBSEN0	EBICSEN3	EBICSEN2	EBICSEN1	EBICSEN0	—	—	EBIDEN1	EBIDEN0	0000
00E0	CFGPG	31:16	ICD1PG<1:0>		—	—	—	—	CRYPTPG<1:0>		FCPG<1:0>		SQ1PG<1:0>		—	—	ETHPG<1:0>		0000
		15:0	CAN2PG<1:0>		CAN1PG<1:0>		—	—	USBPG<1:0>		—	—	DMAPG<1:0>		—	—	CPUPG<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

Note 2: This register is not available on 64-pin devices.

TABLE 34-4: DEVICE SERIAL NUMBER SUMMARY

Virtual Address (BFC5_#)	Register Name	Bit Range	Bits																All Resets ⁽¹⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4020	DEVSN0	31:16	Device Serial Number <31:16>																XXXX
		15:0	Device Serial Number <15:0>																XXXX
4024	DEVSN1	31:16	Device Serial Number <31:16>																XXXX
		15:0	Device Serial Number <15:0>																XXXX

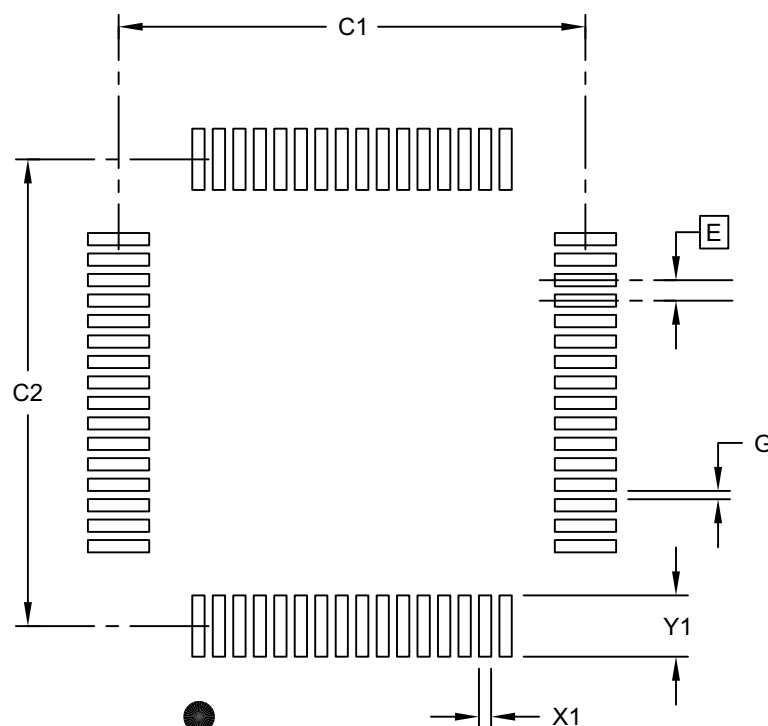
Legend: x = unknown value on Reset.

Note 1: Reset values are dependent on the device variant.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2085B Sheet 1 of 1

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

ADCCMPx (ADC Digital Comparator 'x' Limit Value Register ('x' = 1 through 6)).....	461
ADCCMPxCON (ADC Digital Comparator 'x' Control Register ('x' = 1 through 6)).....	469
ADCCON1 (ADC Control Register 1).....	437
ADCCON2 (ADC Control Register 2).....	440
ADCCON3 (ADC Control Register 3).....	442
ADCCSS1 (ADC Common Scan Select Register 1).....	457
ADCCSS2 (ADC Common Scan Select Register 2).....	458
ADCDATAx (ADC Output Data Register ('x' = 0 through 44)).....	474
ADCDSTAT1 (ADC Data Ready Status Register 1).....	459
ADCDSTAT2 (ADC Data Ready Status Register 2).....	459
ADCEIEN1 (ADC Early Interrupt Enable Register 1).....	477
ADCEIEN2 (ADC Early Interrupt Enable Register 2).....	477
ADCEIEN2 (ADC Early Interrupt Status Register 2).....	479
ADCFLTRx (ADC Digital Filter 'x' Register ('x' = 1 through 6)).....	462
ADCGIRQEN1 (ADC Interrupt Enable Register 1).....	456
ADCIMCON1 (ADC Input Mode Control Register 1).....	447
ADCIMCON2 (ADC Input Mode Control Register 2).....	450
ADCIMCON3 (ADC Input Mode Control Register 3).....	453
ADCIRQEN2 (ADC Interrupt Enable Register 2).....	456
ADCSYSCFG1 (ADC System Configuration Register 1).....	483
ADCSYSCFG2 (ADC System Configuration Register 2).....	483
ADCTRG1 (ADC Trigger Source 1 Register).....	464
ADCTRG2 (ADC Trigger Source 2 Register).....	465
ADCTRG3 (ADC Trigger Source 3 Register).....	466
ADCTRGMODE (ADC Triggering Mode for Dedicated ADC).....	445
ADCTRGSNS (ADC Trigger Level/Edge Sensitivity).....	475
ADCxCFG (ADCx Configuration Register 'x' ('x' = 1 through 6)).....	482
ADCxTIME (Dedicated ADCx Timing Register 'x' ('x' = 0 through 4)).....	476
ALRMTIME (Alarm Time Value).....	399
BFXSEQ3/ABFXSEQ3 (Boot Flash 'x' Sequence Word 3 Register).....	70
CEBDADDR (Crypto Engine Buffer Descriptor).....	405
CEBDPADDR (Crypto Engine Buffer Descriptor Processor).....	405
CECON (Crypto Engine Control).....	404
CEHDLEN (Crypto Engine Header Length).....	411
CEINTEN (Crypto Engine Interrupt Enable).....	409
CEINTSRC (Crypto Engine Interrupt Source).....	408
CEPOLLCON (Crypto Engine Poll Control).....	410
CESTAT (Crypto Engine Status).....	406
CETRLLEN (Crypto Engine Trailer Length).....	411
CEVER (Crypto Engine Revision, Version, and ID).....	403
CFGEBIA (External Bus Interface Address Pin Configuration).....	597
CFGEBIC (External Bus Interface Control Pin Configuration).....	598
CFGPG (Permission Group Configuration).....	600
CiCFG (CAN Baud Rate Configuration).....	492
CiCON (CAN Module Control).....	490
CiFIFOBA (CAN Message Buffer Base Address).....	517
CiFIFOCIn (CAN Module Message Index Register 'n' ('n' = 0-31)).....	522
CiFIFOCONn (CAN FIFO Control Register 'n' ('n' = 0-31)).....	518
CiFIFOINTn (CAN FIFO Interrupt Register 'n' ('n' = 0-31)).....	520
CiFIFOUn (CAN FIFO User Address Register 'n' ('n' = 0-31)).....	522
CiFLTCON0 (CAN Filter Control Register 0).....	500
CiFLTCON1 (CAN Filter Control Register 1).....	502
CiFLTCON2 (CAN Filter Control Register 2).....	504
CiFLTCON3 (CAN Filter Control Register 3).....	506
CiFLTCON4 (CAN Filter Control Register 4).....	508
CiFLTCON5 (CAN Filter Control Register 5).....	510
CiFLTCON6 (CAN Filter Control Register 6).....	512
CiFLTCON7 (CAN Filter Control Register 7).....	514
CiFSTAT (CAN FIFO Status).....	497
CiRXFn (CAN Acceptance Filter 'n' Register 7 ('n' = 0-31)).....	516
CiRXMn (CAN Acceptance Filter Mask 'n' Register ('n' = 0-3)).....	499
CiRXOVF (CAN Receive FIFO Overflow Status).....	498
CiTMR (CAN Timer).....	498
CiTREC (CAN Transmit/Receive Error Count).....	497
CiVEC (CAN Interrupt Code).....	496
CMSTAT (Comparator Control Register).....	570
CMxCON (Comparator Control).....	569
CNCONx (Change Notice Control for PORTx).....	282
CONFIG (Configuration Register - CP0 Register 16, Select 0).....	51
CONFIG1 (Configuration Register 1 - CP0 Register 16, Select 1).....	52
CONFIG3 (Configuration Register 3 - CP0 Register 16, Select 3).....	53
CONFIG5 (Configuration Register 5 - CP0 Register 16, Select 5).....	54
CONFIG7 (Configuration Register 7 - CP0 Register 16, Select 7).....	54
CVRCON (Comparator Voltage Reference Control).....	573
DCHxCON (DMA Channel x Control).....	186
DCHxCPTR (DMA Channel x Cell Pointer).....	194
DCHxCsIZ (DMA Channel x Cell-Size).....	194
DCHxDAT (DMA Channel x Pattern Data).....	195
DCHxDPTR (Channel x Destination Pointer).....	193
DCHxDSA (DMA Channel x Destination Start Address).....	191
DCHxDsIZ (DMA Channel x Destination Size).....	192
DCHxECON (DMA Channel x Event Control).....	188
DCHxINT (DMA Channel x Interrupt Control).....	189
DCHxSPTR (DMA Channel x Source Pointer).....	193
DCHxSSA (DMA Channel x Source Start Address).....	191
DCHxSSIZ (DMA Channel x Source Size).....	192
DCRCCON (DMA CRC Control).....	183
DCRCDATA (DMA CRC Data).....	185
DCRCXOR (DMA CRCXOR Enable).....	185
DEVCFG0/ADEVCFG0 (Device Configuration Word 0).....	587
DEVCFG1/ADEVCFG1 (Device Configuration Word 1).....	589
DEVCFG2/ADEVCFG2 (Device Configuration Word 2).....	592
DEVCFG3/ADEVCFG3 (Device Configuration Word 3).....	594
DEVCP0/ADEVCP0 (Device Code-Protect 0).....	586
DEVID (Device and Revision ID).....	601
DEVSIGN0/ADEVSIGN0 (Device Signature Word 0).....	586
DMAADDR (DMA Address).....	182
DMACON (DMA Controller Control).....	181
DMASTAT (DMA Status).....	182