



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efk100-e-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efk100-e-pt</a>

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**TABLE 1-1: ADC PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/LQFP			
AN0	16	25	A18	36	I	Analog	Analog Input Channels
AN1	15	24	A17	35	I	Analog	
AN2	14	23	A16	34	I	Analog	
AN3	13	22	A14	31	I	Analog	
AN4	12	21	A13	26	I	Analog	
AN5	23	34	B19	49	I	Analog	
AN6	24	35	A24	50	I	Analog	
AN7	27	41	A27	59	I	Analog	
AN8	28	42	B23	60	I	Analog	
AN9	29	43	A28	61	I	Analog	
AN10	30	44	B24	62	I	Analog	
AN11	10	16	B9	21	I	Analog	
AN12	6	12	B7	16	I	Analog	
AN13	5	11	A8	15	I	Analog	
AN14	4	10	B6	14	I	Analog	
AN15	3	5	A4	5	I	Analog	
AN16	2	4	B2	4	I	Analog	
AN17	1	3	A3	3	I	Analog	
AN18	64	100	A67	144	I	Analog	
AN19	—	9	A7	13	I	Analog	
AN20	—	8	B5	12	I	Analog	
AN21	—	7	A6	11	I	Analog	
AN22	—	6	B3	6	I	Analog	
AN23	—	1	A2	1	I	Analog	
AN24	—	17	A11	22	I	Analog	
AN25	—	18	B10	23	I	Analog	
AN26	—	19	A12	24	I	Analog	
AN27	—	28	B15	39	I	Analog	
AN28	—	29	A20	40	I	Analog	
AN29	—	38	B21	56	I	Analog	
AN30	—	39	A26	57	I	Analog	
AN31	—	40	B22	58	I	Analog	
AN32	—	47	B27	69	I	Analog	
AN33	—	48	A32	70	I	Analog	
AN34	—	2	B1	2	I	Analog	
AN35	—	—	A5	7	I	Analog	

**Legend:** CMOS = CMOS-compatible input or output  
ST = Schmitt Trigger input with CMOS levels  
TTL = Transistor-transistor Logic input buffer

Analog = Analog input  
O = Output  
PPS = Peripheral Pin Select

P = Power  
I = Input

## 3.1.4 FLOATING POINT UNIT (FPU)

The Floating Point Unit (FPU), Coprocessor (CP1), implements the MIPS Instruction Set Architecture for floating point computation. The implementation supports the ANSI/IEEE Standard 754 (IEEE for Binary Floating Point Arithmetic) for 32-bit and 64-bit floating point data formats. The FPU can be programmed to have thirty-two 32-bit or 64-bit floating point registers used for floating point operations.

The performance is optimized for 32-bit formats. Most instructions have one FPU cycle throughput and four FPU cycle latency. The FPU implements the multiply-add (MADD) and multiply-sub (MSUB) instructions with intermediate rounding after the multiply function. The result is guaranteed to be the same as executing a MUL and an ADD instruction separately, but the instruction latency, instruction fetch, dispatch bandwidth, and the total number of register accesses are improved.

IEEE denormalized input operands and results are supported by hardware for some instructions. IEEE denormalized results are not supported by hardware in general, but a fast flush-to-zero mode is provided to optimize performance. The fast flush-to-zero mode is enabled through the FCCR register, and use of this mode is recommended for best performance when denormalized results are generated.

The FPU has a separate pipeline for floating point instruction execution. This pipeline operates in parallel with the integer core pipeline and does not stall when the integer pipeline stalls. This allows long-running FPU operations, such as divide or square root, to be partially masked by system stalls and/or other integer unit instructions. Arithmetic instructions are always dispatched and completed in order, but loads and stores can complete out of order. The exception model is “precise” at all times.

Table 3-4 contains the floating point instruction latencies and repeat rates for the processor core. In this table, 'Latency' refers to the number of FPU cycles necessary for the first instruction to produce the result needed by the second instruction. The “Repeat Rate” refers to the maximum rate at which an instruction can be executed per FPU cycle.

**TABLE 3-4: FPU INSTRUCTION LATENCIES AND REPEAT RATES**

Op code	Latency (FPU Cycles)	Repeat Rate (FPU Cycles)
ABS.[S,D], NEG.[S,D], ADD.[S,D], SUB.[S,D], C.cond.[S,D], MUL.S	4	1
MADD.S, MSUB.S, NMADD.S, NMSUB.S, CABS.cond.[S,D]	4	1
CVT.D.S, CVT.PS.PW, CVT.[S,D].[W,L]	4	1
CVT.S.D, CVT.[W,L].[S,D], CEIL.[W,L].[S,D], FLOOR.[W,L].[S,D], ROUND.[W,L].[S,D], TRUNC.[W,L].[S,D]	4	1
MOV.[S,D], MOVF.[S,D], MOVN.[S,D], MOVT.[S,D], MOVZ.[S,D]	4	1
MUL.D	5	2
MADD.D, MSUB.D, NMADD.D, NMSUB.D	5	2
RECIP.S	13	10
RECIP.D	26	21
RSQRT.S	17	14
RSQRT.D	36	31
DIV.S, SQRT.S	17	14
DIV.D, SQRT.D	32	29
MTC1, DMTC1, LWC1, LDC1, LDXC1, LUXC1, LWXC1	4	1
MFC1, DMFC1, SWC1, SDC1, SDXC1, SUXC1, SWXC1	1	1

**Legend:** S = Single (32-bit) D = Double (64-bit)  
W = Word (32-bit) L = Long word (64-bit)

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 3-2: CONFIG1: CONFIGURATION REGISTER 1; CP0 REGISTER 16, SELECT 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1 —	R-0	R-0	R-1	R-1	R-1	R-1	R-0
	MMU Size<5:0>							IS<2>
23:16	R-1	R-0	R-0	R-1	R-1	R-0	R-1	R-1
	IS<1:0>		IL<2:0>			IA<2:0>		
15:8	R-0	R-0	R-0	R-0	R-1	R-1	R-0	R-1
	DS<2:0>			DL<2:0>			DA<2:1>	
7:0	R-1 DA<0>	U-0 —	U-0 —	R-1 PC	R-1 WR	R-0 CA	R-1 EP	R-1 FP

<b>Legend:</b>	r = Reserved bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to a '1' to indicate the presence of the Config2 register.

bit 30-25 **MMU Size<5:0>:** Contains the number of TLB entries minus 1

001111 = 16 TLB entries

bit 24-22 **IS<2:0>:** Instruction Cache Sets bits

010 = Contains 256 instruction cache sets per way

bit 21-19 **IL<2:0>:** Instruction-Cache Line bits

011 = Contains instruction cache line size of 16 bytes

bit 18-16 **IA<2:0>:** Instruction-Cache Associativity bits

011 = Contains 4-way instruction cache associativity

bit 15-13 **DS<2:0>:** Data-Cache Sets bits

000 = Contains 64 data cache sets per way

bit 12-10 **DL<2:0>:** Data-Cache Line bits

011 = Contains data cache line size of 16 bytes

bit 9-7 **DA<2:0>:** Data-Cache Associativity bits

011 = Contains the 4-way set associativity for the data cache

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **PC:** Performance Counter bit

1 = The processor core contains Performance Counters

bit 3 **WR:** Watch Register Presence bit

1 = No Watch registers are present

bit 2 **CA:** Code Compression Implemented bit

0 = No MIPS16e® present

bit 1 **EP:** EJTAG Present bit

1 = Core implements EJTAG

bit 0 **FP:** Floating Point Unit bit

1 = Floating Point Unit is present

**TABLE 4-4: INITIATORS TO TARGETS ACCESS ASSOCIATION**

Target #	Initiator ID	1	2	3	4	5	6	7	8	9	10	11	12	13	14
	Name	CPU		DMA Read		DMA Write		USB	Ethernet Read	Ethernet Write	CAN1	CAN2	SQI1	Flash Controller	Crypto
1	<b>Flash Memory:</b> Program Flash Boot Flash Prefetch Module	X		X				X	X		X	X			X
2	RAM Bank 1 Memory	X		X		X		X	X	X	X	X	X	X	X
3	RAM Bank 2 Memory	X		X		X		X	X	X	X	X	X	X	X
4	External Memory via EBI and EBI Module	X		X		X		X	X	X	X	X	X		X
5	<b>Peripheral Set 1:</b> System Control, Flash Control, DMT, RTCC, CVR, PPS Input, PPS Output, Interrupts, DMA, WDT	X													
6	<b>Peripheral Set 2:</b> SPI1-SPI6 I2C1-I2C5 UART1-UART6 PMP	X		X		X									
7	<b>Peripheral Set 3:</b> Timer1-Timer9 IC1-IC9 OC1-OC9 ADC Comparator 1 Comparator 2	X		X		X									
8	<b>Peripheral Set 4:</b> PORTA-PORTK	X		X		X									
9	<b>Peripheral Set 5:</b> CAN1 CAN2 Ethernet Controller	X													
10	<b>Peripheral Set 6:</b> USB	X													
11	External Memory via SQI1 and SQI1 Module	X													
12	<b>Peripheral Set 7:</b> Crypto Engine	X													
13	<b>Peripheral Set 8:</b> RNG Module	X													

**TABLE 4-14: SYSTEM BUS TARGET 6 REGISTER MAP**

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
9820	SBT6ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>				0000
9824	SBT6ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>			0000
9828	SBT6ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9830	SBT6ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9838	SBT6ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9840	SBT6REG0	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>					PRI	—	SIZE<4:0>					—	—	—	xxxx	
9850	SBT6RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9858	SBT6WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9860	SBT6REG1	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>					PRI	—	SIZE<4:0>					—	—	—	xxxx	
9870	SBT6RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9878	SBT6WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note:** For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

## REGISTER 4-3: SBTxELOG1: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 1 ( 'x' = 0-13) (CONTINUED)

- bit 7-4    **REGION<3:0>**: Requested Region Number bits  
          1111 - 0000 = Target's region that reported a permission group violation
- bit 3     **Unimplemented**: Read as '0'
- bit 2-0   **CMD<2:0>**: Transaction Command of the Requester bits  
          111 = Reserved  
          110 = Reserved  
          101 = Write (a non-posted write)  
          100 = Reserved  
          011 = Read (a locked read caused by a Read-Modify-Write transaction)  
          010 = Read  
          001 = Write  
          000 = Idle

<b>Note:</b> Refer to Table 4-6 for the list of available targets and their descriptions.
---

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 5-7: NVMPWP: PROGRAM FLASH WRITE-PROTECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	PWPULOCK	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PWP<23:16>							
15:8	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
	PWP<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PWP<7:0>							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **PWPULOCK:** Program Flash Memory Page Write-protect Unlock bit

1 = Register is not locked and can be modified

0 = Register is locked and cannot be modified

This bit is only clearable and cannot be set except by any reset.

bit 30-24 **Unimplemented:** Read as '0'

bit 23-0 **PWP<23:0>:** Flash Program Write-protect (Page) Address bits

Physical memory below address 0x1Dxxxxxx is write protected, where 'xxxxxx' is specified by PWP<23:0>.

When PWP<23:0> has a value of '0', write protection is disabled for the entire program Flash. If the specified address falls within the page, the entire page and all pages below the current page will be protected.

**Note:** The bits in this register are only writable when the NVMKEY unlock sequence is followed.



**TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)**

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3170	USB E7CSR0	31:16 15:0	Indexed by the same bits in USBIE7CSR0																0000 0000
3174	USB E7CSR1	31:16 15:0	Indexed by the same bits in USBIE7CSR1																0000 0000
3178	USB E7CSR2	31:16 15:0	Indexed by the same bits in USBIE7CSR2																0000 0000
317C	USB E7CSR3	31:16 15:0	Indexed by the same bits in USBIE7CSR3																0000 0000
3200	USB DMAINT	31:16 15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
3204	USB DMA1C	31:16 15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
3208	USB DMA1A	31:16 15:0	DMAADDR<31:16> DMAADDR<15:0>																0000 0000
320C	USB DMA1N	31:16 15:0	DMACOUNT<31:16> DMACOUNT<15:0>																0000 0000
3214	USB DMA2C	31:16 15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
3218	USB DMA2A	31:16 15:0	DMAADDR<31:16> DMAADDR<15:0>																0000 0000
321C	USB DMA2N	31:16 15:0	DMACOUNT<31:16> DMACOUNT<15:0>																0000 0000
3224	USB DMA3C	31:16 15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
3228	USB DMA3A	31:16 15:0	DMAADDR<31:16> DMAADDR<15:0>																0000 0000
322C	USB DMA3N	31:16 15:0	DMACOUNT<31:16> DMACOUNT<15:0>																0000 0000
3234	USB DMA4C	31:16 15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
3238	USB DMA4A	31:16 15:0	DMAADDR<31:16> DMAADDR<15:0>																0000 0000
323C	USB DMA4N	31:16 15:0	DMACOUNT<31:16> DMACOUNT<15:0>																0000 0000
3244	USB DMA5C	31:16 15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: Device mode.
  - 2: Host mode.
  - 3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
  - 4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 11-1: USBCSR0: USB CONTROL STATUS REGISTER 0**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	R-0, HS EP7TXIF	R-0, HS EP6TXIF	R-0, HS EP5TXIF	R-0, HS EP4TXIF	R-0, HS EP3TXIF	R-0, HS EP2TXIF	R-0, HS EP1TXIF	R-0, HS EP0IF
15:8	R/W-0 ISOUPD —	R/W-0 SOFTCONN —	R/W-1 HSEN	R-0, HS HSMODE	R-0 RESET	R/W-0 RESUME	R-0, HC SUSPMODE	R/W-0 SUSPEN
7:0	U-0 —	R/W-0 —	R/W-0 —	R/W-0 —	R/W-0 —	R/W-0 —	R/W-0 —	R/W-0 —
FUNC<6:0>								

<b>Legend:</b>	HS = Hardware Set	HC = Hardware Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-17 **EP7TXIF:EP1TXIF:** Endpoint 'n' TX Interrupt Flag bit

- 1 = Endpoint has a transmit interrupt to be serviced
- 0 = No interrupt event

bit 16 **EP0IF:** Endpoint 0 Interrupt bit

- 1 = Endpoint 0 has an interrupt to be serviced
- 0 = No interrupt event

All EPxTX and EP0 bits are cleared when the byte is read. Therefore, these bits must be read independently from the remaining bits in this register to avoid accidental clearing.

bit 15 **ISOUPD:** ISO Update bit (*Device mode only; unimplemented in Host mode*)

- 1 = USB module will wait for a SOF token from the time TXPKTRDY is set before sending the packet
- 0 = No change in behavior

This bit only affects endpoints performing isochronous transfers when in *Device mode*. This bit is unimplemented in *Host mode*.

bit 14 **SOFTCONN:** Soft Connect/Disconnect Feature Selection bit

- 1 = The USB D+/D- lines are enabled and active
- 0 = The USB D+/D- lines are disabled and are tri-stated

This bit is only available in *Device mode*.

bit 13 **HSEN:** Hi-Speed Enable bit

- 1 = The USB module will negotiate for Hi-Speed mode when the device is reset by the hub
- 0 = Module only operates in Full-Speed mode

bit 12 **HSMODE:** Hi-Speed Mode Status bit

- 1 = Hi-Speed mode successfully negotiated during USB reset
- 0 = Module is not in Hi-Speed mode

In *Device mode*, this bit becomes valid when a USB reset completes. In *Host mode*, it becomes valid when the RESET bit is cleared.

bit 11 **RESET:** Module Reset Status bit

- 1 = Reset signaling is present on the bus
- 0 = Normal module operation

In *Device mode*, this bit is read-only. In *Host mode*, this bit is read/write.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 11-11: USBIENCSR3: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 3 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RXFIFOSZ<3:0>				TXFIFOSZ<3:0>			
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXINTERV<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **RXFIFOSZ<3:0>**: Receive FIFO Size bits

1111 = Reserved

1110 = Reserved

1101 = 8192 bytes

1100 = 4096 bytes

•

•

•

0011 = 8 bytes

0010 = Reserved

0001 = Reserved

0000 = Reserved or endpoint has not been configured

This register only has this interpretation when dynamic sizing is not selected. It is not valid where dynamic FIFO sizing is used.

bit 27-24 **TXFIFOSZ<3:0>**: Transmit FIFO Size bits

1111 = Reserved

1110 = Reserved

1101 = 8192 bytes

1100 = 4096 bytes

•

•

•

0011 = 8 bytes

0010 = Reserved

0001 = Reserved

0000 = Reserved or endpoint has not been configured

This register only has this interpretation when dynamic sizing is not selected. It is not valid where dynamic FIFO sizing is used.

bit 23-16 **Unimplemented**: Read as '0'

NOTES:

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 20-2: SQI1XCON2: SQI XIP CONTROL REGISTER 2**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DEVSEL<1:0>		MODEBYTES<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MODECODE<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11-10 **DEVSEL<1:0>:** Device Select bits

11 = Reserved

10 = Reserved

01 = Device 1 is selected

00 = Device 0 is selected

bit 9-8 **MODEBYTES<1:0>:** Mode Byte Cycle Enable bits

11 = Three cycles

10 = Two cycles

01 = One cycle

00 = Zero cycles

bit 7-0 **MODECODE<7:0>:** Mode Code Value bits

These bits contain the 8-bit code value for the mode bits.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 20-25: SQI1XCON3: SQI XIP CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	R/W-0 INIT1SCHECK	R/W-0 INIT1COUNT<1:0>	R/W-0	R/W-0 INIT1TYPE<1:0>	R/W-0
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT1CMD3<7:0> <sup>(1)</sup>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT1CMD2<7:0> <sup>(1)</sup>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT1CMD1<7:0> <sup>(1)</sup>							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **INIT1SCHECK:** Flash Initialization 1 Command Status Check bit

1 = Check the status after executing the INIT1 command

0 = Do not check the status

bit 27-26 **INIT1COUNT<1:0>:** Flash Initialization 1 Command Count bits

11 = INIT1CMD1, INIT1CMD2, and INIT1CMD3 are sent

10 = INIT1CMD1 and INIT1CMD2 are sent, but INIT1CMD3 is still pending

01 = INIT1CMD1 is sent, but INIT1CMD2 and INIT1CMD3 are still pending

00 = No commands are sent

bit 25-24 **INIT1TYPE<1:0>:** Flash Initialization 1 Command Type bits

11 = Reserved

10 = INIT1 commands are sent in Quad Lane mode

01 = INIT1 commands are sent in Dual Lane mode

00 = INIT1 commands are sent in Single Lane mode

bit 24-16 **INIT1CMD3<7:0>:** Flash Initialization Command 3 bits<sup>(1)</sup>

Third command of the Flash initialization.

bit 15-8 **INIT1CMD2<7:0>:** Flash Initialization Command 2 bits<sup>(1)</sup>

Second command of the Flash initialization.

bit 7-0 **INIT1CMD1<7:0>:** Flash Initialization Command 1 bits<sup>(1)</sup>

First command of the Flash initialization.

**Note 1:** INIT1CMD1 can be WEN and INIT1CMD2 can be SECTOR UNPROTECT.

**Note:** Some Flash devices require Write Enable and Sector Unprotect commands before read/write operations and this register is useful in working with those Flash types (XIP mode only)

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 22-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	R/W-0 ADM_EN
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-1
	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT
7:0	R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/W-0	R-0
	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **ADM\_EN:** Automatic Address Detect Mode Enable bit

- 1 = Automatic Address Detect mode is enabled
- 0 = Automatic Address Detect mode is disabled

bit 23-16 **ADDR<7:0>:** Automatic Address Mask bits

When the ADM\_EN bit is '1', this value defines the address character to use for automatic address detection.

bit 15-14 **UTXISEL<1:0>:** TX Interrupt Mode Selection bits

- 11 = Reserved, do not use
- 10 = Interrupt is generated and asserted while the transmit buffer is empty
- 01 = Interrupt is generated and asserted when all characters have been transmitted
- 00 = Interrupt is generated and asserted while the transmit buffer contains at least one empty space

bit 13 **UTXINV:** Transmit Polarity Inversion bit

If IrDA mode is disabled (i.e., IREN (UxMODE<12>) is '0'):

- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IrDA mode is enabled (i.e., IREN (UxMODE<12>) is '1'):

- 1 = IrDA encoded UxTX Idle state is '1'
- 0 = IrDA encoded UxTX Idle state is '0'

bit 12 **URXEN:** Receiver Enable bit

- 1 = UARTx receiver is enabled. UxRX pin is controlled by UARTx (if ON = 1)
- 0 = UARTx receiver is disabled. UxRX pin is ignored by the UARTx module

bit 11 **UTXBRK:** Transmit Break bit

- 1 = Send Break on next transmission. Start bit followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Break transmission is disabled or completed

bit 10 **UTXEN:** Transmit Enable bit

- 1 = UARTx transmitter is enabled. UxTX pin is controlled by UARTx (if ON = 1)
- 0 = UARTx transmitter is disabled. Any pending transmission is aborted and buffer is reset

bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only)

- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register is Empty bit (read-only)

- 1 = Transmit shift register is empty and transmit buffer is empty (the last transmission has completed)
- 0 = Transmit shift register is not empty, a transmission is in progress or queued in the transmit buffer

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 26-3: CEBDADDR: CRYPTO ENGINE BUFFER DESCRIPTOR REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **BDPADDR<31:0>**: Current Buffer Descriptor Process Address Status bits

These bits contain the current descriptor address that is being processed by the Buffer Descriptor Processor (BDP).

**REGISTER 26-4: CEBDPADDR: CRYPTO ENGINE BUFFER DESCRIPTOR PROCESSOR REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **BASEADDR<31:0>**: Buffer Descriptor Base Address bits

These bits contain the physical address of the first Buffer Descriptor in the Buffer Descriptor chain. When enabled, the Crypto DMA begins fetching Buffer Descriptors from this address.



# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## REGISTER 28-18: ADCTRG2: ADC TRIGGER SOURCE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC7<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC6<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC5<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC4<4:0>				

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC7<4:0>:** Trigger Source for Conversion of Analog Input AN7 Select bits

11111 = Reserved

•  
•  
•

01101 = Reserved

01100 = Comparator 2 (COUT)

01011 = Comparator 1 (COUT)

01010 = OCMP5

01001 = OCMP3

01000 = OCMP1

00111 = TMR5 match

00110 = TMR3 match

00101 = TMR1 match

00100 = INT0 External interrupt

00011 = STRIG

00010 = Global level software trigger (GLSWTRG)

00001 = Global software edge Trigger (GSWTRG)

00000 = No Trigger

For STRIG, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSSx registers.

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TRGSRC6<4:0>:** Trigger Source for Conversion of Analog Input AN6 Select bits

See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC5<4:0>:** Trigger Source for Conversion of Analog Input AN5 Select bits

See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC4<4:0>:** Trigger Source for Conversion of Analog Input AN4 Select bits

See bits 28-24 for bit value definitions.

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 29-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	WAKFIL	—	—	—	SEG2PH<2:0> <sup>(1,4)</sup>		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SEG2PHTS <sup>(1)</sup>	SAM <sup>(2)</sup>	SEG1PH<2:0>			PRSEG<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SJW<1:0> <sup>(3)</sup>		BRP<5:0>					

**Legend:** HC = Hardware Clear S = Settable bit  
R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit  
U = Unimplemented bit -n = Bit Value at POR: ('0', '1', x = Unknown)

bit 31-23 **Unimplemented:** Read as '0'

bit 22 **WAKFIL:** CAN Bus Line Filter Enable bit  
1 = Use CAN bus line filter for wake-up  
0 = CAN bus line filter is not used for wake-up

bit 21-19 **Unimplemented:** Read as '0'

bit 18-16 **SEG2PH<2:0>:** Phase Buffer Segment 2 bits<sup>(1,4)</sup>

111 = Length is 8 x Tq

•  
•  
•

000 = Length is 1 x Tq

bit 15 **SEG2PHTS:** Phase Segment 2 Time Select bit<sup>(1)</sup>

1 = Freely programmable

0 = Maximum of SEG1PH or Information Processing Time, whichever is greater

bit 14 **SAM:** Sample of the CAN Bus Line bit<sup>(2)</sup>

1 = Bus line is sampled three times at the sample point

0 = Bus line is sampled once at the sample point

bit 13-11 **SEG1PH<2:0>:** Phase Buffer Segment 1 bits<sup>(4)</sup>

111 = Length is 8 x Tq

•  
•  
•

000 = Length is 1 x Tq

**Note 1:**  $SEG2PH \leq SEG1PH$ . If SEG2PHTS is clear, SEG2PH will be set automatically.

**2:** 3 Time bit sampling is not allowed for BRP < 2.

**3:**  $SJW \leq SEG2PH$ .

**4:** The Time Quanta per bit must be greater than 7 (that is, TqBIT > 7).

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 29-3: CiINT: CAN INTERRUPT REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIF	WAKIF	CERRIF	SERRIF <sup>(1)</sup>	RBOVIF	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

- bit 31      **IVRIE:** Invalid Message Received Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 30      **WAKIE:** CAN Bus Activity Wake-up Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 29      **CERRIE:** CAN Bus Error Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 28      **SERRIE:** System Error Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 27      **RBOVIE:** Receive Buffer Overflow Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 26-20   **Unimplemented:** Read as '0'
- bit 19      **MODIE:** Mode Change Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 18      **CTMRIE:** CAN Timestamp Timer Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 17      **RBIE:** Receive Buffer Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 16      **TBIE:** Transmit Buffer Interrupt Enable bit  
             1 = Interrupt request is enabled  
             0 = Interrupt request is not enabled
- bit 15      **IVRIF:** Invalid Message Received Interrupt Flag bit  
             1 = An invalid messages interrupt has occurred  
             0 = An invalid message interrupt has not occurred

**Note 1:** This bit can only be cleared by turning the CAN module off and on by clearing or setting the ON bit (CiCON<15>).

40.0 AC AND DC CHARACTERISTICS GRAPHS

**Note:** The graphs provided are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 40-1:  $V_{OH}$  – 4x DRIVER PINS

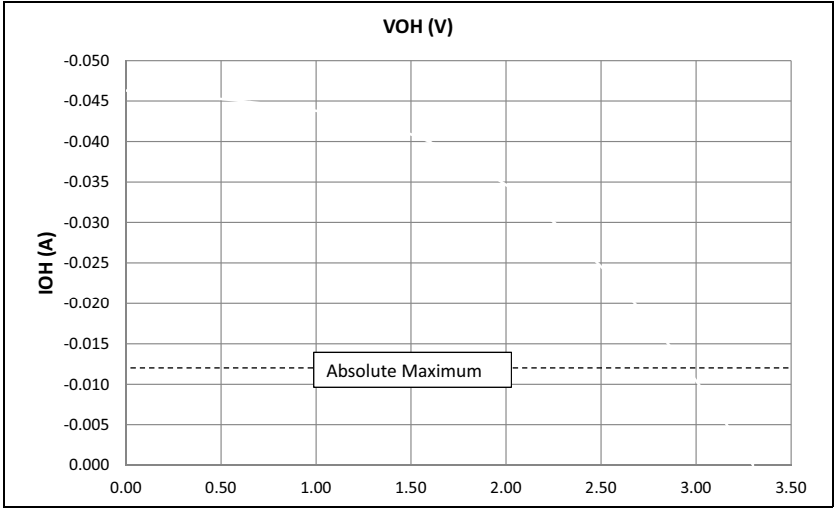


FIGURE 40-3:  $V_{OH}$  – 8x DRIVER PINS

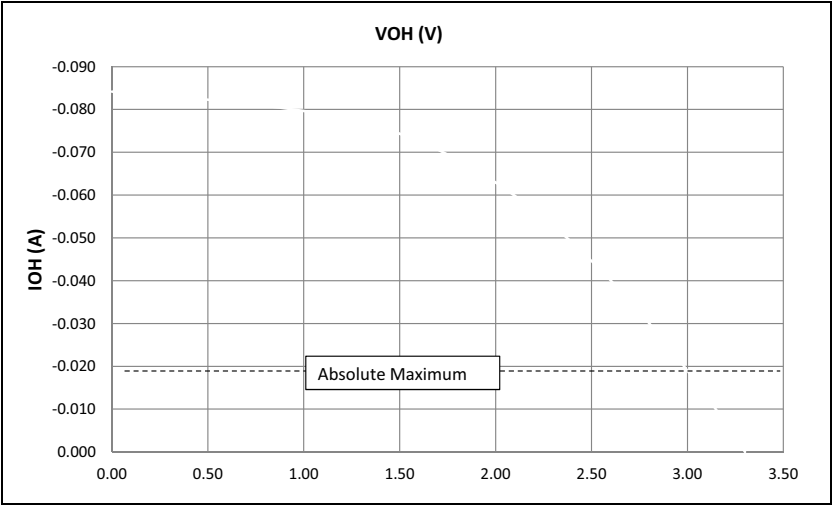


FIGURE 40-2:  $V_{OL}$  – 4x DRIVER PINS

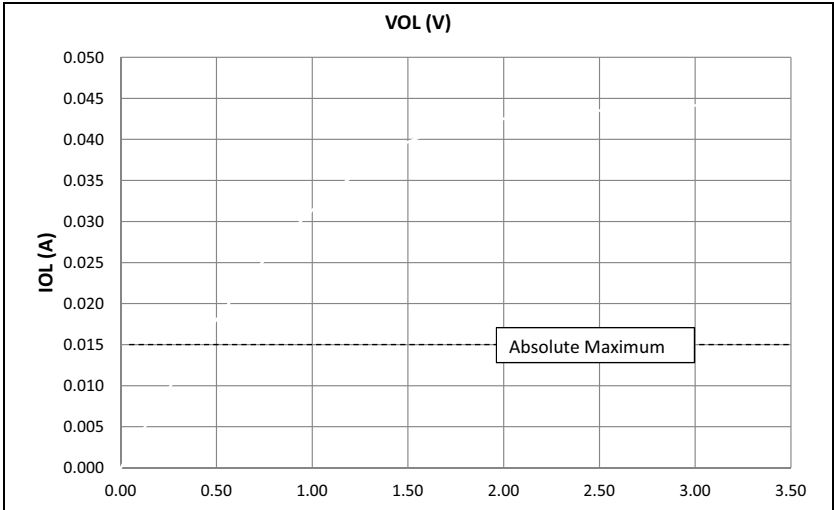
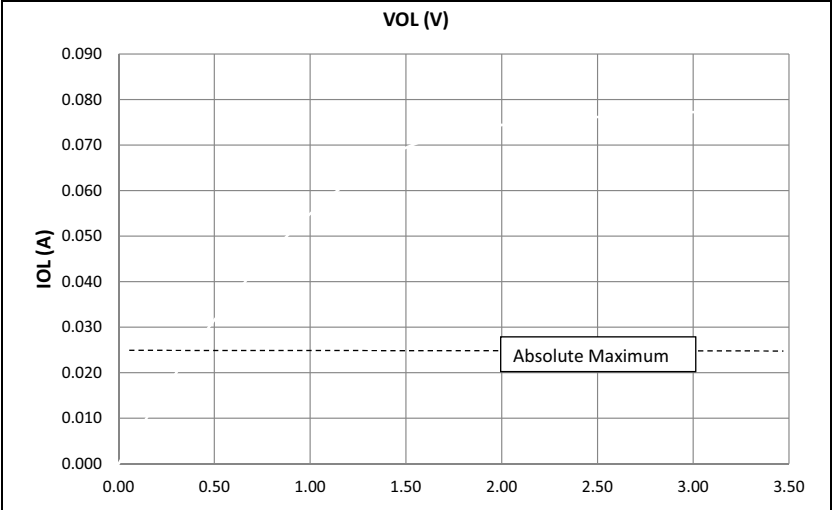


FIGURE 40-4:  $V_{OL}$  – 8x DRIVER PINS



# PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

## B.2 Analog-to-Digital Converter (ADC)

The PIC32MZ EC family features a Pipelined ADC module, while the PIC32MZ EF family of devices has an entirely new 12-bit High-Speed SAR ADC module. Nearly all registers in this new ADC module differ from the registers in PIC32MZ EC devices. Due to this difference, code will not port from PIC32MZ EC devices to PIC32MZ EF devices. Table B-2 lists some of the differences in registers to note to adapt code as quickly as possible.

**TABLE B-2: ADC DIFFERENCES**

PIC32MZ EC Feature	PIC32MZ EF Feature
<b>Clock Selection and Operating Frequency (TAD)</b>	
On PIC32MZ EC devices, there are three possible sources of the ADC clock: FRC, REFCLKO3, and SYSCLK.	On PIC32MZ EF devices, there are four sources for the ADC clock. In addition to the ones for PIC32MZ EC, PBCLK4 is added as a source. Also, the clock source selection is in a different register.
ADCSEL<1:0> (AD1CON1<9:8>) 11 = FRC 10 = REFCLKO3 01 = SYSCLK 00 = Reserved	ADCSEL<1:0> (ADCCON3<31:30>) 11 = FRC 10 = REFCLKO3 01 = SYSCLK 00 = <b>PBCLK4</b>
<b>Scan Trigger Sources</b>	
On PIC32MZ EC devices, there are 10 available trigger sources for starting ADC sampling and conversion.	On PIC32MZ EF devices, two new sources have been added. One is a shared trigger source (STRIG). The other is a Global Level Software Trigger (GLSWTRG). With the GLSWTRG, the conversions continue until the bit is cleared in software.
STRGSRC<4:0> (AD1CON1<26:22>) 11111 = Reserved . . . 01101 = Reserved 01100 = Comparator 2 COUT 01011 = Comparator 1 COUT 01010 = OCMP5 01001 = OCMP3 01000 = OCMP1 00111 = TMR5 match 00110 = TMR3 match 00101 = TMR1 match 00100 = INT0 00011 = <b>Reserved</b> 00010 = <b>Reserved</b> 00001 = Global Software Trigger (GSWTRG) 00000 = No trigger	TRGSRC<4:0> (ADCTRGx<y:z>) 11111 = Reserved . . . 01101 = Reserved 01100 = Comparator 2 COUT 01011 = Comparator 1 COUT 01010 = OCMP5 01001 = OCMP3 01000 = OCMP1 00111 = TMR5 match 00110 = TMR3 match 00101 = TMR1 match 00100 = INT0 00011 = <b>STRIG</b> 00010 = <b>Global Level Software Trigger (GLSWTRG)</b> 00001 = Global Software Trigger (GSWTRG) 00000 = No trigger
<b>Debug Mode</b>	
On PIC32MZ EC devices, the ADC module continues operating when stopping on a breakpoint during debugging.	On PIC32MZ EF devices, the ADC module will stop during debugging when stopping on a breakpoint.
<b>Electrical Specifications and Timing Requirements</b>	
Refer to the “ <b>Electrical Characteristics</b> ” chapter in the PIC32MZ EC data sheet for ADC module specifications and timing requirements.	On PIC32MZ EF devices, the ADC module sampling and conversion time and other specifications have changed. Refer to <b>37.0 “Electrical Characteristics”</b> for more information.
<b>ADC Calibration</b>	
PIC32MZ EC devices require calibration values be copied into the AD1CALx registers before turning on the ADC. These values come from the DEVADCx registers.	PIC32MZ EF devices also require ADC calibration values, but the destination registers are named ADCxCAL.